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PRODUCT BRIEF
February 2017

Proc10A™

PCIe x8 (Gen 3) FPGA Computation Accelerators

Key Features

- Altera Arria 10 (GX660,1150, SX660) FPGAs
- PCI Express Gen3 x8 or Stand-alone(Option)
- Dynamically reconfigurable FPGA(Not ready)
- Up to 15×12.5 GB/s reconfigurable transceivers supporting multiple protocols and data rates
- Up to 40 GFLOPS-per-Watt
- 1 QSFP suitable for 40 GbE or 4×10 GbE Ethernet, single Infiniband QDR link, or up to 4×12.5 Gb/s
- 3 SFP+ cage suitable for 8 Gb/s Fiber Channel, 10-Gigabit Ethernet and Optical Transport Network standard OTU2 or up to 3×12.5 Gb/s
- High-Speed Inter-Board connectors (up to 8×12.5 Gb/s full duplex GPIO) for board-to-board connectivity and Proc High-Speed (***PHS***) daughter board, including 8 links of Mini-SAS-HD and 8×SATA-3 Interface options
- 12 general purpose LVTTL External IOs
- Optional: 1 PPS or External clock input
- Multi-level memory structure (**17+ GB**)

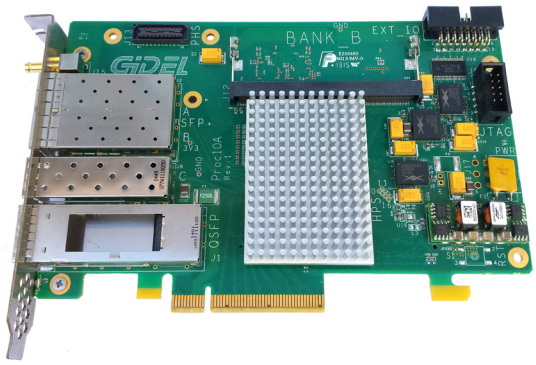
  Sustain throughput of **10,000 GB/s** for internal memories and ~**20 GB/s** for on-board memory as follows:

  - ✓ Enhanced MLAB (640-bit) SRAM blocks
  - ✓ Up to 2,713 M20K (20K-bit) SRAM blocks (53 Mb) with a typical throughput of **10,000 GB/s** at 450 MHz
  - ✓ DDR3 1GB 1400 MT/s on-board memory at a maximum sustain throughput of **3.9GB/s**
  - ✓ 2×DDR3 SoDIMM Banks with up to a total of 16 GB at a maximum sustain throughput of **15.6 GB/s**

- Typical system frequencies: 150-450 MHz
- Flexible clocking system
- Low power (8-70W)
- MTBF of over 1.5 million hours
- Support for OpenCL™
- Supported by Gidel's ***ProcDeveloper's Kit***

Benefits

- Leading edge performance and modular flexibility
- Advanced development tools reducing the development cycle and simplifying maintenance and upgrade tasks
- Maintainability, reliability and long-life cycle



Overview

The Proc10A system optimizes processing power, memory capacity and access speed, I/O performance, system tailoring capability, low-power consumption and cost. Proc10A can accelerate a computer via its PCIe port or it may be a fully independent compute engine in its stand-alone SoC-based models that include an internal ARM CPU. This powerful compute engine is supported by OpenCL and Gidel innovative developing tools enabling high productivity based on C and HDL designs.

The Proc10A is based on Altera's newest generation Arria 10 (20 nm) FPGA devices providing up to 1150K LEs and IEEE floating-point capability. In addition to the PCIe x8 (gen 3), the Proc10A has fifteen 12.5 Gb/s transceivers providing external IOs of up to 187 Gb/s (full duplex). These 15 transceivers enable direct links to standard networking, up to one QSFP and 3×SFP+, as well as FPGA-to-FPGA or computer-to-computer communication with direct links at small latency.
These links may be used for many system topologies including 3D torus and 4-way tree. Direct disk connection to 8 links of Mini SAS-HD or SATA-3 may be used in parallel to QSFP or SFP+ connections. The memory scheme includes an embedded SRAM memory with ~10.0 TB/s throughput, 1GB DDR III, and up to 16 GB DDR III. The DDR memory may be accessed via up to 48 parallel ports simultaneously.

The Proc10A SoC boards based on SX devices offer SD Memory interface as well as stand-alone capability. The Stand-alone models have full system capability suitable for IoT (Internet Of Things) and other embedded applications. The PCIe based SoC enables real-time low-latency support for the FPGA processing using shared 1GB on-board memory as well as FPGA fabric memory and registers.

Target Application Examples

- ✓ DSP (Digital Signal Processing) and HPRC (High Performance Reconfigurable Computing)
- ✓ High-speed low-latency networking and network analysis
- ✓ Life science Applications
- ✓ Linear algebra and 3D applications
- ✓ Computational Finance and HFT
- ✓ Data Analytics
- ✓ Deep Packet Inspection
- ✓ Surveillance, Machine Vision and Imaging
- ✓ High-performance acquisition systems

Development Environment

Based on Altera's SDK availability, Gidel will support the **OpenCL™** programming model providing means to develop on Gidel's Proc10A board. OpenCL is a royalty-free, open standard model enabling developers to use C-based language to execute program across heterogeneous systems including FPGAs, CPUs, GPUs and DSPs.

The ProcDeveloper's Kit, Gidel's intuitive design and debug environment, enables easy and fast development of the HDL optimal design on the Proc10A system. The kit contains ***ProcWizard***™ Development Application, ***ProcMultiPort***™ and other IPs, ***Quartus II*** and ***USB Blaster***.

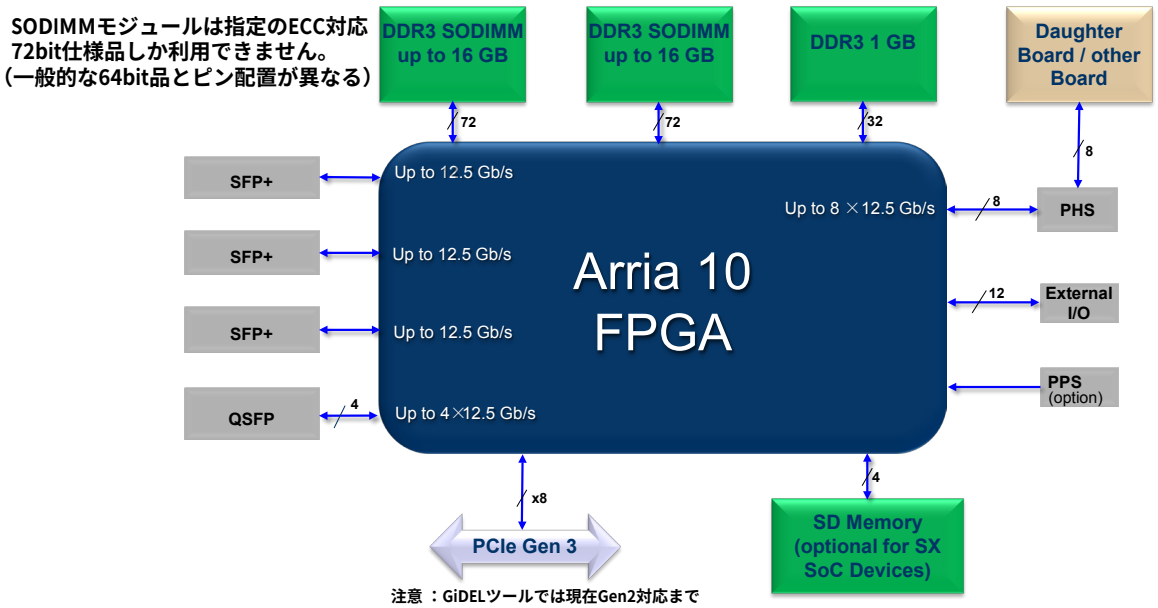
For other high-level design entry options, please contact the Gidel support.

The ***ProcWizard*** performs hardware initialization and automatically generates the following:

- Top-level designs, interface modules/entities, and on-board memory controllers for application use.
- Device constraints (e.g., timing, pin-outs and drive strength).
- C++ class application driver enabling the host to access the FPGA code using tailored class. The application driver improves the development process and eliminates performance degradation and other communication layers artifacts.
- Interface documentation in HTML or MS Word.

The ***ProcMultiPort*** IP and other Gidel memory and data management IPs provide simple and efficient data processing and access to on-board memory. The ProcMultiPort splits the memory into several logical memories, each accessible simultaneously by multiple ports. As a result, the on-board memory is mapped according to the desired algorithm and not vice versa. The main benefits are:

- Simplification of design and enhanced system performance.
- Design compatibility and migration amongst legacy and future Gidel Proc boards.
- Replaces the need for inventory of special memories by using standard field-tested IPs.



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