Think Speed think Gidel™

Arria10GX 480搭載 HawkEye-40GPは立野電脳(株)でアカデミック向け19万円台。浮動小数点乗算加算器は1368個。60万円台のGX1150で1518個なので、この点の単純比較では約３倍のコスパ。

ADAVANCE INFORMATION
October 2016

HawkEye™

40/56 Gbps Arri10 FPGA Computation Accelerators

Key Features

- Intel Programmable Solutions Group(Altera) Arria 10 160 or 480
- PCIe x8 Gen. 3 Express or Stand-alone
- Form factor: low-profile
- Low-power starting at less than 15W
- Up to 4 SFP+ cage suitable for 8 Gb/s Fiber Channel, 10-Gigabit Ethernet and Optical Transport Network standard OTU2 or up to 4×14.2 Gb/s
- MTBF > million hours
- Cost-effective solutions
- Dedicated features enabling tailoring to vertical markets
- Dynamically reconfigurable FPGA
- Multi-level memory structure (**18+ GB**)

  Sustain throughput of **6,000+ GB/s** for internal memories and ~**16 GB/s** for on-board memory as follows:
  - ✓ Enhanced MLAB (640-bit) SRAM blocks
  - ✓ Up to 1,431M20K (20K-bit) SRAM blocks (28 Mb) with a typical throughput of **6,000 GB/s** at 450 MHz
  - ✓ 1-2GB DDR4 on-board memory at a maximum sustain throughput of **5.4 GB/s**
  - ✓ 8-16 GB DDR4 ECC SoDIMM Bank for maximum sustain throughput of **10.8 GB/s** (480 device only)
- Typical system frequencies: 150-450 MHz
- Flexible clocking system
- Support for OpenCL™ - Open Computing Language programming model (for 480 device only)
- Supported by Gidel's ***ProcDeveloper's Kit***
  - ✓ Acceleration of multi-applications/process simultaneously
  - ✓ Unmatched HDL design productivity
  - ✓ Simplification of integration with Software applications

Benefits

- Advanced development tools reducing the development cycle and simplifying maintenance and upgrade tasks
- Maintainability, reliability and long-life cycle
- Best-in-class cost performance

この写真は概要紹介用イメージです。最終納品物ではありません。

Overview

The HawkEye is low-profile PCIe accelerator based on Intel PSG (ex. Altera) Arria 10 FPGAs. The platform boasts up to 18 GB DDR4 on-board memory, up to 4 SFP+ links for a maximum of 56 Gbps, and a PCIe x8 Gen. 3 host interface.

The Arria 10 FPGA provides up to 480K LEs and IEEE floating-point capability. The HawkEye's memory scheme comprises embedded SRAM memory with ~6.0 TB/s throughput, 1-2 GB DDR4, and up to 16 GB of DDR4 SoDIMM (only for boards with 480 devices). The DDR memory may be accessed via up to 48 parallel ports simultaneously. The HawkEye accelerator board exhibits an impressive power efficiency starting from less than 15W.

In addition to abundant GPIOs that include RS422, Opto-coupler, External clock, LVDS, LVTTL (3V), 30V/0.9A output, the HawkEye is designed with dedicated features tailored for vertical markets such as network security and HFT.

The HawkEye can operate as a PCIe-based platform or as a stand-alone compute accelerator. The system has been designed for exceptional high reliability with an MTBF beyond 1 Million hours.

The HawkEye presents an unprecedented cost-performance solution providing high-end FPGA capabilities previously considered beyond the budget of many applications. At a remarkable sub-$1000 starting price, the HawkEye family opens the way for acceleration of diverse applications that can immensely benefit from high-end FPGA capabilities.

Target Application Examples

- ✓ Network security, processing and analysis
- ✓ DSP and High Performance Reconfigurable Computing (HPRC)
- ✓ Computational Finance and High Frequency Trading (HFT)
- ✓ Deep Packet Inspection
- ✓ Life science Applications
- ✓ Data Analytics
- ✓ Surveillance, Machine Vision and Imaging

Development Environment

Gidel offers two powerful development methodologies:

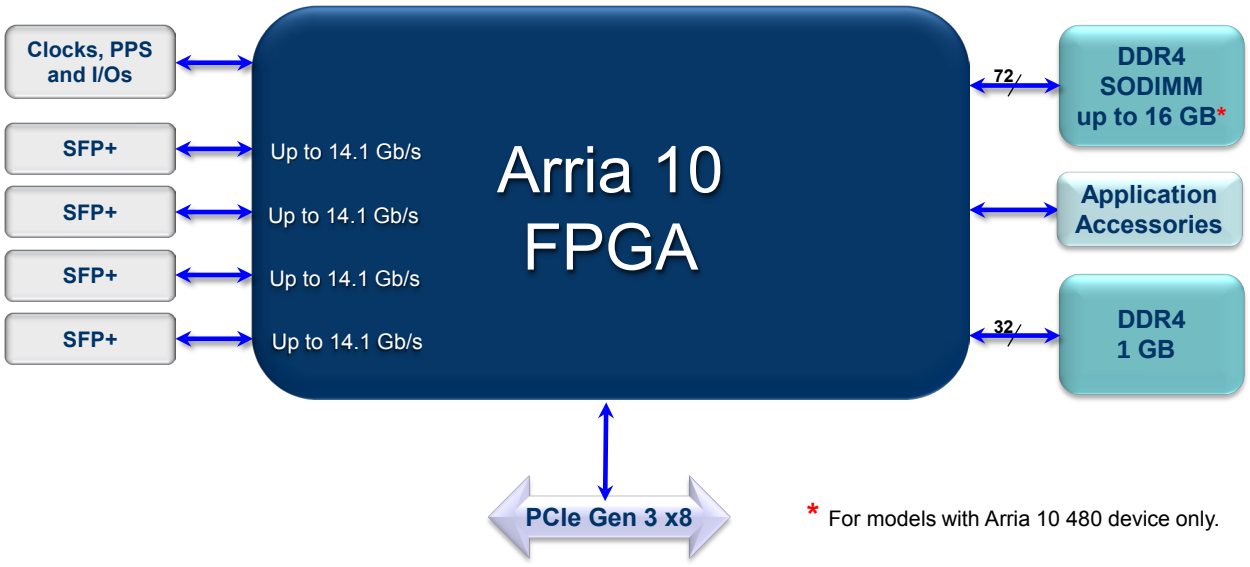
1. Open Computing Language (OpenCL™) based on Intel PSG's SDK and Gidel Developer's bundle for high-level development flow (available for 480 devices only).
2. The ProcDeveloper's Kit, Gidel's intuitive design and debug environment, enabling acceleration of multi-application/process simultaneously and unmatched productivity. The kit includes Gidel's ProcWizard application, libraries and memory controller IPs.

The ***ProcWizard*** application performs hardware initialization and automatically generates the following:

- Top-level designs, interface modules/entities, and on-board memory controllers for application use.
- Device constraints (e.g., timing, pin-outs and drive strength).
- C++ class application driver enabling the host to access the FPGA code using tailored class. The application driver improves the development process and eliminates performance degradation and other communication layers artifacts.
- Interface documentation in HTML or MS Word.

The ***ProcMultiPort*** IP and other Gidel memory and data management IPs provide simple and efficient data processing and access to on-board memory. The ProcMultiPort splits the memory into several logical memories, each accessible simultaneously by multiple ports. As a result, the on-board memory is mapped according to the desired algorithm and not vice versa. The main benefits are:

- Simplification of design and enhanced system performance.
- Design compatibility and migration amongst legacy and future Gidel Proc boards.
- Replaces the need for inventory of special memories by using standard field-tested IPs.



HawkEye System Diagram

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