March 2010

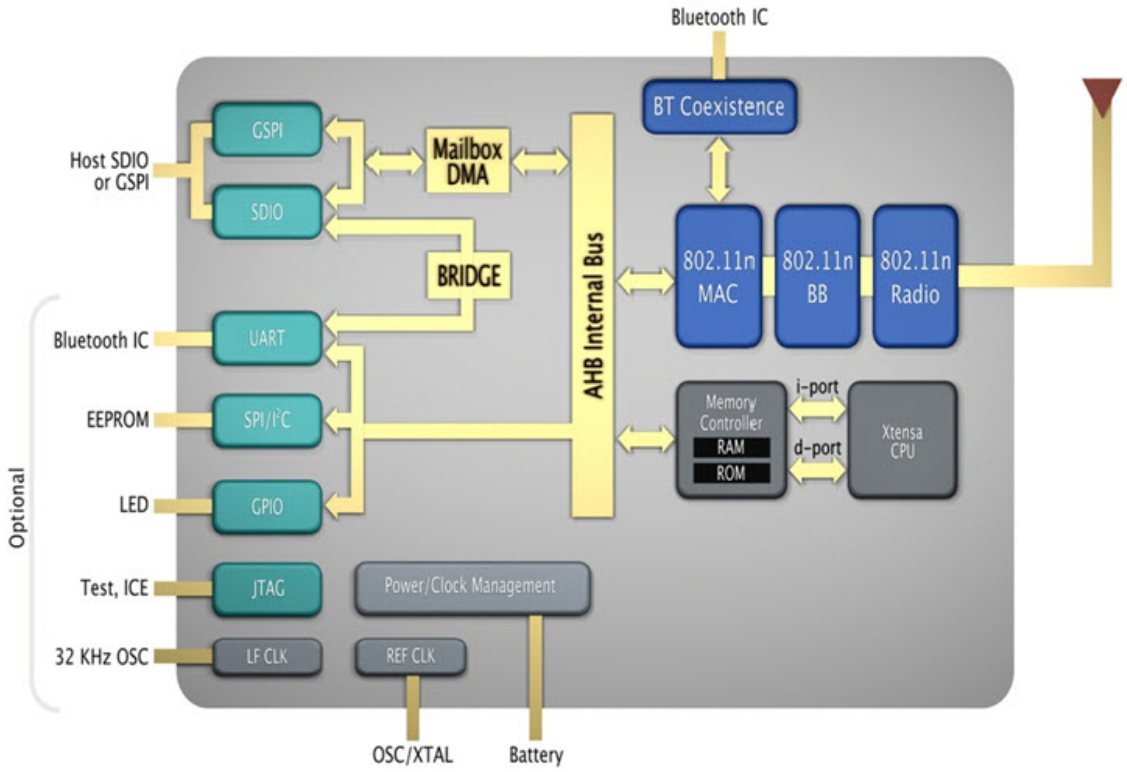
AR6103 ROCm™ Integrated 802.11n

General Description

The AR6103 is a small form factor 802.11 b/g/n WiFi solution optimized for low-power, low-cost and highly integrated mobile and portable CE devices.

The AR6103 is part of the 3rd generation ROCm™ family of mobile 11n devices, employing the world's lowest power consumption embedded architecture.

The AR6103 can support any number of external Bluetooth devices, and includes advanced PTA coexistence support. A flexible architecture enables optional customization to meet customer specific profiles and use cases.



AR6103 Block Diagram

On-chip high-efficiency high-output EPA™ power amplifier and integrated LNAs with zero calibration eliminate the need for external RF components. Ultra low power consumption radio architecture and proprietary power save technologies extend battery life. On-chip high-efficiency PMU (power management unit) enables direct-connect to battery, eliminating the need for external regulators. An on-chip embedded CPU handles complete 11n processing to minimize host processor loading.

The AR6103 is available in a low profile 8.3mm x 9.2mm LGA package with 500um pitch pads for robust low-cost PCB design.

The AR6103 can be treated as a single -row QFN for direct on-board designs.

The AR6103 is halogen-free, Pb-free and fully ROHS compliant.

AR6103 Features

AR6103S - High performance, ultra-low power, single stream (1x1) IEEE 802.11n featuring:

- Half Guard Interval for high max throughput;
- Frame Aggregation for high max throughput;
- Space Time Block Coding (STBC) for improved downlink robustness over range; and
- Low Density Parity Check (LDPC) encoding for improved uplink robustness over range
- Near zero power consumption in idle and stand-by enables users to leave Wi-Fi always on"
- Integrated high-power, high efficiency linearized Power Amplifier
- Best in class Rx sensitivity for superior throughput rate-over-range performance
- Support for standard interfaces including:
- SDIO 2.0 (50MHz, 4-bit and 1-bit)
- Integrated Sleep Clock eliminates the need for expensive bulky 32kHz real-time clock
- Integrated conformal RF shielding and near-zero RBOM for lowest cost
- Atheros proprietary Ap Mode for mobile devices, and DirectConnect™ Peer-to-Peer connectivity.

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1. Features Summary

1.1 Overview

The AR6103 is a single package combination IEEE 80211 (b, g, n) based on cutting edge technology from the AR6003 ROCm™ family of mobile 11n. The AR6103 contains 802.11 including full digital MAC and baseband engines handling all 802.11b (CCK), 11g/n (OFDM). An embedded low-power CPU cores minimize host loading and maximize flexibility to support customer specific profiles and use cases.

The AR6103 is architected for ultra-low power consumption, with near zero power consumption in idle and stand-by modes, enabling users to leave Wi-Fi "always on".

A pin-compatible standalone 802.11n plus advanced Bluetooth device (AR6133) is also available.

1.2 Radio Front End

The AR6103 features a high-power high-efficiency on-chip power amplifier featuring Atheros proprietary EPA™ linearization technology for Wi-Fi, and highly integrated LNAs enable high performance, low power consumption, and near-zero RBOM for lowest cost.

1.3 Power Management

The AR6103 features direct connection to battery, eliminating the need for external regulators and/or PMU. The AR6103 supports operating voltage from 4.8V down to 2.5V and is tolerant of momentary overvoltage up to 5.5V. An on-chip switching regulator supports PWM mode and burst mode to optimize power efficiency under both peak operation and low load conditions. An internal PMU with separate analog and digital LDO regulation provides superior noise isolation for analog and digital supplies.

An optional PMU bypass mode, disables the on-chip switching regulator to allow an external 1.8V regulated supply to directly power the device, if so desired.

The AR6103 power management engine utilizes advanced power save techniques such as: gating clocks to idle or inactive blocks, voltage scaling to specific blocks in certain states, fast start and settling circuits to reduce Tx and active duty cycles, CPU frequency scaling, and other techniques to optimize power consumption across all operation states.

1.4 Manufacturing Calibration

The AR6103 utilizes internal self-calibration and BIST (built-in self test) circuits to maintain optimal performance over temperature, time and process variation. The AR6103 is delivered fully tested and does not require any customer manufacturing line calibration.

1.5 Internal One-Time Programmable Memory

The AR6103 includes internal one-time programmable memory which may be used to store the device MAC address, eliminating the need for external EEPROM.

1.6 Reference Frequency

The AR6103 incorporates an on-chip 26MHz (20ppm) reference frequency source. Internally, the system reference frequency is sleep regulated and gated to enable the internal crystal to be powered down when the device is in sleep mode. Manufacturing calibration of the crystal is not required, but is supported as an option.

1.7 Internal Sleep Clock

The AR6103 incorporates integrated on-chip low power sleep clocks to regulate internal timing, eliminating the need for any external 32kHz real time clocks or crystal oscillators.

1.8 Interfaces

The AR6103 supports SDIO 1.x and the latest 2.0 standard.

1.8.1 Standard Host Interface

The AR6103 supports industry standard SDIO 2.0 (50MHz, 4-bit and 1-bit) and GSPI (Generic SPI) for Wi-Fi.

1.9 Mobile 802.11n

The AR6103 incorporates the latest generation of mobile 802.11n technology from Atheros. The AR6103 is draft 802.11n compliant and features Frame aggregation, reduced inter-frame spacing (RIFS) and half guard intervals

for improved throughput and space time block codes (STBC) on downlink receptions and Low Density Parity Check (LDPC) codes on uplink transmissions for improved robustness over range. Table 1-1 shows the 1 802.11n (PHY layer) throughput at different modulations.

Table 1-1. **802.11n (PHY layer) Throughput at Different Modulations**

Mode	MCS	Modulation	Data Rate (Mbps)	
			20MHz	
			FGI	HGI
IEEE 802.11n	0	BPSK	6.5	7.2
	1	QPSK	13.0	14.4
	2	QPSK	19.5	21.7
	3	16-QAM	26.0	29.9
	4	16-QAM	39.0	43.3
	5	64-QAM	52.0	57.8
	6	64-QAM	58.5	65.0
	7	64-QAM	65.0	72.2

Host interface design optimized for high throughput, low latency, and very low host loading enable high effective throughput. See Table 1-2.

Table 1-2. **Effective 802.11n Throughput**

MCS	Modulation	TCP Data Rate (Mbps)	
		20MHz	
		FGI	HGI
0	BPSK	5.6	6.1
1	QPSK	10.9	12.0
2	QPSK	16.1	17.7
3	16-QAM	21.1	23.3
4	16-QAM	30.5	33.5
5	64-QAM	39.2	40.8
6	64-QAM	43.4	47.4
7	64-QAM	47.4	51.8
MCS	**Modulation**	**UDP Data Rate (Mbps)**	
0	BPSK	6.1	6.7
1	QPSK	12.0	13.3
2	QPSK	17.8	19.8
3	16-QAM	23.5	26.0
4	16-QAM	34.5	38.0
5	64-QAM	44.8	49.3
6	64-QAM	49.9	54.7
7	64-QAM	54.7	60.1

Host CPU running 88MHz, SDIO 2.0, 8-subframe per A-MPDU and host assisted re-ordering

The AR6103 is fully compliant with IEEE 802.11e QoS, Wi-Fi Alliance WMM® Power Save and 802.11n power saving, ensuring the lowest possible power consumption.

The AR6103 features hardware-based AES, AES-CCMP, and TKIP engines for faster data encryption, and supports industry leading security features including Cisco CCXv4 ASD, WAPI (for China), Wi-Fi Protected Setup (WPS), along with standard WEP/WPA/WPA2 for personal and enterprise environments.

1.10 Advanced Wi-Fi Features

Advanced features such as Host wake-on-wireless and ARP (address resolution protocol) off-loading enable the Wi-Fi link to remain associated for extended periods with host processor asleep for additional deep system power savings.

Other standard Wi-Fi features include:

- WWR, 802.11d, 802.11h
- Wi-Fi Protected Setup (WPS)
- Device based scanning & roaming, tunable parameters optimized for seamless handover

- Statistics and events for monitoring
- Self-managed power state handling
- Self-contained beacon processing
- Shared authentication
- Adhoc power save
- Multiple PMK Id support
- Simulated UAPSD
- T-Spec support
- Production flow diagnostics
- Dynamic PS-Polling for enhanced coexistence performance with Bluetooth
- QoS support for VoIP applications

1.10.1 AP Mode (Mobile Hot Spot)

Atheros industry leading AP Mode feature allows the AR6103 device to operate as both a station and an Access Point, enabling seamless station-to-station interconnection with all the benefits of standard infrastructure-level simplicity (no special client software or settings required), security, and power save functionality. AP Mode enables the deployment of unique and powerful applications such as mobile 3G gateway and mobile range extension.

1.10.2 DirectConnect™ (Peer-to-Peer)

Atheros industry leading DirectConnect™ implementation of advanced peer-to-peer connectivity enables faster device-to-device data & media transfer, improved network efficiency eliminating the 'hop' through the access point, simultaneous connection to device and the internet, and simple PAN setup (with Wi-Fi Protected Setup), all with reduced power consumption to extend battery life.

1.11 Host Offloading (Wi-Fi)

The AR6103 integrates extensive hardware signal processing and an embedded on-chip CPU to offload complete 11n MAC/BB/PHY processing to minimize host processor loading and support application specific customization for gaming and mobile phones.

The AR6103 offloads the complete 802.11 a/b/g/n baseband and MAC functions as standard feature, including:

- Link Maintenance
- 802.11 frame transmission sequence to initiate the connection with an Acces Point;
- Background scanning, including transmission of Probe Request;
- Signal quality detection and automated maintenance of current Access Point list;
- Roaming to a new Access Point
- Rate Adaptation, including automatic retry
- Encapsulation of 802.3 frames from the host to 802.11 frames. This includes adding the security headers for 802.11
- Decapsulation of the 802.11 frame to 802.3 frame
- Encryption & decryption (hardware ciphers) for WEP/TKIP/AES-CCMP, and WAPI
- IEEE PowerSave. Periodic wakeup when in sleep mode to check for buffered traffic
- Packet Filtering and Host Wakeup, including ARP (Address Resolution Protocol) Response. Automated filtering of received data in the sleep mode to transfer only data packets of interest to the host.
- Frame Aggregation (A-MPDU) processing
- LDPC encode and STBC processing

Additionally, the AR6103 also provides host offloading of the following advanced features:

- TCP Checksum
- Security Negotiation

1.11.1 TCP Checksum

The AR6103 can compute the complete TCP checksum.

1.11.2 Security Negotiation

The AR6103 can perform initial and subsequent 4-way handshake offload, and initial Group Key exchange and Re-Keying.

2. WiFi Functional Description

2.1 Overview

The AR6103 is a single chip 802.11 a/b/g/n device based on cutting edge technology, optimized for low power embedded applications. The typical data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory accesses. External interfaces include SDIO or GSPI, reference clock, and front-end components as well as optional connections such as UART, SPI/I2C, GPIO, JTAG, 32 kHz source. See the AR6103 block diagram.

2.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. This CPU has four interfaces:

- The Code RAM/ROM interface (iBus), going to the Virtual Memory Controller (VMC).
- The Data RAM Interface (dBus), going to the VMC
- The AHB interface, used mainly for register accesses.
- JTAG interface for debugging

2.3 Virtual Memory Controller (VMC)

The VMC contains 256 kBytes of ROM and 256 kBytes of RAM. It has three interfaces:

- iBus,
- dBus, and
- AHB interface.

Any one of these interfaces can request access to the ROM or RAM modules within the VMC. The VMC contains arbiters to serve these three interfaces on a first-come-first-serve basis.

2.4 AHB and APB Blocks

The AHB block acts as an arbiter. It has AHB interfaces from three Masters:

- MAC,
- MBOX (from the Host), and
- CPU.

See below for more on the MBOX and MAC. Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the VMC. Data requests to the VMC are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the AR6103's main blocks. Depending on the address, the APB request can go to one of theplaces listed below:

- Radio
- VMC
- SI/SPI
- MBOX
- GPIO
- UART
- Real Time Clock (RTC), or
- MAC/BB

2.5 Master SI/SPI Control

The AR6103 has a master serial interface (SI) that can operate in two, three, or four-wire bus configurations to control EEPROMs or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the two-wire bus. Multiple SPI devices are supported by sharing the clock and data signals and using separate software-controlled GPIO pins as chip selects.

An SI transaction consists of two phases: a data transmit phase of 0-8 bytes followed by a data receive phase of 0-8 bytes. The flexible SI programming interface allows software to support various address and command configurations in I2C/SPI devices. In addition, software may operate the SI in either polling or interrupt mode.

2.6 GPIO

The AR6103 has 26 GPIO pins with direct software access. Many are multiplexed with other functions such as the host interface, UART, SI, Bluetooth coexistence, etc. (see Chapter 6 for details). Each GPIO supports the following configurations via software programming:

- Internal pull-up/down options
- Input available for sampling by a software register
- Input triggering an edge or level CPU interrupt

- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the Sigma Delta Pulse-width Modulation (PWM) DAC

The AR6103 has one Sigma Delta PWM DAC that is shared by all of the GPIO pins. It allows the GPIO pins to approximate intermediate output voltage levels. The DAC has a period of 256 samples with a software controllable duty cycle. In applications where the AR6103 is driving LEDs using GPIO pins, the Sigma Delta PWM DAC can provide a continuous dimmer function.

2.7 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or GSPI. The AR6103 can handle only one of these hosts at any given time. The type of host the AR6103 uses depends upon the polarity of some package pins upon system power-up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface which is used by the external host to access the VMC memory or other registers within the AR6103.

2.8 Debug UART

The AR6103 includes a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface that is fully compatible with the 16550 UART industry standard. This UART is a general purpose UART although it is primarily used for debug.

2.9 Reset Control

The AR6103 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR6103 waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the host has initiated communication, the AR6103 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted. The only resets that stay asserted are given below:

- Warm and cold resets to the MAC
- Warm reset to the radio (The cold reset gets automatically de-asserted)

The above resets are deasserted by software. All AR6103 reset control logic resides in the RTC block to ensure stable reset generation.

2.9.1 CPU Reset

CPU reset is different from the other resets mentioned above. There are four scenarios where the CPU reset can be asserted:

1. The AR6103 CHIP_PWD_L pin is asserted or the host has not initiated communication.
2. The polarity of certain package pins are set to enable JTAG debugging via an In-Circuit Emulator (ICE). In this case, the external ICE can assert CPU reset through a package pin.
3. The polarity of a package pin is set to hold the CPU in reset until the host clears an internal AR6103 register.
4. An internal AR6103 register is set by the host to force the CPU out of an unknown state.

2.10 Reset Sequence

After a COLD_RESET event (e.g., the host toggles CHIP_PWD_L) the AR6103 will enter the HOST_OFF state and await communication from the host. From that point, the typical AR6103 COLD_RESET sequence is shown below:

1. When the host is ready to use the AR6103, it initiates communication via SDIO or GSPI.
2. The AR6103 enters the WAKEUP state then the ON state and enables the XTENSA CPU to begin executing ROM code. Software configures the AR6103 functions and interfaces. When the AR6103 is ready to receive commands from the host, it will set an internal function ready bit.
3. The host reads the ready bit and can now send function commands to the AR6103.
4. The CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register. See section "CPU Reset" on page 10.
5. The MAC cold reset and the MAC/BB warm reset will continue to stay asserted until their respective reset registers are cleared by software.

2.11 Power Management Unit

The AR6103 has a an integrated Power Management Unit (PMU) which generates all the power supplies required by its internal circuitry from an external battery connection. The only supplies needed by the AR6103 are the battery input (2.5V - 4.8V) and the host and SOC I/O supplies (1.8V - 3.3V).

The main components of the PMU are as follows:

- A switching regulator (SWREG) which produces a 1.8V supply from the battery input.
- A small linear regulator (SREG) which converts the host IO supply to a 1.2V supply for some small control blocks which are turned on when CHIP_PWD_L is de-asserted.
- A larger linear regulator (DREG) which converts the 1.8V input to 1.2V for the bulk of AR6103 core digital circuitry. The input is typically connected to the SWREG output.
- A linear regulator (PAREG) which converts the battery input to a 3.3V supply that can be used for the antenna switch controls as well as the internal AR6103 EPA.

In applications where external supplies are already present, the AR6103 supports bypassing all supplies generated by the PMU.

2.12 Power Transition Diagram

The AR6103 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

When the AR6103 is in a low power state, the switching power supply (SWREG) as well as the main 1.2V regulator for digital circuits (DREG) are both turned off. All digital circuits that normally rely upon 1.2V power from DREG are switched to use power from the smaller SREG regulator using a "Make-and-Break" mechanism.

2.12.1 Hardware Power States

AR6103 hardware has five top level hardware power states managed by the RTC block. Table 2-1 describes the input from the MAC, CPU, SDIO/MBOX, interrupt logic, and timers that affect the power states.

2.12.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. The SWREG, DREG, and PAREG supplies are also turned off during SLEEP. For the AR6103 to enter SLEEP state, the MAC, MBOX, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.

Figure 2-1 depicts the state transition diagram.

Table 2-1. **Power Management States**

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
	SWREG, SREG, DREG, and PAREG are turned off.
HOST_OFF	WLAN is turned off.
	SREG is turned on.
	SWREG, PAREG, DREG are turned off.
	Only the host interface is powered on - the rest of the chip is power gated (off).
	The host instructs the AR6103 to transition to WAKEUP by writing a register in the host interface domain.
	Embedded CPU and WLAN do not retain state (separate entry).
	This state can be bypassed by asserting FORCE_HOST_ON_L during CHIP_PWD_L deassertion.
SLEEP	Only the sleep clock is operating.
	SREG is kept on.
	SWREG, DREG, and PAREG are turned off.
	The high speed crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state.
	All internal states are maintained.
WAKEUP	The system transitions from sleep states to ON.
	SREG, SWREG, DREG, PAREG are kept on.
	The high frequency clock is gated off as the crystal or oscillator is brought up and the PLL is enabled.
	WAKEUP duration is programmable (default 3.8ms).
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	SREG, SWREG, DREG, PAREG are kept on.
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction while the system is on. No CPU, host and WLAN activities will transition to sleep states.

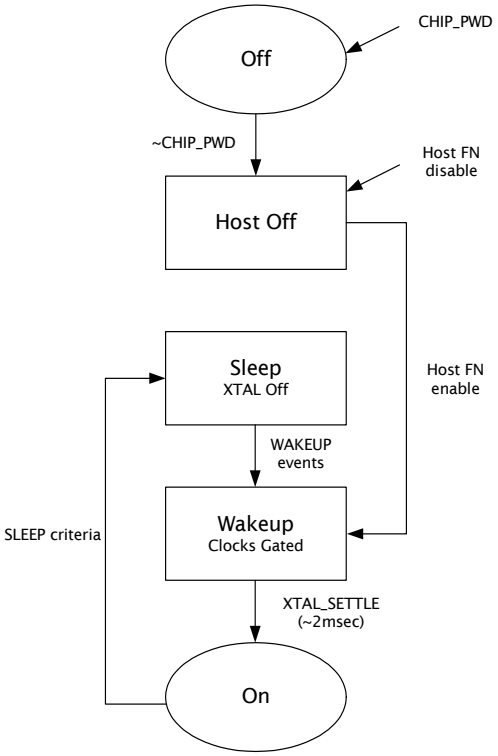

Figure 2-1. **AR6103 Power State**

2.13 System Clocking (RTC Block)

The AR6103 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR6103's clocking is grouped into two types: high-speed and low-speed.

2.13.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the AR6103. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. For an external crystal, the AR6103 disables the on-chip oscillator driver. For an external oscillator, the AR6103 de-asserts its CLK_REQ signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the AR6103 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ signal is asserted to allow for the reference clock source to settle. The CLK_REQ signal remains asserted in ON state.

The AR6103 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output whenever an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_REQ signal, and the input clock is passed along to the reference clock output.

2.13.2 Low-Speed Clocking

The AR6103 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters inside the AR6103's Power Control

Module (PCM). The PCM controls all power and isolation control signals for the entire chip.

The AR6103 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

The AR6103 also supports using an external low frequency sleep clock source in applications where one is already available.

2.13.3 Interface Clock

The host interface clock represents another clock domain for the AR6103. This clock comes from the SDIO or GSPI host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

2.14 Front End Control

For applications that use external front-end components, the AR6103 provides the ability to control them with five antenna switch control outputs named as follows:

- ANTE
- ANTD
- ANTC
- ANTB
- ANTA

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The AR6103 supports antenna sharing with another wireless chip in all power states by using ANTE to control the shared antenna switch.

2.15 MAC/BB/RF Block

The AR6103 Wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for VMC data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring TX data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring RX data

2.16 Baseband Block

The AR6103 baseband module (BB) is the physical layer controller for the 802.11a/b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

2.17 Design for Test

The AR6103 has a built in JTAG boundary scan of its pins. It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

3. Electrical Performance and Characteristics

This section describes the electrical and performance characteristics of the AR6103.

NOTE: All performance characterization is preliminary and subject to change.

Table 3-1 shows the absolute maximum ratings.

Table 3-1. **Absolute Maximum Ratings**

Specification	Symbol	Condition	Min.	Max.	Unit
Operating Voltage	*Vbat*	TA=-20 to +85C, no permanent damage or degradation	-0.5	5.5	V
Storage temperature range	T_{STG}		-55	+150	oC
Operating temperature	T_A	Ambient -20	+85	-	oC
Max Current	I_{MAX}	Current on any pin to avoid latch-up	-30	+30	mA
ESD protection	V_{ESD1}	non-RF pins and non-test monitor pins	2000	-	V
ESD protection	V_{ESD2}	RF pins and test monitor pins	250	500	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 3-2 through show the general DC electrical characteristics.

Table 3-2. **General Electrical Characteristics**

Specification	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	*Vbat*	TA=-20 to +85C	-2.5	3.0	4.2	V

Table 3-3. **Transmitter Characteristics for 802.11 Operation**

Specification	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Power	*Pout*	Mask Compliant CCK output power	+15	-	+17	dBm
		EVM Compliant OFDM output power for 64 QAM, 11g and HT20	+15	-	+17	dBm
PA gain step	SP_{gain}	-	-1.5	-	+1.5	dB
Accuracy of power leveling loop	*Apl*	-	-1.5	-	+1.5	dB

Table 3-4. **Receiver Characteristics for 802.11 Operation**

Specification	Symbol	Condition	Min.	Typ.	Max.	Unit
Receive input frequency range	Frx	-	2.132	-	2.484	GHz
Sensitivity (802.11b) 1 Mbps 2 Mbps 5.5 Mbps 11 Mbps	Srf	-	-	 -97 -93 -92 -90	-	dBm
Sensitivity (802.11g) 6 Mbps 9 Mbps 12 Mbps 18 Mbps 24 Mbps 36 Mbps 48 Mbps 54 Mbps	Srf	-	-	 -92 -92 -91 -88 -85 -82 -77 -75		dBm
Sensitivity (802.11n) MCS: 0 MCS: 1 MCS: 2 MCS: 3 MCS: 4 MCS: 5 MCS: 6 MCS: 7	Srf	20MHz Channel	-	 -92 -91 -88 -85 -82 -77 -75 -74	-	dBm
Input 1dB compression	IP1dB	Min gain	-	-	-	-
Input third intercept point	IIP3	Min gain	-	-	-	-
IQ phase error						

3.18 Typical Power Consumption

Table 3-5 shows the typical power consuption.

Table 3-5. **Wi-Fi target Power Consumption for Various Modes of Operation**

Mode	Channel Bandwidth	Target Power		
		Chip Power	PA	Total Power [mW]
Standby	Chip power down			0.015
	Host off			0.045
	Sleep			0.250
IEEE PS	DTIM = 1			3.106
	DTIM= 3			1.268
	STIM = 10			0.626
Active RX	11g	105	-	105
	HT20	105	-	105
	HT40	112	-	112
Active TX with internal EPA™+15 dBm output at the PA	11g	85	430	515
	HT20	85	470	555
	HT40	85	480	565
Active TX with internal xPA+15 dBm output at the xPA	11g	125	310	435
	HT20	125	330	455
	HT40	125	340	465
Note: HT40 is not currently defined for 2.4GHz				

4. Pin Assignments and Descriptions

This section describes the pin assignment of the AR6103. Figure 4-1 shows the PCB footprint and pin assignments (X-ray view through the chip) for AR6103.

Table 4-1 shows the pin assignments and descriptions.

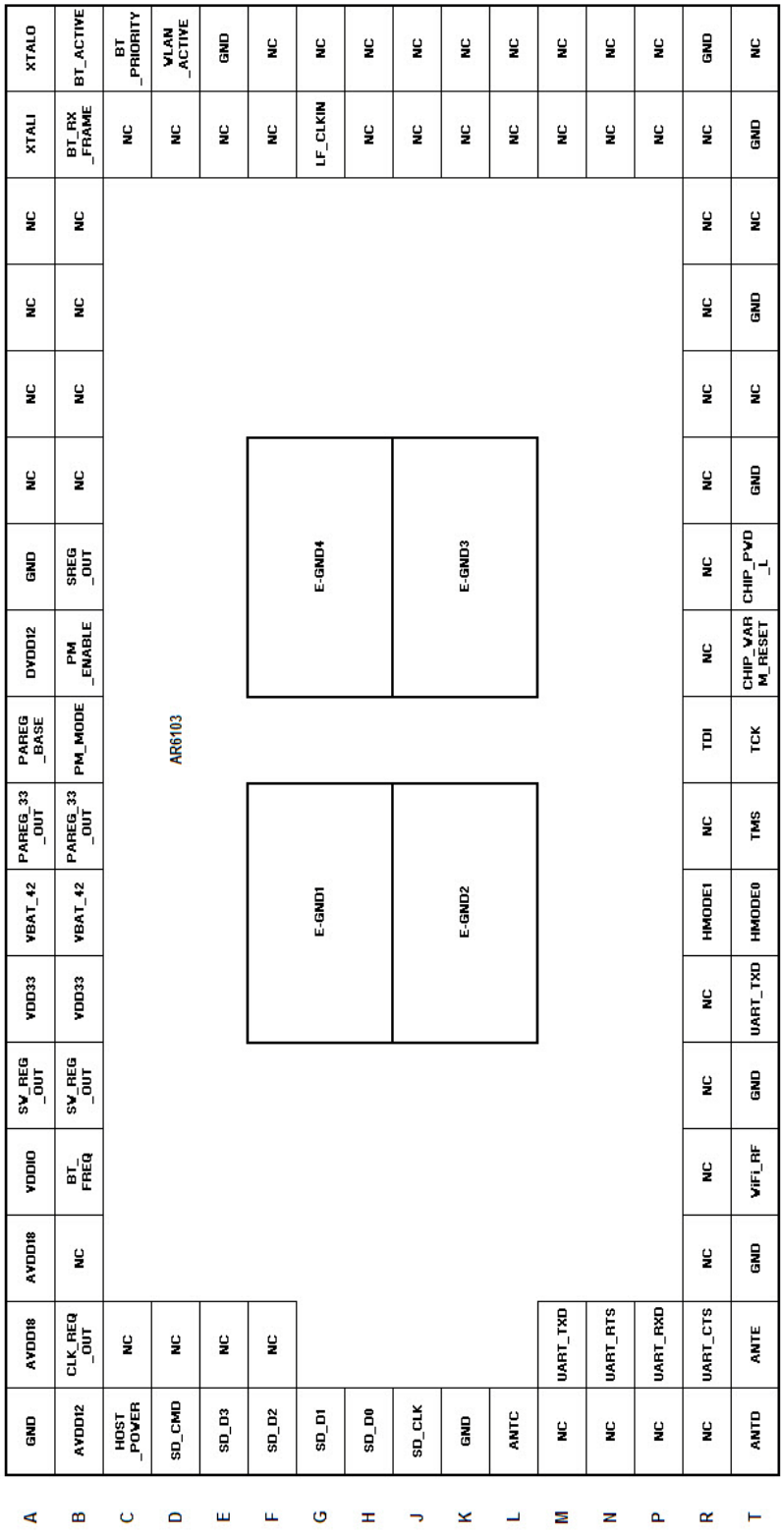

Figure 4-1. **AR6103 Pin Assignment - X-ray View Through the Chip**

Table 4-1. AR6103 Pin Assignments and Descriptions

Pin No.	Signal Name	Description
A1	GND	Ground
A10	DVDD12	Power, 1.2V digital supply
A11	GND	Ground
A12	NC	No Connect.
A13	NC	No Connect.
A14	NC	No Connect.
A15	NC	No Connect.
A16	XTALI	For external crystal or clock source
A17	XTALO	For external crystal
A2	AVDD18	Power, 1.8V analog supply
A3	AVDD18	Power, 1.8V analog supply
A4	VDDIO	Power, IO voltage reference
A5	SW_REG_OUT	Power Supply, Switching Regulator output
A6	VDD33	Power Supply, Analog, 3.3V Output (from PMU), test port
A7	VBAT_42	Power Supply, VBAT
A8	PAREG_33_OUT	Power Supply, Analog, connect to collector of power supply transistor
A9	PAREG_BASE	Power Supply, Analog, connect to base of power supply transistor
B1	AVDD12	Power, 1.3V analog supply
B10	PM_ENABLE	Control signals from BT chip for power and antenna sharing
B11	SREG_OUT	Internal SDIO regulator output, reserved for external bypass option
B12	NC	No Connect.
B13	NC	No Connect.
B14	NC	No Connect.
B15	NC	No Connect.
B16	BT_RX_FRAME	IO, Coexistence (debug)
B17	BT_ACTIVE	IO, Coexistence, 3-wire PTA, test port (debug)
B2	CLK_REQ_OUT	IO, Digital test port
B3	NC	No Connect.
B4	BT_FREQ	IO, Coexistence, 3-wire PTA, test port (debug)
B5	SW_REG_OUT	Power Supply, Siwtching Regulator Output
B6	VDD33	Power Supply, Analog, 3.3V Output (from PMU), test port
B7	VBAT_42	Power Supply, VBAT
B8	PAREG_33_OUT	Power Supply, Analog, connect to collector of power supply transistor
B9	PM_MODE	
C1	HOST_POWER	Power, 1.8V or 3.3V, Host IO (SDIO) power, depends on SDIO voltage
C2	NC	No Connect.

Table 4-1. AR6103 Pin Assignments and Descriptions

Pin No.	Signal Name	Description
C16	NC	No Connect.
C17	BT_ACTIVE	IO, Coexistence, 3-wire PTA, test port (debug)
D1	SD_CMD	IO, Digital, SDIO Command
D2	NC	No Connect.
D16	NC	No Connect.
D17	WLAN_ACTIVE	IO, Coexistence, 3-wire PTA, test port (debug)
E1	SD_D3	IO, Digital, SDIO Data 3
E2	NC	No Connect.
E16	NC	No Connect.
E17	GND	Ground
F1	SD_D2	IO, Digital, SDIO Data 2
F2	NC	No Connect.
F16	NC	No Connect.
F17	NC	No Connect.
G1	SD_D1	IO, Digital, SDIO Data 1
G16	LF_CLKIN	IO, Low Frequency (sleep) clock input
G17	NC	No Connect.
H1	SD_D0	IO, Digital, SDIO Data 0
H16	NC	No Connect.
H17	NC	No Connect.
J1	SD_CLK	IO, Digital, SDIO Clock
J16	NC	No Connect.
J17	NC	No Connect.
K1	GND	Ground
K16	NC	No Connect.
K17	NC	No Connect.
L1	ANTC	IO, Digital, Switch Control
L16	NC	No Connect.
L17	NC	No Connect.
M1	NC	No Connect.
M2	UART_TXD	AR6003 SDIO-HCI interface
M16	NC	No Connect.
M17	NC	No Connect.
N1	NC	No Connect.
N2	UART_RTS	AR6003 SDIO-HCI interface
N16	NC	No Connect.
N17	NC	No Connect.

Table 4-1. AR6103 Pin Assignments and Descriptions

Pin No.	Signal Name	Description
P1	NC	No Connect.
P2	UART_RXD	AR6003 SDIO-HCI interface
P16	NC	No Connect.
P17	NC	No Connect.
R1	NC	No Connect.
R10	NC	No Connect.
R11	NC	No Connect.
R12	NC	No Connect.
R13	NC	No Connect.
R14	NC	No Connect.
R15	NC	No Connect.
R16	NC	No Connect.
R17	GND	Ground
R2	UART_CTS	SDIO-HCI interface
R3	NC	No Connect.
R4	NC	No Connect.
R5	NC	No Connect.
R6	NC	No Connect.
R7	HMODE1	Host Select, Bit 1
R8	NC	No Connect.
R9	TDI	IO, WLAN JTAG
T1	ANTD	IO, Digital, Switch Control
T10	WAKE_ON_WLAN (CHIP_WARM_RESET)	IO, Wake-On-Wireless (if used), test port
T11	CHIP_PWD_L	IO, WLAN Power Down (0=power down, 1=WLAN awake)
T12	GND	Ground
T13	NC	No Connect
T14	GND	Ground
T15	NC	No Connect.
T16	GND	Ground
T17	NC	No Connect.
T2	ANTE	IO, Digital, Switch Control
T3	GND	Ground
T4	WiFi_RF	RF, WiFI Antenna Port
T5	GND	Ground
T6	DEBUG_UART_TXD	IO, UART (debug)
T7	HMODE0	Host Select, Bit 0 (11=SDIO, 01=SDIO)
T8	TMS	IO, WLAN JTAG

Table 4-1. AR6103 Pin Assignments and Descriptions

Pin No.	Signal Name	Description
T9	TCK	IO, WLAN JTAG
	E-GND1	Ground
	E-GND2	Ground
	E-GND3	Ground
	E-GND4	Ground

5. Package Dimensions

Figure 5-1 through Figure 5-2 show the AR6103 pacakge dimension.

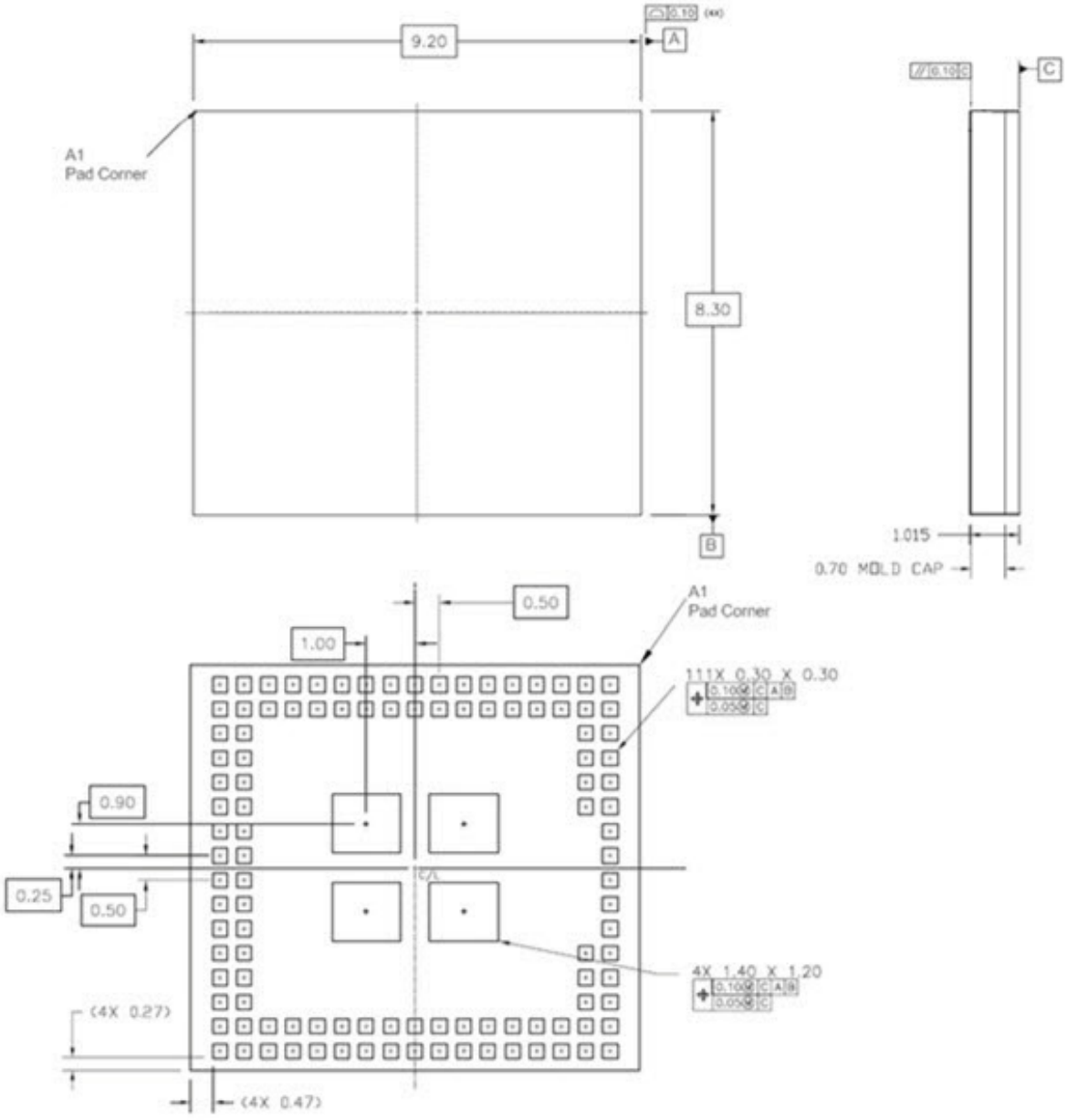

Figure 5-1. AR6103 Package Dimensions Top and Side Views

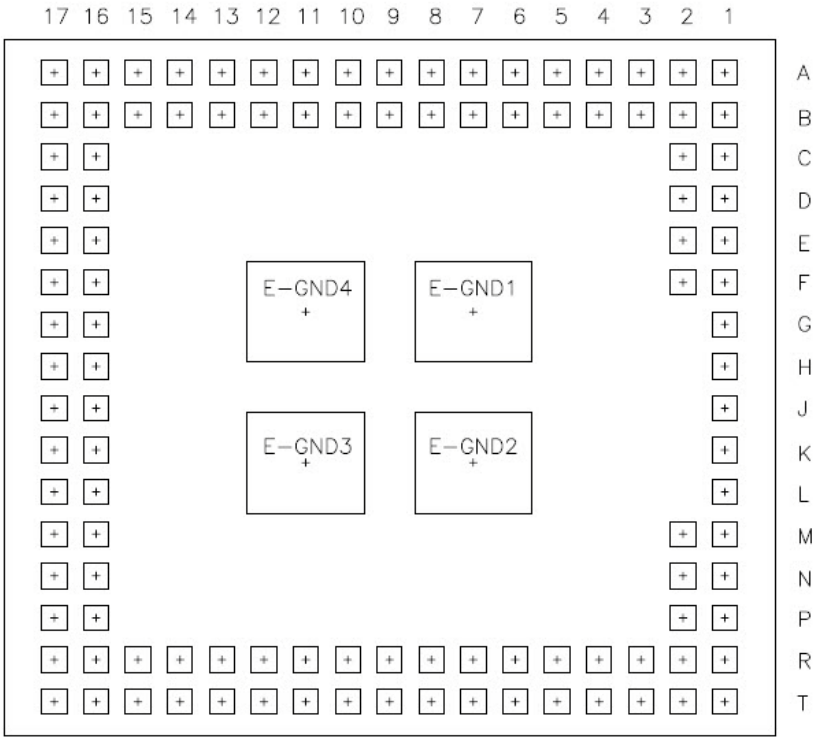

Figure 5-2. AR6103 Pin Assignments

6. Assembly Guidelines

This section describes the assembly guidelines and solder material information.

6.1 Solder Material Information

Manufacturer name: Kester

Solder past part number: EM808-Sn96.5% Ag3.0% Cu0.5% SAC305 alloy with Type 3 powder, water soluble solder paste

7. Application Schematic

This section provides the AR6103 schematic.
See Figure 7-1 for details.

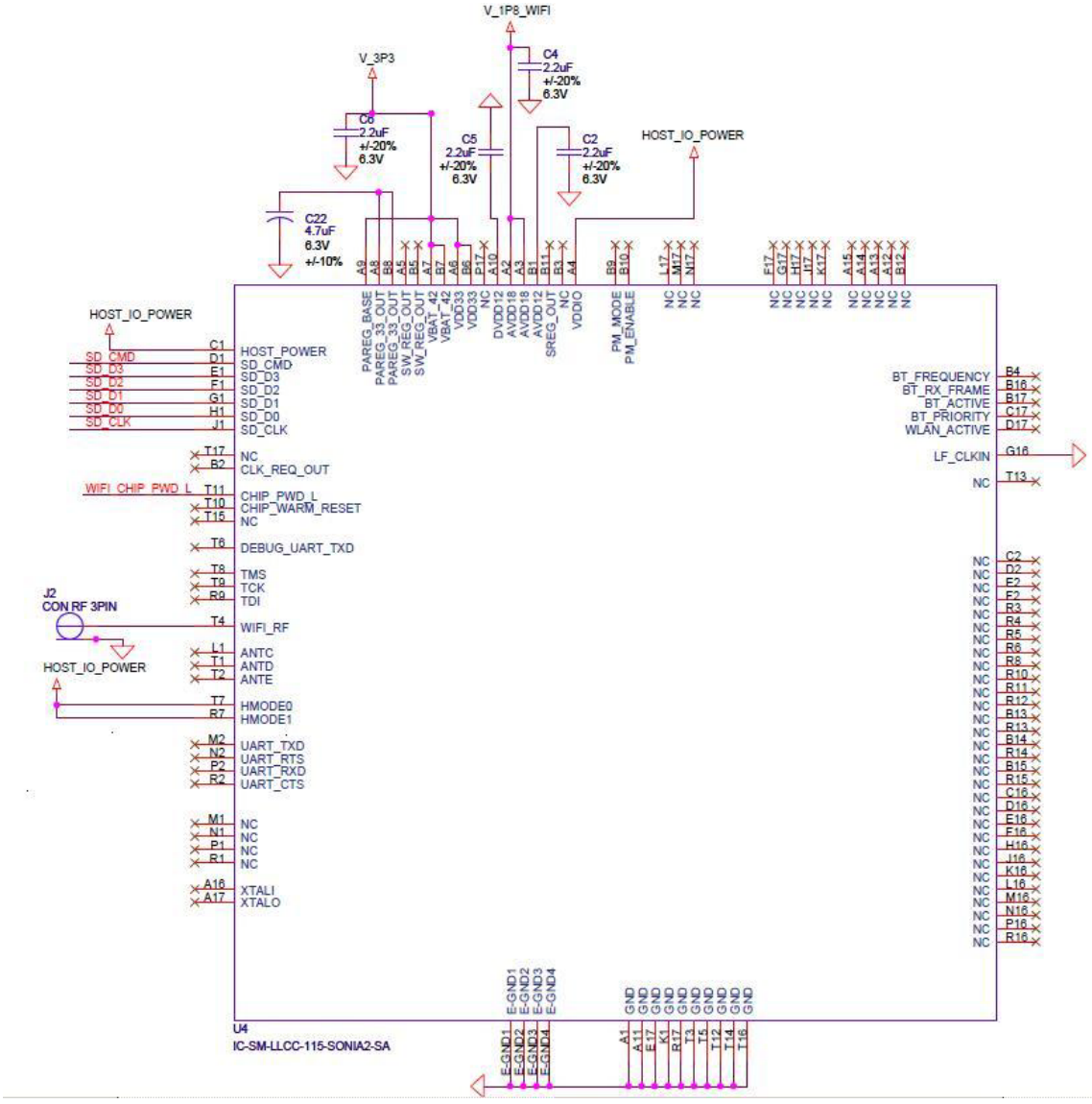

Figure 7-1. **AR6103 Reference Schematic**

8. Ordering Information

For more information on the AR6103 or other solutions from Atheros, contact your local representative:

Atheros Communications, Inc.

t +1 408.773.5200

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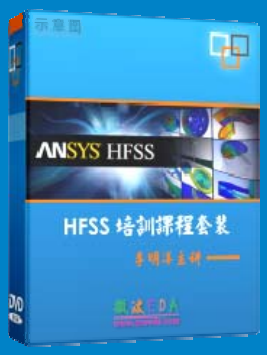

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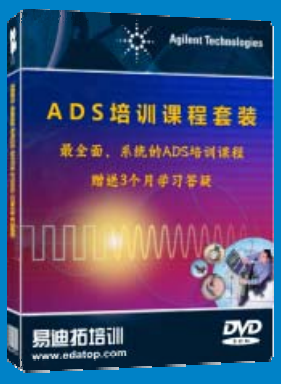

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