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Simulating and Measuring Microohms in PDNs

Jae Young Choi, Oracle
jae.young.choi@oracle.com

Istvan Novak, Oracle
istvan.novak@oracle.com

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Abstract

In high-current computing boards PDN target impedance requirement could be a fraction of a milliohm. Measuring and simulating such low impedances create challenges that require care to resolve. In simulations, special challenges include the proper choice of load and source components, the proper selection of initial conditions and solver setup. In measurements, the instrumentation setup requires a very wide dynamic range with low noise floor and very careful selection and connection of test locations and probes. The paper shows the correlation between measured and simulated self and transfer impedance profiles of large computer boards down to the micro ohm range.

Author(s) Biography

Jae Young Choi is a Hardware Engineer at Oracle America Inc. He is engaged in the design and characterization of high-speed signal interconnects and power distribution networks for high-performance server systems. He received his Ph.D. in Electrical and Computer Engineering from the Georgia Institute of Technology.

Istvan Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

1. Introduction

In modern computing and communication systems the target impedance of a power distribution network (PDN) can be as low as in the sub-milliohm range, and tends to decrease even more to meet the high power and low voltage requirement. Because even a small change of PDN impedance may cause excessive fluctuations of supply power which in turn leads to slow-down or breakdown of a system, precise assessment and control of such low impedance is a significantly important engineering practice in the PDN design process. Despite of such high importance, simulating and measuring extremely low impedance of a PDN is still very challenging.

Simulating extremely low impedance requires special consideration on various factors. For example, suboptimum choice of load and source component models can lead to accidentally misleading results, and small changes in design parameters, such as layer stack-up, metal conductivity, and via diameter and plating thickness can alter simulated impedance significantly. In addition, the selection of solver, solver setup, and simulation conditions can also be crucial factors affecting the accuracy of simulation results.

One particular aspect and potential issue with DC-drop simulation is illustrated in *Figure 1*. The screen capture shows the DC drop across a surface pad, connecting to a high-current device. For the purposes of field-solver software, (full-wave and hybrid alike), external devices are connected through nodes. The physical size of the node connection may make a difference if the current going through the node creates significant current density. Hybrid solvers may have the user-defined option to set the size of the connecting node, but it is usually a radius or diameter for a circular node connection. The left side of *Figure 1* illustrates a default-size node in a hybrid solver connecting to a large pad, which altogether carried more than 15 ampere DC current.

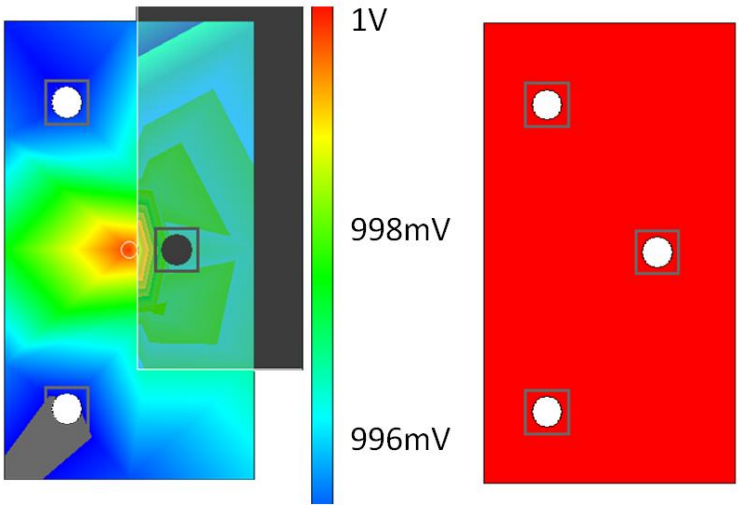

***Figure 1**. DC drop on a large surface pad with default-size node connection (left) and equipotential pad option (on the right).*

The voltage drop across the pad itself is more than 5 mV, which on a 1V supply rail amounts to 0.5% error. If the solver has an equipotential user option, and we turn it on, the DC drop across the same pad with the same current will be zero (as expected). This is illustrated on the right side of *Figure 1*. Of course in a real circuit none of these two extremes occur exactly as shown here: if we have a large pad for a component pin, the connector pin will not connect through a small circular disc area as it is assumed on the left of *Figure 1*. But it is also true that even if the component pad is exactly as big as the pad, there is still no guarantee that the surface of the pad is equipotential. However, it is reasonable to assume that the component pin of a high-current device has a low-resistance pin almost as big as the pad, which will make the pad *almost* equipotential. In summary: a large pad with a small connecting node is very pessimistic, while the equipotential pad assumption is only slightly optimistic.

Even the most accurate DC simulations may produce misleading data if the sources and loads are not set up correctly. On high-current supply rails devices, sources and loads alike, tend to have multiple connection pins. Simulation tools allow us to place sources and loads at any location on the DUT, but placing sources and loads at hundreds of pins becomes a time burden. Tools may offer help by identifying components and assigning the necessary network elements for each device in one step. The default configuration, however, is to create an equipotential area over the pins of each device, thus removing the voltage drop under the device. This can lead up to 50% miscalculation of DC drop in large dense memory arrays, while script-assisted or manual setup with individual floating sources and loads at every pin tends to produce much better correlation.

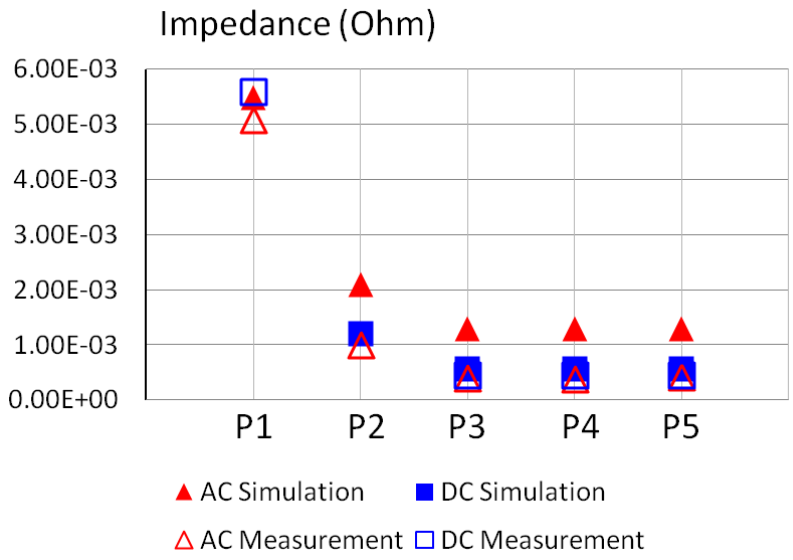

***Figure 2**. Correlation of various measured and simulated responses at low frequencies.*

The choice of simulation solver also affects the results especially at low frequencies where somewhat different physical behavior starts to come into play, such as inter plane-pair coupling caused by a larger skin-depth compared to the metal thickness. AC simulation tools may extrapolate DC values based on the AC result at low frequency, and this may produce erroneous results at the DC point. The results of AC and DC simulations and measurements are shown in Figure 2. The DUT had a construction similar to describe later in Section 3, where the construction created flat self- and transfer- impedance profiles from DC up to at least 10 kHz. AC data was the average response of the DUT around 100 Hz. P1 through P5 represent different port locations on this DUT. P1 is self-impedance and the rest are transfer-impedances. The AC simulation and measurement responses seem to show a good correlation at P1, where the impedance is several milliohms. However, the correlation – when the AC simulation is not assisted by a DC solution – starts to break down when the impedance falls below a milliohm as seen at P2 through P5.

Measuring extremely low impedance of a PDN also requires careful considerations of several aspects such as the selection of the measurement configurations, the selection of test locations, and the connection of measurement components, including probes, cables, and measurement instrument. The biggest challenges are connection discontinuity and cable braid loop error [1].

In order to illustrate and discuss the aforementioned factors in simulating and measuring low impedance in a PDN, we will present the correlation work performed on large printed circuit boards. On one board, we shorted all capacitor pads on one particular power net with wires and flat conductors matching the footprint of each particular capacitor case size, but left the multi-phase DC-DC converter output pads open. In a complementary manner, we left the capacitor pads open but shorted the converter output pads on an identical board thereby making the second board providing different current paths and different impedances for the correlation. With this set of example structures the self and transfer impedance ranges were established, within which we can confidently simulate and measure the power distribution network impedance with the selected tools. Lastly the same boards were built up with various combinations of capacitors, and again, were measured and simulated.

The boards were also cross sectioned, and the simulation results were re-created based on the cross-section data. The new simulations include typical, best, and worst case impedance responses resulting from the manufacturing variations. With these simulation data, we can show how well the simulation data correlate with the measurement and consequently close the correlation and validation loop.

The rest of this paper is organized as follows: Next section describes the device under test (DUT), and the simulation and measurement setup. Section 3 covers the DC simulation and measurement using one of the DUTs. Section 4 presents the setup and the results of the AC simulation and measurement of the DUTs including the board with mounted capacitors. Finally, Section 5 concludes the paper.

2. DUT, Simulation and Measurement Setup

2.1. DUT

To study how to simulate and measure extremely low impedance, we chose a power supply rail of a large printed circuit board where large metal planes provide very low impedance. A very similar DUT is also described in [7]. An approximate top view of the board is shown in *Figure 3* where memory banks, DC-DC converters, and port locations are indicated as well. Note that, for simplicity, even-number ports are omitted in the figure as they are right next to odd-number ports. These port pairs with probe connections on the top side of the board allow us to implement the Two-Port Shunt-through impedance measurement scheme [4].

To make the problem simple we used a bare board without any attached component. Instead of attaching actual capacitors, first we shorted the capacitor pads with wires and metal braids. Shorting hundreds of capacitor pads leads to the impedance of the power rail to become very low. Although our intention was to create such a low-impedance DUT, some of the transfer impedances were actually too low to be correctly measured.

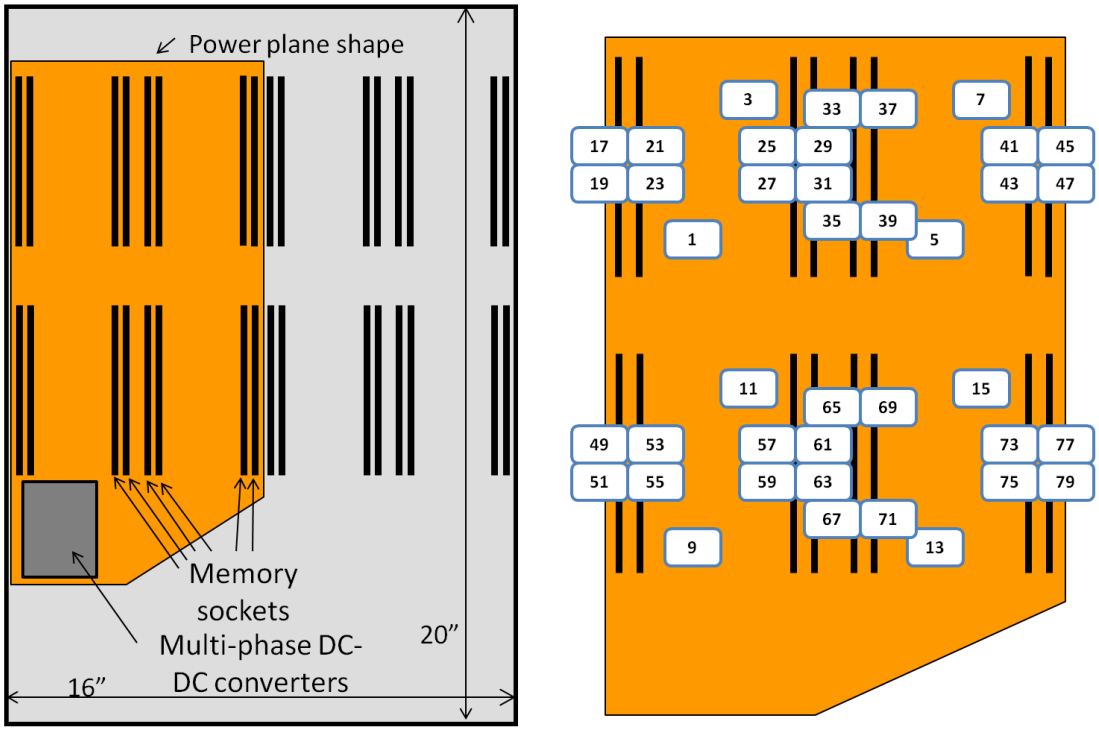

Figure 3. *Sketch outline of a large printed circuit board with multiple memory sockets. The left side shows the approximate dimensions and placements, the right side shows the port-numbering definition.*

Figure 4 shows two of such transfer-impedance traces together with the noise floor of the setup. The noise floor is a measured response with the same measurement setup, cables

and probes that were used to measure the DUT, except the probes touched the opposite sides of a solid metal sheet.

To allow more correlation points in the sub-milliohm range, we had to create another DUT which provides an impedance profile higher than the measurement noise floor but still as sufficiently low as a sub-milliohm range. It was possible to slightly raise the impedance of the DUT by shorting the pads of the multi-phase DC-DC converters while leaving the capacitor pads open.

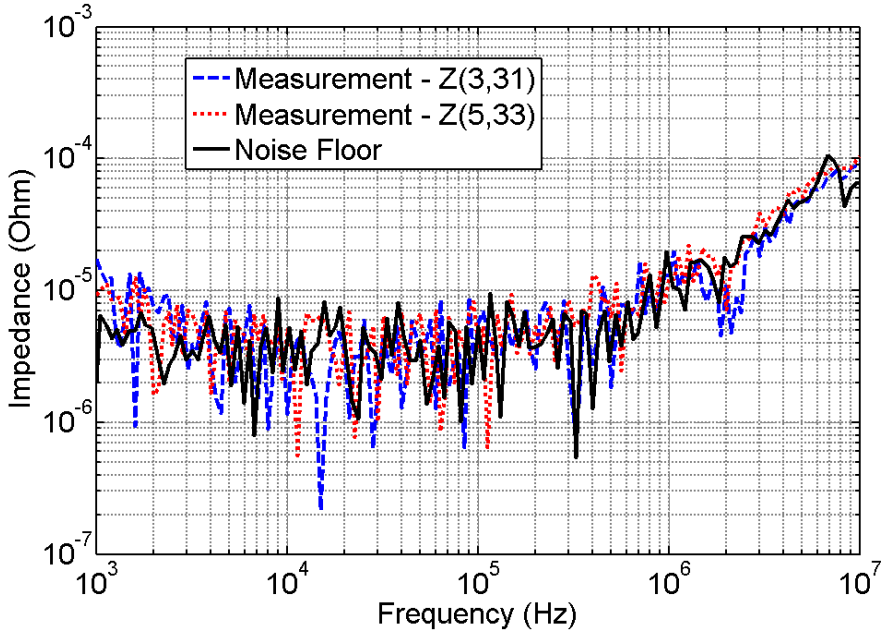

Figure 4. *Noise floor of the measurement system with two transfer impedances not being recognizably above the noise floor.*

2.2. Measurement Setup

Measuring impedance at a DC operating point and at frequencies above zero require different measurement instruments, techniques and configurations. DC measurement can be made simply by sending a direct current between two points and measure the resulting voltage drop with a voltmeter.

The components used in our DC measurements are two coaxial cables, two probes with spring-loaded ground pins, a current source generator, and a sensitive voltmeter. Their connectivity is shown in *Figure 5*. If the source current is 1A, the measured voltage becomes simply the self or transfer resistance between the two ports which can be explained by Ohm's law (R=V/I.) Many coaxial cables can easily carry 1A DC current, and digital multimeters with 10 microvolt resolution are readily available. With this simple instrumentation we can achieve 10 microohm resolution floor. The coaxial cables

and probes allow for quick positioning of probes and change of connection points. Semirigid probes with rigid center pins and spring-loaded ground pins are convenient for landing on flat PCB pads. The photo on the right of *Figure 5* shows a home-made semirigid coaxial probe with spring-loaded ground pin in a 3D probe holder. The semirigid coaxial cable has 0.084" diameter; the spring-loaded ground pin comes from a standard oscilloscope probe accessory kit.

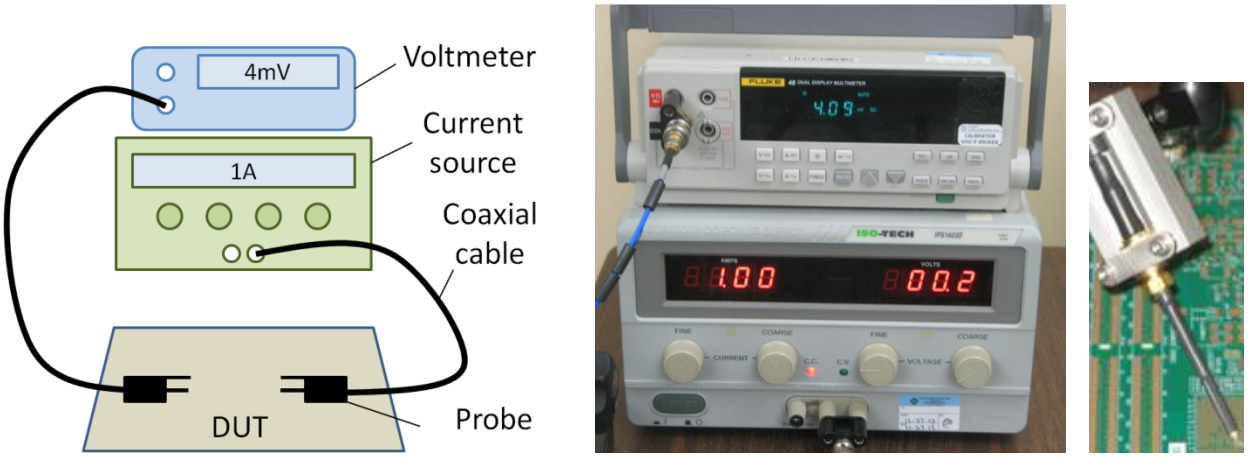

Figure 5. *DC measurement setup sketch on the left, photo of actual instrumentation in the middle, home-made semirigid probe in 3D holder on the right.*

Probes with two rigid pins are better suited for connecting to through holes with matching dimensions or to soft compliant surfaces. If better sensitivity is needed, either higher DC source current can be applied, possibly through heavier wires and directly soldered to the DUT or a more sensitive DC voltmeter can be used.

Impedance measurement at non-zero frequencies on the other hand can be made by various measurement setup, but it also requires more careful considerations on the cabling, probing and connections. From a number of available impedance measurement methods [2], we chose to use the two-port shunt-through network analyzer method. Since the impedance of a PDN is very low, using a one-port measurement may suffer from the parasitic impedance coming from the connection point between the measurement system and the DUT. Moreover, the port that only receives the measured data provides the sufficiently low error floor, enabling making measurements of extremely low impedance [3], [4].

The instrument described in [5] has two options to measure low impedances: the Gain-Phase setup side of the instrument, working up to 30 MHz, has semi-floating ground connections and its cable-braid error floor is typically in the tens of microohms range. The S-parameter side, shown in *Figure 6*, has regular grounded VNA connections and it works in the 5 Hz to 3 GHz frequency range.

Figure 6. *AC measurement setup with regular two-port VNA and ferrite toroid common-mode choke.*

The size of the DUT required a few feet of cables, which would have created a low-frequency cable-braid error floor of about 30 milliohms. To reduce this error, and at the same time keeping the benefits of the wide-band VNA ports, approximately six feet of RG178 coaxial cable was wound on a large ferrite toroid core. With the good dynamic range of the instrument, this common-mode choke can guarantee less than 10 microohm impedance error floor above 1 kHz (see *Figure 4*).

2.3. Simulation Setup

In this study, we have used a commercial simulation tool, which is described as a hybrid solver [6]. It decomposes a given problem into separate domains where different types of solvers will be used. Then, it calculates the field in each problem domain using a corresponding field solver. The tool finally extracts frequency-dependent network parameters.

Like most of the electromagnetic simulation tools do, the simulation tool used in this paper requires its users a careful consideration on the simulation setup to ensure that the tool generates accurate results. The tool also comes with many options available that may affect the result significantly. For example, a special option that engages a DC simulator in the middle of the AC simulation process enables calculating the IR drop response using a dedicated DC solver. Subsequently, the resulting AC and DC results are merged to generate low frequency responses.

Stack-ups and pad-stacks also need to be carefully checked when the tool has finished importing the layout file, as certain data may have been neglected or altered during the process. Also, updating geometric dimensions and material properties to the most realistic ones is a good practice to create well simulation data that correlates well with

measurements, because a small change of those parameters may affect the simulation results significantly, especially in very low impedance PDNs.

The setup for the most of simulations used in this paper is as follows:

- Adaptive frequency sweep for 0 Hz – 100 MHz
- Calculate DC point as reference
- Natural boundary condition considering boundary radiation
- Ignore inter-plane coupling
- Apply up-to-date cross-section information of the board to the stack-up and pad-stack

3. DC Simulations and Measurements

As explained in 2.1, we shorted the multi-phase DC-DC converter pads of the board shown in *Figure 3* using short wires and metal braids while leaving the capacitor pads open to slightly raise the impedance of the above the noise floor.

We used two types of solvers to generate DC point results. One is an AC solver that generated a result at its lowest-possible frequency and extrapolated that to the DC point. The other is a DC solver which actually calculated IR drops at DC using a DC-specific solving technique.

After all the planned measurements were performed, we cross sectioned the board to obtain actual geometric dimensions, such as a via drill hole size and plating thickness, metal and dielectric thickness.

(Unit: mil)

Layer	Layout	Board 1	Board 2
Power1	1.20	1.24	1.23
	4.24	4.01	4.04
Power2	1.20	1.24	1.24
	1.00	0.97	0.96
Power3	1.20	1.23	1.23
	4.24	4.11	4.13
Power4	1.20	1.23	1.22
	1.00	0.96	0.96

Figure 7*. Vertical geometry data from the layout tool (labeled 'layout') and cross-section data of the two DUT boards*

Figure 7 shows the stack-up dimensions of the original board design and the ones obtained from the actual board cross sections. The table shows part of the stack-up, the internal portion where four metal layers were used for high-current power and ground connections. The rows with no layer name indicate the dielectric layers between the copper layers. The variation of via diameter and plating thickness was from 11.8 to 12.3 mil and from 1.1 to 1.6 mil, respectively. Using the cross section data we categorized each geometric dimension to three cases; typical, best, and worst. The typical case simply represents the mean value of the measured dimensions. The best and worst cases were selected as potential upper bounds: the highest and lowest thickness values were uniformly applied across all similar geometry items. Those combinations were selected, which would potentially result in the lowest and highest impedance, respectively. Therefore, the best and the worst cases can set the upper and lower boundaries of the impedance caused by manufacturing uncertainty.

3.1. DC Correlation

The self-impedance results of the AC simulations as well as low-frequency VNA and DC measurements are shown in *Figure 8*. Three simulations are created using the typical, best, and worst cross section data. Both the VNA and DC measurement results are within the corner cases, the best and the worst.

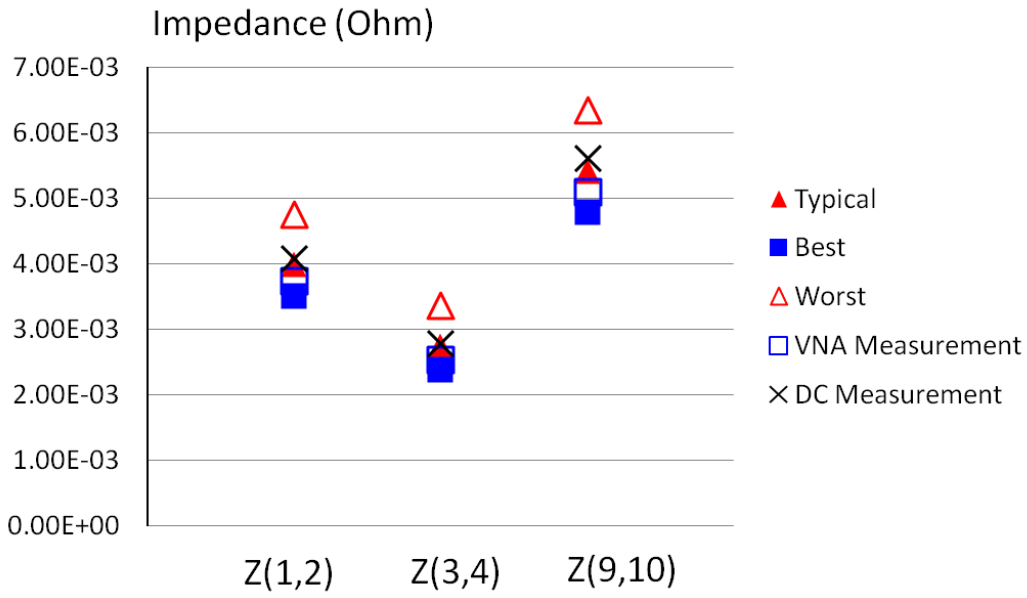

Figure 8. *Typical, best, and worst case self-impedance results of simulation closely correlate with low-frequency VNA and DC measurements.*

Figure 9 shows transfer impedance results. The transfer impedances are lower than the self impedances and two of them (Z(1,17) and Z(51,73)) are below 1 mOhm. The DC and VNA measurement results of port 51 and 73 correspond to each other at 0.45 mOhm, and

they are within the simulation corner cases. Other transfer impedance results also show that the VNA measurements and the simulation results are with a good correlation.

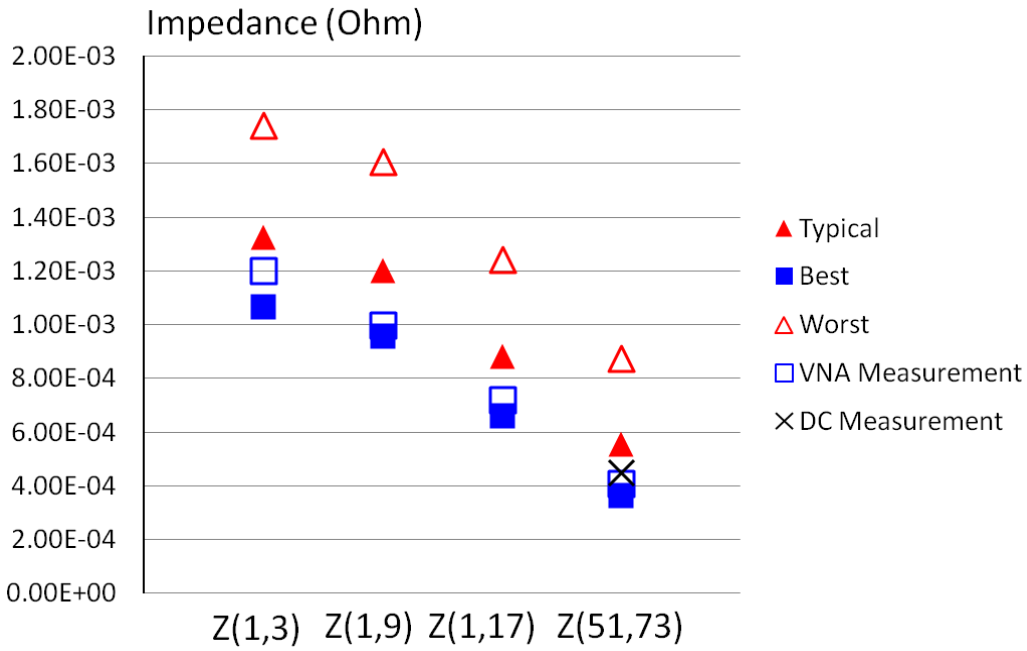

Figure 9*. Transfer-impedance simulation and measurement results of typical, best, and worst case at 1mOhm and below.*

4. AC Simulations and Measurements

4.1. Shorts at DC-DC Converters

The DUT in this section is the board with the shorted DC-DC converter pads, which was also used for the DC simulations and measurements presented in Section 3.

Since our focus is on the low frequency response of the DUT, we measured and simulated from 100 Hz to 10 MHz. In the measurement setup, we used two coaxial cables covered by multiple ferrite beads to reduce the measurement error caused by ground loop. In addition, one of the cables was connected to a coaxial cable wrapped around a large ferrite toroid core to further reduce the measurement error at low frequency as shown in *Figure 6*. Probes used in the measurements have spring-loaded ground pins which enable proper contact of the probe pins to the board pads.

The simulation included the wires and metal braids shorting the converter pads, and each short is represented by a series connection of a 1 mOhm resistor and 1 nH inductor. The DC reference option was enabled so that the tool actually calculates the DC point using a DC-dedicated solver. In order to apply the effect of manufacturing variations, the

dimensions and material properties have been modified to the typical values based on the cross-section data.

Figure 10 shows the self-impedance results from the AC simulation with the DC reference option, as well as the measurement. The impedance ranges from 2.5 mOhm to 5 mOhm and the simulation and measurement curves correlate well.

Since our interest is in the sub-milliohm range, we need to look at transfer-impedances as they provide lower impedance than self-impedance. We made measurements of four transfer-impedances, Z(1,3), Z(1,9), Z(1,17), and Z(51,73). Port1 and port3 are geometrically closest to each other, whereas port51 and port73 are the farthest apart, and therefore expected to have lower transfer-impedance. *Figure 11* shows all the measured transfer-impedances together with simulation results, and most of the impedances are in the sub-milliohm range. The lowest impedance is observed from Z(51,73) as expected, and the values from the simulation and measurement correlate at 0.55 mOhm and 0.40 mOhm, respectively.

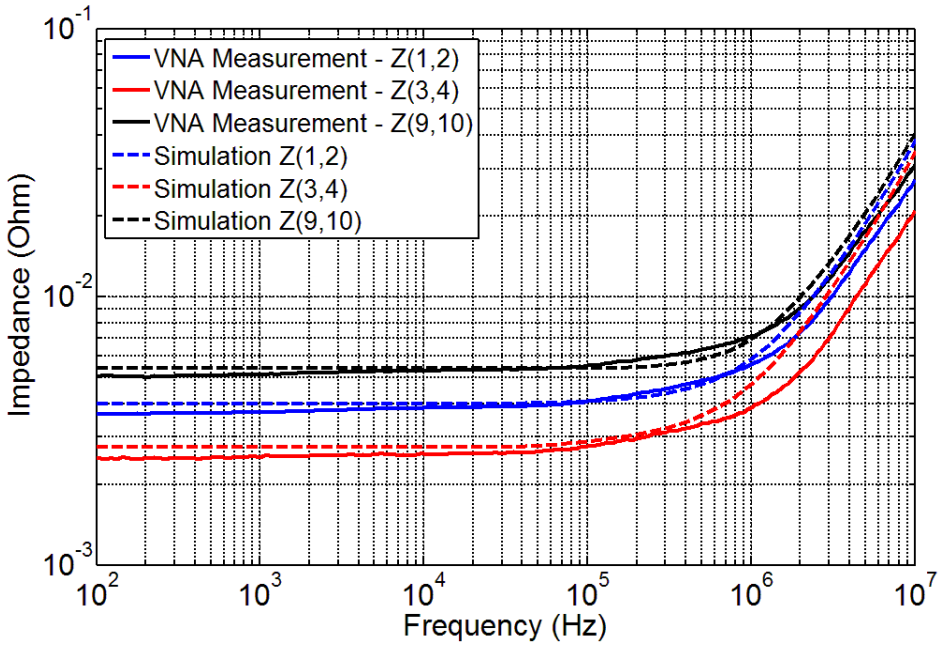

Figure 10. *Self-impedance results of measurements and simulations of the board with shorted DC-DC converter pads*

The simulation results in *Figure 11* were based on the typical dimensions and material properties that we obtained from the cross-sectioning. In order to assess and quantify how the manufacturing uncertainties eventually affect the resultant impedance, we also simulated two corner cases from *Figure 7* data, the best and the worst, representing the minimum and maximum impedance boundaries, respectively. *Figure 12* shows measurement data compared to the simulation results of two select port combinations, Z(1,3) (left) and Z(51,73) (right). In both cases, the measured response stays within the

impedance boundary set by the simulation corner cases along the frequency range. Notice that the shape of the curves is very similar to each other in the entire frequency range.

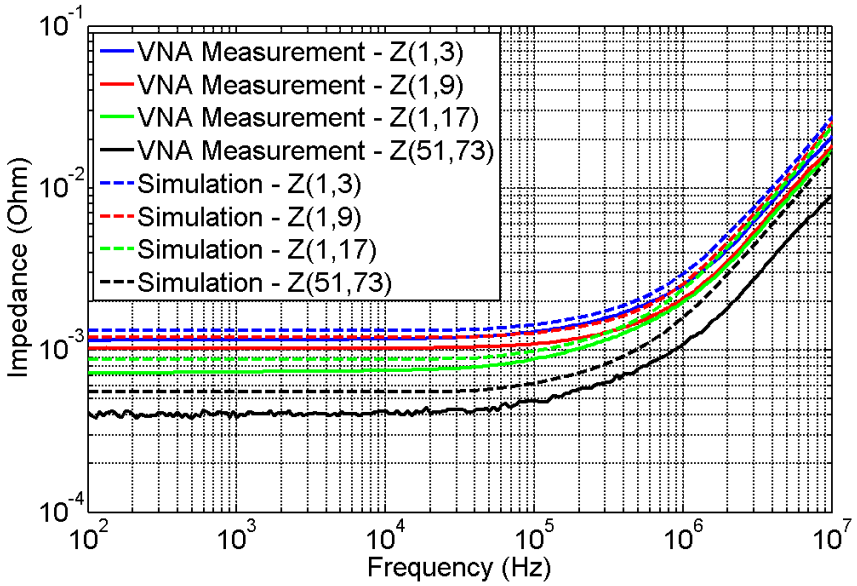

Figure 11*. Transfer-impedances from measurements and simulations of the board with shorted DC-DC converter pads*

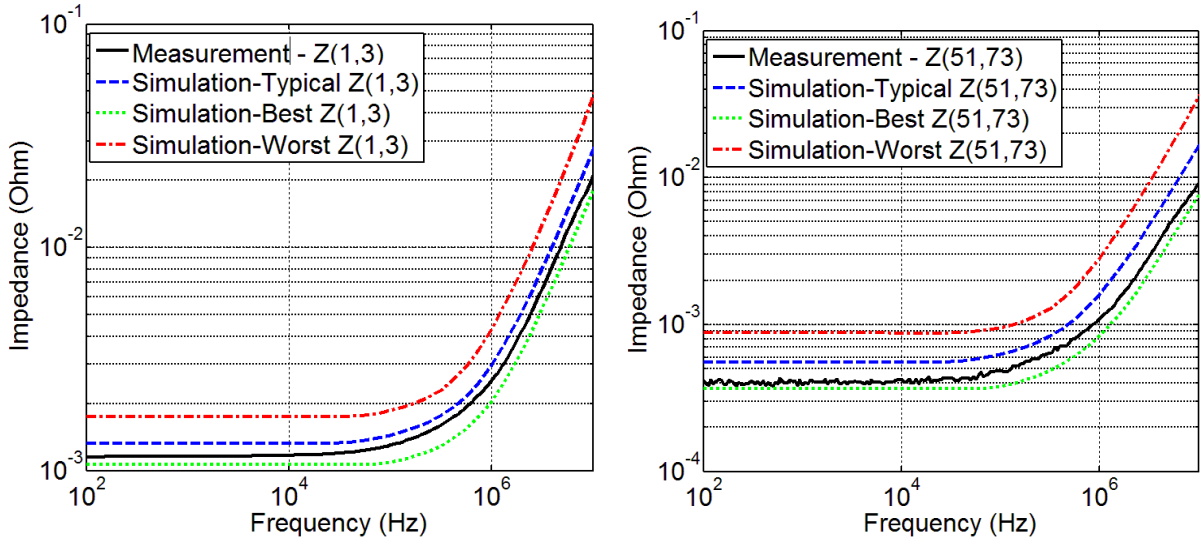

Figure 12*. Measurement result compared to simulation results with cross-section data.*

4.2. Shorts at capacitors

The DUT shown in this section is the board with shorts at the capacitor sites. Shorting hundreds of the power and ground pads of capacitors makes the DUT impedance extremely low.

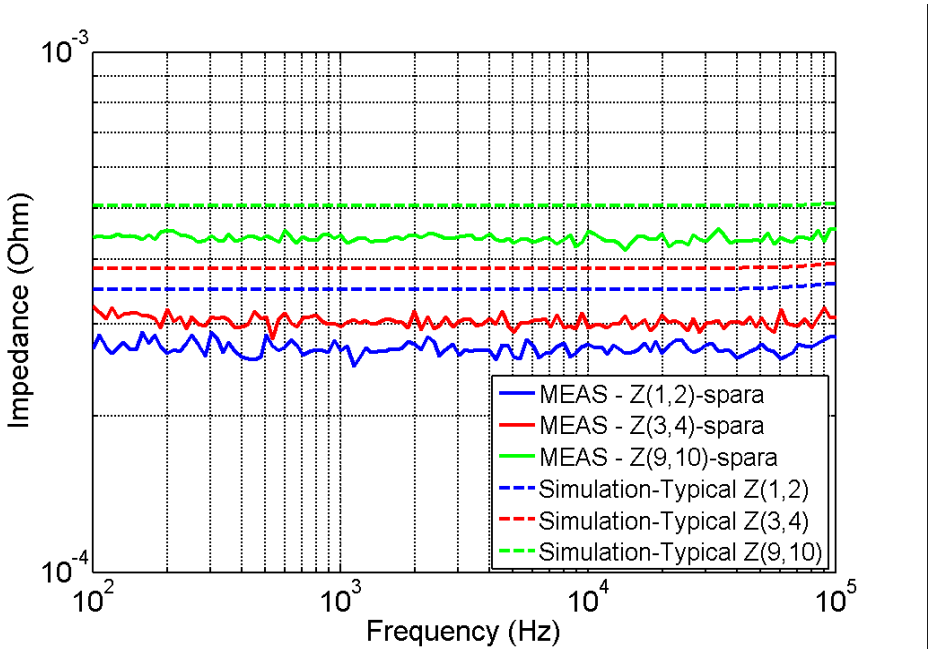

***Figure 13**. Measured and simulated self-impedance of the board with shorts at capacitors*

Figure 13 shows three self-impedances curves generated by simulations and VNA measurements, and they have a good impedance correlation in the microohm range. As described in Section 2, some of the transfer impedance combinations are below the noise floor and could not be correctly measured. Note that the layout dimensions and material properties used in the simulation were based on the typical values of the cross section data.

4.3. Board with Capacitors

The board used in this paper has hundreds of capacitor locations where three types of capacitors can be placed. We selected 12 pieces of 1000uF polymer tantalum capacitors and 40 pieces of 0805-size 47uF multi-layer ceramic capacitors and mounted them on the board and made multiple combinations of self and transfer impedance measurements and simulations. To add the capacitors in the simulation, we measured each capacitor and attached the measured data into the simulation. Since the test fixture used for the capacitor measurements was initially included in the capacitor models, it was separately measured by shorting its surface pads and subtracted the resulting impedance from the

capacitor model. *Figure 13* shows the measurement and de-embedded results for the 1000 uF (left) and 47 uF (right) capacitors. The dashed blue traces represent the impedance of the shorted test fixture. From the de-embedded capacitor impedance-frequency curve separate .s1p Touchstone model files were created for each capacitor.

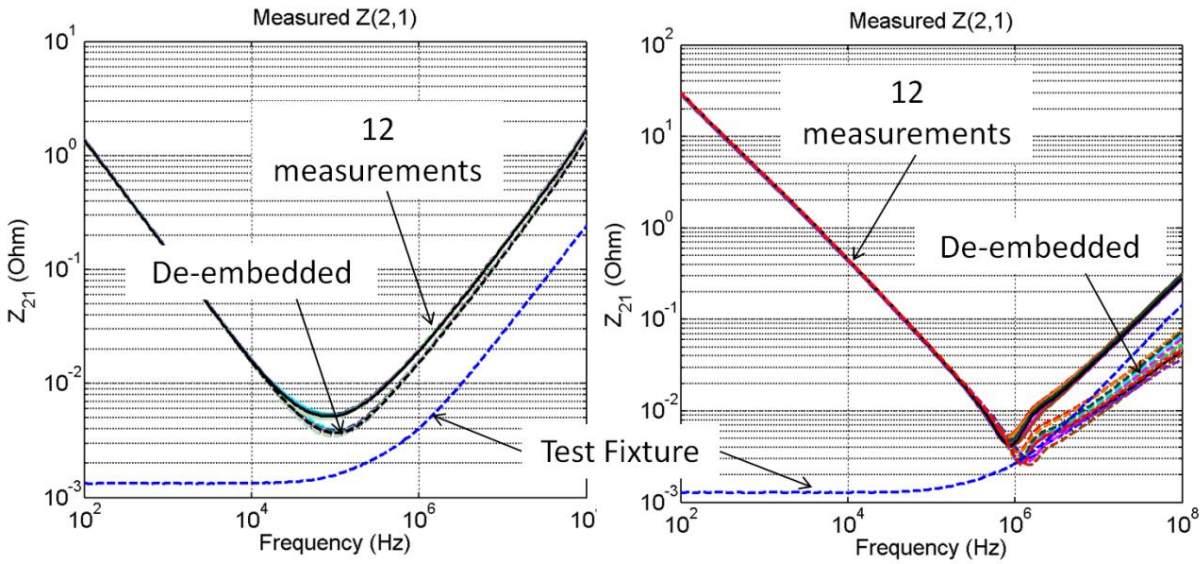

Figure 13. *Measured impedance of 12 capacitors and test fixture together with de-embedded models.1000uF (left) and 47uF (right) capacitors.*

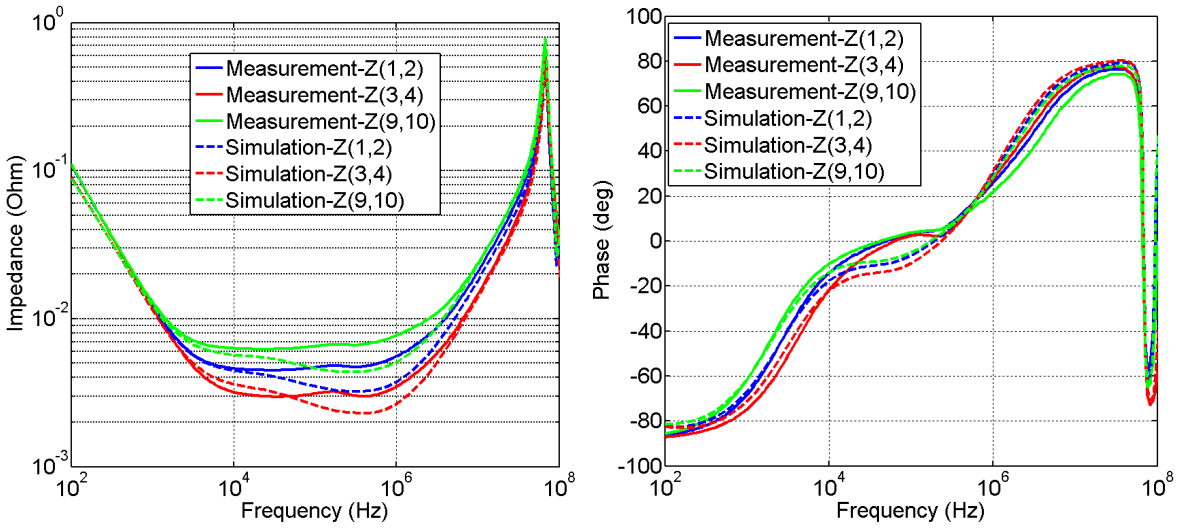

Figure 14. *Self-impedances from simulations and measurements of the capacitor loaded DUT.*

The simulation and measurement results of the board with 52 pieces of the two types of capacitors are plotted in *Figure 14* and *Figure 15*. The correlation used passive components only; no DC-DC converter was included as those usually have higher variability and therefore are not well suited for correlating measurement and simulation processes. For measured impedances on a similar board with active DC-DC converters running, see for instance [7], [9], [10] and [11].

The self impedances were simulated and measured at the power-ground pad pairs of various devices. In the memory area the opposite pads in the socket footprints were used, which connect with shared vias to the internal planes. As a result, the self-impedance values of *Figure 14* contain a short section of the corresponding via loop, raising the impedance to a few milliohms, where correlation to simulated values is easier. The same series vias do not noticeably alter transfer-impedance values and therefore impedances in *Figure 15* are sub-milliohm values.

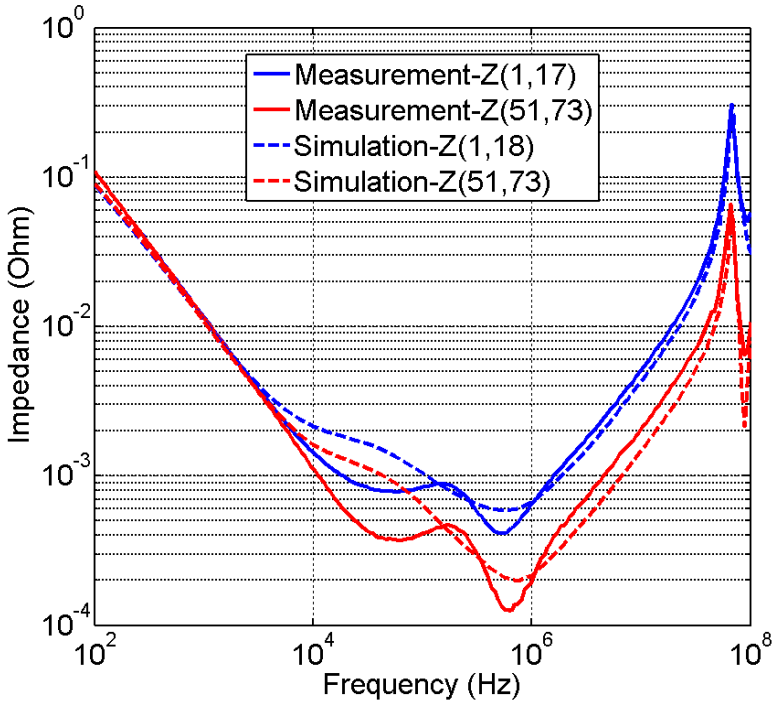

Figure 15. *Transfer-impedances from simulations and measurements of the capacitor loaded DUT.*

The correlation of the DUT with capacitors shows the simulation and measurement resulted in similar trend and curve shape, such as the frequency points where the local and global minima of the impedances are observed. However, the impedances at such frequencies show somewhat noticeable disagreement. The reason for the discrepancy may resulted from either single or multiple sources, such as an imperfect technique of applying a capacitor model to the simulation tool, improper simulation setup, or the bad condition of the capacitor model applied to the simulation.

5. Conclusions

We have presented the correlation of simulations and measurements performed on low-impedance PDN on a large memory array with different component configurations: shorts at capacitor sites, shorts at DC-DC converter outputs and with a selected sub-set of polymer bulk and ceramic capacitors. Challenges of simulating extremely low impedance include the choice of simulation solver, simulation setup, and the application of manufacturing variation. It was shown that simulation settings and setup parameters can significantly alter the results. It was also illustrated that AC simulation results from hybrid solvers can produce reasonably accurate results in the milliohm range, but require DC-solution assist in the sub-milliohm range. Measuring of microohm impedance values requires careful consideration of the choice of measurement method, configuration, and setup. Recent instrumentation advances make it possible to achieve a low-frequency noise floor of ten microohms or less with conventional two-port VNA shunt-through connection with a series common-mode choke.

Using a hybrid field solver and a two-port network analyzer measurement method, we have shown good correlation of impedance between simulations and measurements in the sub-milliohm range. Further improvement of the low-impedance analysis requires the correlation effort in simulating and measuring more realistic and complex devices such as a DUT with live active components.

Acknowledgement

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