Chapter 5

A Power Distribution System

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5.1 Introduction

The goal of a power distribution system is to have an impedence that is flat over frequency. This goal may or may not be achievable depending on the system requirements. In a case where flatness cannot be achieved, the design will exhibit some pseudo-parallel resonance. The magnitude of the parallel impedance will have to be determined to make sure that the voltage drop, as seen by the load, does not exceed expectations.

5.2 An Example of a Power Distribution Design System

The input parameters for the example are shown in *Table 5.1*.

Description	Min	Nom	Max
Power Supply Voltage	1.400	1.500	1.600
Power Supply Transient Response		10.6 µs	
Load Current Static		10 Amps	
Load Current Dynamic		10 Amps	
Load Switching Frequency		533 MHz	
Pk – Pk Ripple Voltage on Chip		100 mV	
On Die Capacitance (parasitic est.)		40 nF	

Table 5.1: *Input Parameters for Design Example*

5.3 The Problem Schematic

The schematic in *Figure 5.1* covers a five-stage system with three stages on the board low-inductance capacitator arrays (LICAs) that

may be placed within the package and additional on-die capacitance that may be required. The schematic also indicates several series R and L components placed in series with each capacitor bank. The value of each component cannot be determined until the spacing between the components can be determined. The package inductance and resistance must be determined first because their values significantly affect the design of the power distribution system.

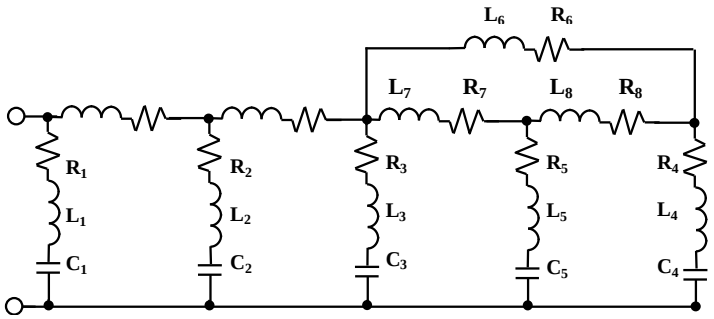

Figure 5.1: *Schematic of a Power Distribution System*

In *Figure 5.1*, R_4 represents the equivalent load within the chip. C_4 represents the amount of on-die capacitance. L_7 and R_7 represent the chip package inductance and resistance to any LICAs. L_8 and R_8 represent the inductance and resistance from the LICAs to the die itself. L_6 and R_6 represent the inductance and resistance of the board under the chip area.

R_4 has two values, the first is based on the static current and the second is based on the sum of the dynamic current and the static current. Using the nominal value of supply voltage, the two values for R_4 are 0.150 Ω, and 0.075 Ω.

The combined impedance of the board section under the chip and the package represents a series impedance to the load. Further, the combination of the equivalent inductance and resistance is a significant voltage drop at the load, R_4. If the maximum peak-to-peak voltage drop is 100 mV, then the voltage drop due to the

series resistance is the static factor. Whereas, the voltage drop due to the series inductances is the dynamic factor.

If the chip is a ball grid array or land grid array, the current in the leg represented by L_6 should be equal to the current in the leg represented by L_7 and L_8. This is of particular importance if there is a LICA capacitor represented by C_5. The proper sharing of current in each leg is assured if the current per pin of the chip is equal to the total peak current divided by the number of pins. The board inductance is then determined by the number of pins in each row of the ball grid array (BGA) or land grid array (LGA). Let us subtract the number of power pins in a row from the total current times the current per pin. The difference in current then becomes the total current seen in the next row. Let us repeat the process until the center of the chip has been reached. Moving from row to row represents a strip inductor with current flowing through it. A voltage drop is then created across the strip. Summing the individual voltage drops represents the total drop across the board. This sum when multiplied by time gives volt-seconds. Dividing the volt-seconds by the dynamic current gives the value of inductance L_6 and should also be equal to the sum of L_7 and L_8.

The package inductance is estimated to be 12 pH. The board inductance is estimated to be 8.32 pH. The combined inductance is 4.91 pH.

The package resistance is estimated at 320 μΩ, and the board resistance is estimated at 84 μΩ. The combined resistance value then becomes 67 μΩ.

5.4 The Characterization of the Load

Figure 5.2 shows the waveforms. The AC current has a 10 amp peak and a 5 amp average, making the total average of 15 amps. The difference between peak current and average current is 5 amps. The frequency is 533 MHz. Assuming a 50% duty cycle, the on-time is 938 ps, t_{on}. The on-time determines the necessary on-die capacitance as well as the maximum series inductance from the supply voltage.

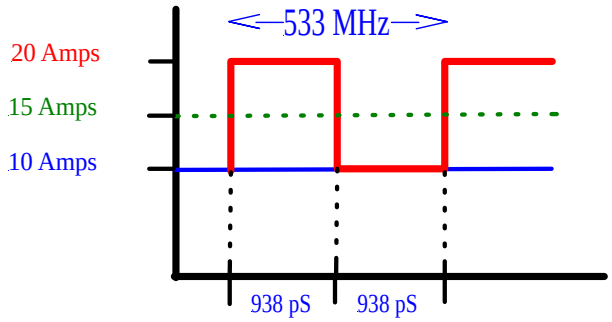

Figure 5.2: *Load Current Waveforms*

5.5 System Bandwidth

The bandwidth and the number of stages of the system should be determined first, because this will give a preview to the number of stages necessary to complete the goal. *Table 5.1* gives the loop response of the power supply as 10.6 μs and this becomes the low frequency end of the bandwidth. The on-time as given by the duty cycle of the waveform at the load provides the upper frequency range of the bandwidth. The ratio of these two frequencies gives the bandwidth ratio of the system:

$$b_{RS} = \frac{f_{HS}}{f_{LS}} = \frac{10.6\,\mu s}{938\,ps} = 11300$$

The number of stages is then estimated from $n \sim Log(b_{RS})$ by taking the log of b_{RS}.

From inspection it is somewhat larger than 4. However useful this may seem, it does not give any information about the Q of the system. Further, it may be more useful to have 3 stages or even 5 stages rather than 4.

$Q_S = \sqrt[N]{\frac{f_R}{BW}}$ can be determined from the 2 values of time currently known. The first part of the process is to determine the value of the center resonance frequency of the system as indicated by the

abbreviation f_R. The value of Q_S can then be determined. If the inversion of the value of time is used to determine the value of frequency, then the series resonant frequency, f_R, becomes 10.03 MHz.

The second part of the process is to determine the bandwidth (BW) and the difference between these two frequencies, or 1066 MHz. The Q of the system is the ratio between the center frequency and the bandwidth, resulting in a series Q of 0.0094. This value is far lower than what may be expected. The value of Q as calculated is the Q for the system. The value of Q for each stage is found by taking the nth root of the system Q. The initial estimate of 4 stages results in a value of Q for each stage of 0.311. This is very close to the ideal situation. A visual inspection of *Figure 5.3* shows four stages and a system Q of 0.0094 which are very close to the third line from top, which represents a stage Q of 0.300.

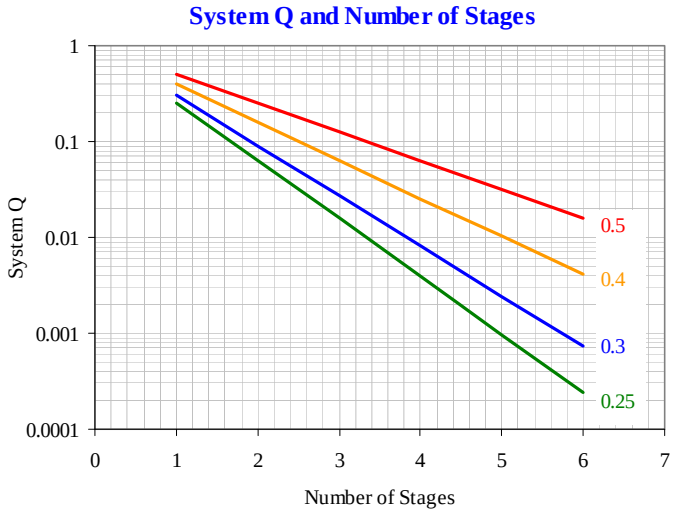

Figure 5.3: *Number of Stages Based on System Q*

Figure 5.3 also indicates that the same system Q could be accomplished by using five stages. Each stage would then have a value of Q equaling 0.400, as represented by the second line from top.

There are two solutions: the first with a lower value of Q; a system having four stages and a lower parallel resonance impedance. With only four stages, then three would be placed on the printed wire board and the fourth would be the added on-die capacitor.

The second solution requires the addition of package capacitance as represented by C_5 in *Figure 5.1*. The type of capacitor used for this purpose is the LICA. This capacitor is an expensive solution and is usually needed when the package inductance is relatively high.

5.6 Determination of the Maximum Impedance

Table 5.1 shows a maximum noise voltage of 100 mV. The maximum impedance can actually be determined from the value of this noise voltage value and the dynamic current. The dynamic current is 10 amps and thus the impedance is 0.010 Ω. The value of impedance is the value at the pseudo-parallel resonant frequencies. The limit line for all frequencies should be less than 0.010 Ω. For parallel resonance, the impedance level should not exceed the limit line. When impedance is plotted against frequency, all values of impedance should not exceed the limit line.

5.7 The Q of the System

For n stages, the series Q_S for each stage is approximated by

$$Q_S = \sqrt[N]{\frac{f_R}{BW}}$$

To keep the system stable, the value of Q_S for the system is 0.311. The bandwidth ratio has been determined as 11300. The value of f_{R4} is the switch frequency at the load and the value of f_{R1} is the loop response of the power supply. These values are 533 MHz and 47 kHz, respectively.

Given the approximate value of Q_S, 0.311 for each stage, the bandwidth for the fourth stage is based on the resonant frequency 533 MHz. For this stage, the bandwidth is 1714 MHz. The value of

f_{H4} needs to be determined and is found by dividing the resonant frequency by the series Q. Since

$f_H = \frac{f_R}{Q_S}$ and $f_L = f_R Q_S$ and bandwidth is defined as

$$B_W = f_H - f_L$$

therefore, by substituting for f_L and f_H, bandwidth is

$$B_W = \left(\frac{1 - Q_S^2}{Q_S} \right)$$

With Q_S equal to 0.311, the value of f_{H4} is 1,714, thereby making f_{L4} equal to 1,714 minus the bandwidth or 165 MHz. However, f_{L4} is the same point as f_{H3}, making this a parallel resonant point. In addition, at f_{H4}, the value of the parallel impedance and resistance is at the maximum.

Since the maximum impedance is 10 mΩ and assuming that this impedance is resistive, then the parallel resistance is the maximum value of 10 mΩ. Dividing this value by $(1 + Q_S^2)$ will give the series resistance value. The calculated value of RS then is 9.11 mΩ. The value of $X_L - X_C$, the difference in impedance at this center frequency, is equal to $Q_S \times R_S$ or 2.83 mΩ. The value of impedance Z then is equal to

$$Z = \sqrt{R_S^{\,2} + \left(Q_S R_S \right)^2}$$

In our example, using Q_S equal to 0.311, the value of R_S is 9.11 mΩ and the value of Z is 9.54 mΩ.

5.8 Capacitance and Inductance Determination

The value of f_{R4} is 533 MHz, and the value of f_{H4} is 1714 MHz. The bandwidth for this stage is found by subtracting f_{R4} from f_{H4}, 1,714 MHz – 165 MHz = 1549 MHz. Having the bandwidth, the series resonant frequency and the high frequency point, f_{H4}, all the other

points for the entire system can now be found using a value of Q_S for each stage of 0.311.

Important Points to Remember Are:

- The maximum resistance is the maximum parallel resistance, R_P.
- Divide R_P by $(1 + Q^2)$ where Q is the series Q. This is the equivalent series resistance.
- Multiply the series resistance by the series Q, this is the resistance at the series resonant frequency. Given the resonant frequency and impedance, the values of inductance L and capacitance C can now be found.

For the third stage, the value of f_{L4} is the value of f_{H4} minus the bandwidth or 165 MHz. The value of f_{L4} is also the value for f_{H3}. This duality represents the first center frequency f_{C3}, or a parallel resonance point, whose value is now 165 MHz. Having the center frequency, the value of capacitance for stage 4 and the inductance of stage 3 can now be determined. The value of R_S has already been determined and the value of capacitance required within the die can now be estimated.

Allocating the die capacitance assumes that there is a certain amount of inductance associated with it and that the series resistance is the value of R_S. The risk posed with this assumption is that the actual value of capacitance, inductance, and resistance of the on-die capacitance have been communicated from the original manufacturer. Instead of these required communications, alternate means to estimate these values can be carried out but at the peril of the user. The package designers all too often do not communicate with those who design the actual die, and then fail once again by not properly communicating with the user of the device. These parametric elements should be part of the specifications of the device, thereby eliminating unsuccessful prototype builds due to power quality problems as well as signal integrity problems.

First, let us try to estimate the die capacitance that already exists within the logic of the complementary metal oxide semiconductor (CMOS) driver or a similar transistor. This can be accomplished by

using the dynamic current and supply voltage to estimate power, where power is

$$P_C = 0.5CV^2 f$$

where P_C is the power consumption of the on-die capacitance, V is the supply rail voltage, and f is the load switching frequency. For the example being contemplated, V is 1.5 volts and f is 533 MHz. The value of P_C is determined knowing that the dynamic current is 10 amperes and the supply voltage is 1.5 volts, giving a value of P_C of 15 watts. From this knowledge, C is determined to be 25.0 nF. Although conservative, the basic assumption is that all the bits will switch state. Those that are in a "1" state, switch to a "0" state, and those that are in a "0" state, switch to a "1" state. Realistically, 25 percent to 50 percent of the bits will change state, which then indicates that the amount of capacitance due to the non-switched bits will increase by a factor of two to four times. The estimated capacitance then could be as much as 100 nF. This value of capacitance can be more than the required need of on-die capacitance. It also could be still far less than the required need of capacitance at the die.

To determine the required value of die capacitance, the use of the characteristic impedance can be determined based on the value of the required series Q.

$$Q_S R_S = \sqrt{\frac{L}{C}}$$

The value of impedance calculated is the impedance of both L and C at resonance. For R_S equal to 9.11 mΩ and Q_S equal to 0.311, the characteristic impedance becomes 2.83 mΩ. At 533 MHz, C is 106 nF and L becomes 0.845 pH. However, the value of impedance, X_C, at f_{LA} is 9.11 mΩ as required at the first parallel resonant frequency point, 165 MHz. The required on-die capacitance from a conservative point of view is far from the required value. Additional capacitance is required.

The minimum additional capacitance needed is approximately 80 nF, thus bringing the total to 105 nF. The additional capacitance should be increased by the tolerance of the device. If the capacitance increases to 100 nF, the added capacitance of 80 nF would bring the total to 180 nF. The system series *Q* needs to be maintained, therefore the quotient of *L* and *C* must remain constant; if the total capacitance is increased from 106 nF to 180 nF, then the inductance must also increase from 0.845 pH to 1.43 pH.

A particular problem presents itself at this point. The series resonant frequency will now vary based on the actual value of total capacitance on the die itself and the inductance associated with it. There are two extremes. The first is when the capacitance is a maximum value, 180 nF, and maximum inductance, 1.43 pH. This situation has a self-resonant frequency of 314 MHz. The second situation is when the total on-die capacitance is a minimum and the inductance is a minimum value. The result of this combination is 533 MHz for a self resonant frequency. The design effort should be based on the minimum valuation of the on-die capacitance and its minimum inductance.

Important Points to Remember Are:

- For design purposes, use the minimum total on-die capacitance with a minimum tolerance.
- The inductance should be determined by the system series *Q* and the switching frequency of the load.
- When it is possible to obtain information about the on-die capacitance, use those parasitic values of *L* and *C*.

Stage 3 and Stage 4 Resonance

It has been shown that in a parallel resonance circuit, the resistance factor affects the actual resonant frequency. Therefore, a modification to the presumed resonant frequency must be done to be incorporated to obtain the correct value of on-die capacitance. As illustrated in *Figure 5.4*, the impedance in both branches must be equal for resonance to occur. The conversion is shown in *Figure 5.5*.

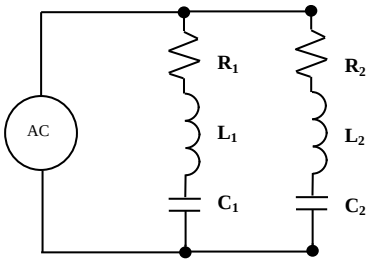

Figure 5.4: *The Two Capacitor Circuit*

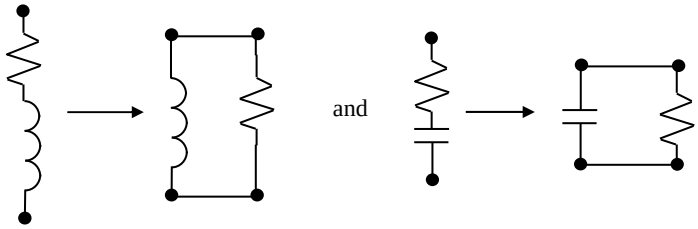

Figure 5.5: *Converting Series Components to Parallel Components*

Parallel resonance is comprised of the inductance of stage 3 together with its resistance, and the capacitance and its resistance of stage 4. Since each in their own way are series elements, each then should be converted to their parallel equivalency.

Beginning with the series inductance and resistance of stage 3 elements, the impedance is

$$Z_1 = \sqrt{(R_{S3})^2 + (X_{L3})^2}$$

and for stage 4, using the series resistance and capacitance, the impedance is

$$Z_2 = \sqrt{(R_{S4})^2 + (X_{C4})^2}$$

For the parallel equivalency, the conductance is the reciprocal of the resistance, and admittance is the reciprocal of the impedance.

$R_{S1} = Z_1 Cos\theta_1$ and $X_L = Z_1 Sin\theta_1$

therefore

$$G_1 = \frac{Z_1}{Cos\theta_1} \text{ and } Y_1 = \frac{Z_1}{Sin\theta_1}$$

In a similar fashion, for stage 4 the conductance and admittance is

$$G_2 = \frac{Z_2}{Cos\theta_2} \text{ and } Y_2 = \frac{Z_2}{Sin\theta_2}$$

Having all the conductance and admittance terms, the elements are in parallel. The circuit now appears in the *Figure 5.6*.

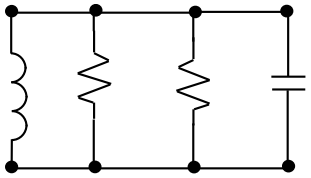

Figure 5.6: *Parallel Equivalent Circuit of the Series Elements.*

Now, since

$R_{S1} = Z_1 Cos\theta_1$ then

$$Cos\theta_1 = \frac{R_{S1}}{Z_1} \text{ and } G_1 = R_{P1} = \frac{Z_1}{Cos\theta_1} \text{ then } Cos\theta_1 = \frac{Z_1}{R_{P1}}$$

therefore

$$\frac{R_{S1}}{Z_1} = \frac{Z_1}{R_{P1}} \text{ and } R_{P1} = \frac{Z_1^2}{R_{S1}} = \frac{R_{S1}^2 + X_L^2}{R_{S1}}$$

In similar form then

$$R_{P2} = \frac{Z_2^2}{R_{S2}} = \frac{R_{S2}^2 + X_C^2}{R_{S2}}$$

However, since each parallel resistance is in parallel with each other, the equivalent resistance is the parallel equivalent of each R_P. With the two parallel resistors reduced to one resistor, the parallel value of L and C form the classical resonant circuit shown in *Figure 7*. The value of R_P cannot exceed the value of 10 mΩ in the discussed example.

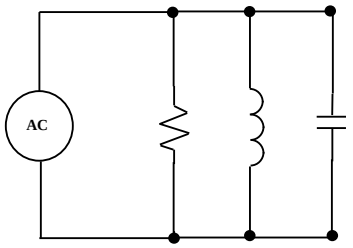

Figure 5.7: *Parallel Resonant Circuit*

The values of equivalent parallel impedances are found through the same method used to find the equivalent parallel resistance.

Therefore

$$X_{CP} = \frac{R_{S2}^2 + X_{CS}^2}{X_{CS}} \text{ and } X_{LP} = \frac{R_{S1}^2 + X_{LS}^2}{X_{LS}}$$

At the point of resonance, X_{LP} is equal to X_{CP}, therefore

$$X_{CP} = \frac{R_{S1}^2 + X_{LS}^2}{X_{LS}}$$

and determines the value of parallel capacitance at resonance. However, to find the resonant frequency, the above equation needs to be reduced to

$$\frac{\omega L_S}{\omega C_P} = R_{S1}^2 + \omega^2 L_S^2 \text{ and } 1 = \frac{R_{S1}^2 C_P}{L_S} + \omega^2 L_S C_P \text{ or}$$

$$f_R = \frac{\sqrt{1 - \frac{R_{S1}^2 C_P}{L_S}}}{2\pi\sqrt{L_S C_P}} \quad (1)$$

This equation has a special situation because, if the radical of the numerator is equal to 0, then there is no resonance.

This equation implies that if the value of Q_S is greater than 10, the actual value of the resonant frequency is found in the traditional way, by taking the square root of L_S and C_P and multiplying this result by 2 π to get the radial time. The inverse of time is the radial frequency. In designing a power distribution network, the value of Q_S is always less than 1 and greater than approximately 0.2.

In the problem being studied, the value of the series Q is 0.311, and the parallel frequency of resonance is determined by L_S and C_P which is now modified by the Equation (1). The modification to the resonant frequency is by the terms that involve Q_S, the other terms define the resonant frequency itself. The series Q terms are equal to 0.297.

5.9 Resonant Frequency Points

Figure 5.8 shows the relative series resonant points on the bottom and the parallel resonant frequencies on top. The declining slopes are the capacitive effect with its series resistance and the rising slopes represent the inductive portion and its series resistance. The upper horizontal line represents the maximum value of impedance and the lower horizontal line represents the minimum series value. The value of frequency is given in MHz. When the series Q is 0.311, then if the switching frequency of the load is 533 MHz; this represents a series resonant frequency. The first parallel resonant frequency that should occur is located at a frequency of $Q_S f_R$. This product evaluates to 165.76 MHz. The next lower series resonant frequency will occur at a frequency which is the series Q multiplied

by the previous frequency, (0.311)(165.76 MHz) or 51.55 MHz. The process continues until all four stages are defined.

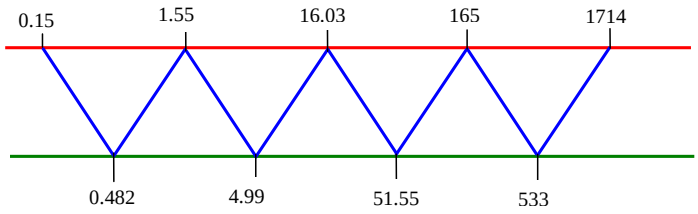

Figure 5.8: *Point-to-Point Resonant Frequencies*

Keeping with the desire to have a constant value of Q suggests that the value of series impedance should be 2.83 mΩ which is R_S times Q_S. The value of impedance of 533 MHz is the same value at 51.55 MHz, 4.99 MHz and 0.482 MHz.

The basic premise in determining the permitted values of inductance as well as the amount of capacitance needed, is based on the fact that the series Q for each stage is identical, thus the series resistance is also equal. Further, at the point of parallel resonance, the impedance of the capacitor and of the inductor is equal and opposite in sign, which when added results in 0. *Figure 5.9* shows the basic premise.

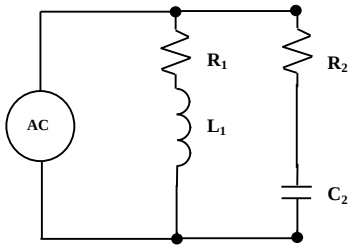

Figure 5.9: *An Equivalent Parallel Circuit*

If

$Z_1 = \sqrt{R_{S1}^2 + X_{LS}^2}$ and if $Z_2 = \sqrt{R_{S2}^2 + X_{CS}^2}$

and if $Z_1 = Z_2$ and $R_{S1} = R_{S2}$ and $X_{LS} = X_{CS}$, then it can be stated that with these equalities and with Z_1 and R_{S1} known, the value of X_{LS} and X_{CS} can be found. Thus

$$X_{CS}^2 = Z_1^2 - R_{S1}^2$$

Using the present problem, the value of X_{CS} or X_{LS} is 2.83 mΩ at each of their respective series resonant frequencies. The actual value of capacitance was determined using the fourth resonant frequency of 533 MHz, thus the value of C is 106 nF. This basically answers the question of how much on-die capacitance is required. If a conservative approach is used, then with 25 nF already present, 81 nF will need to be added on the die. If only 30 percent of the bits are switched, then the total capacitance seen will be 187 nF. The value of the series inductance L_S is found at the third resonant frequency of 51.55 MHz, and has a value of 8.74 pH.

Using this very same method for the other series resonant points, yields values of capacitance of 1.1 μF, 11.33 μF and 117 μF. The inductance for each series point is found in the same way, that is, the impedance is 2.83 mΩ at the points of series resonance. Therefore, these inductances are 8.74 pH, 90.4 pH, 934 pH, and 9659 pH. These values not only represent the equivalent series inductance of each capacitor stage but also any board inductances such as vias and planes, interposers, package inductance and other inductances that may be encountered along the way to the load.

5.10 Number of Capacitors

The next task is to select the package style for each stage. Starting with stage 3, the value of capacitance is 1.1 μF and the value of inductance is 8.74 pH. To obtain the value of inductance, the choice is between 0612 capacitors or 0306 capacitors. Both of these are sideways capacitors and have inductance values of 550 pH or 320 pH. To obtain the required inductance for the 0612 capacitor package, 63 capacitors will be needed; for the 0306 capacitor package, 37 capacitors will be needed. The value of capacitance for the 0612 capacitor package is 0.018 μF and for the 0306 capacitor package is 0.033 μF. The choice of package type can be easily

determined from this data because there are no 0612 capacitors that are that low in value, therefore the 0306 device of 0.033 μF will be used.

Similarly for stage 2, the value of capacitance is 11.33 μF and the value of inductance is 90 pH. There are 2 choices for package types, 1210 capacitors which have an inductance value of 1000 pH and 0612 capacitors which have a value of inductance of 550 pH. The first package type requires 11 capacitors whose value is 1.0 μF. The second choice is the 0612 which will require 6 capacitors whose value is 2.2 μF. The 1210 package will be chosen since it is within the range of acceptable capacitance.

Stage 1 requires a capacitance value of 117 μF and an inductance value of 9659 pH. The power supply requirements are such that the value of capacitance is considerably higher than 117 μF, and as a result, the inductance requirement will be easily met.

5.11 Summary of Compiled Results

This completes the analysis of the determination of the die capacitance, the series inductance of each stage, the capacitance of each stage and the frequencies of interest for each stage. *Table 5.2* illustrates the values of f_L, f_H and f_R for each stage.

	F_L	f_H	f_R
Stage 4	166	1714	533.0
Stage 3	16	166	51.55
Stage 2	1.55	16	4.98
Stage 1	0.15	1.55	0.482

Table 5.2: *Frequency Ranges in MHz for Each Stage of the Design Example*

Table 5.3 shows the capacitance needed and the permissible inductance for each stage.

Stage	Capacitance *μF*	Inductance *pH*	$\sqrt{\frac{L}{C}}$
Stage 4	0.106	0.84	2.82 mΩ
Stage 3	1.1	8.7	2.81 mΩ
Stage 2	11.33	90	2.82 mΩ
Stage 1	117	934	2.83 mΩ

Table 5.3: *Inductance and Capacitance for Each Stage.*

Table 5.4 summarizes the estimated values of capacitance and their parasitics, quantities, and total equivalent component values.

Stage	*C* *μF*	*L* *pH*	*R* *mΩ*	No. of Devices	Total *C* *μF*	Total *L* *pH*	Total *R* *mΩ*
Stage 4	0.106	0.84	9.11	1	0.106	0.84	9.11
Stage 3	0.033	320	167	37	1.22	8.67	4.51
Stage 2	1.0	1000	16.0	11	11	91	1.45
Stage 1	1000	2450	35	14	14000	175	2.5

Table 5.4: *Capacitance and Inductance for the Design Problem.*

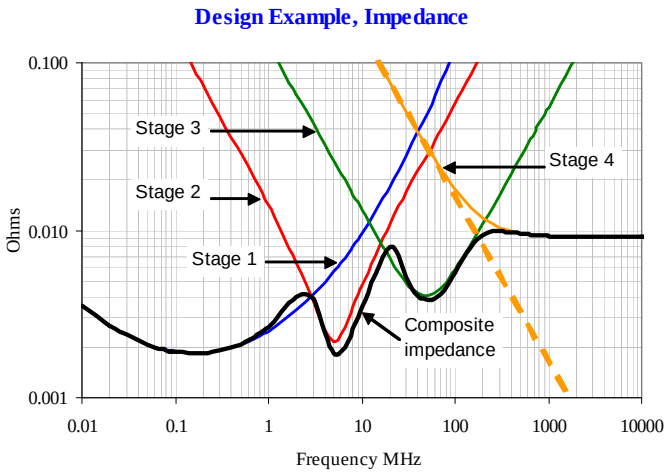

Figure 5.10: *Impedance of Design Example*

The result of the selection of components and their equivalent parasitics, as well as the overall effective impedance, is shown in *Figure 5.10*. Although the intended goal is to have a relatively flat

impedance across the bandwidth, the actual lack of flatness is due to available component types.

5.12 Summary of the Capacitor Selections and Graphical Results

Figure 5.10 shows the results of the design. The leftmost curve represents *stage 1*, the second from left is *stage 2*, the third is *stage 3*, and the rightmost is *stage 4*. The overall impedance of these four stages is represented by the heavy line. The system will see the impedance of the heavy line because it is the composite of all four stages.

One can make several observations from *Figure 5.10*. The bandwidth is wider than calculated, which is a result of using a considerably larger number of stage 1 capacitors to meet the power supply requirements. The estimated value of stage 1 capacitance is 117 μF. This is not suitable to maintain the estimated transient response from the power supply. A much larger value is needed to keep the transient response at a reasonable level.

The impedance at each parallel resonant frequency has met the goal of 10 mΩ or less. The parallel resonant frequency of 1.55 MHz and 16 MHz has been achieved. The impedances at the parallel resonant frequencies have met all other calculated expectations.

The resultant composite line at each of the parallel resonant frequency points has a value of impedance less than or equal to that which is represented by the intersection of any two capacitors. The lines of *stage 1* and *stage 2* intersect at 3 MHz, which is a point of equal impedance. The same situation applies to the intersection point of the *stage 2* and *stage 3*. The intersection of the third and fourth lines is higher in the impedance value than that represented by the composite line in this same area. This indicates that the value of Q_S, although not necessarily the perfect value, is adequate. The *stage 1* line also intersects with the *stage 3* and *stage 4* lines, thus causing the resultant composite line to shift. All of these must be accounted for although these are secondary affects.

The actual parallel resonance between *stage 3* and *stage 4* is as predicted. The approximate value of 170 MHz, as shown by the dashed line that crosses the *stage 3* line, represents the inductance of *stage 3*. The dashed line represents the on-die capacitance.

The goal for a reasonably flat impedance across the entire bandwidth has not necessarily been met. The series resistance of *stage 3* is considerably less than the goal, as is *stage 2* and *stage 1*. The goal of having a Q_S of less than 0.50 has been met; the expectation of no parallel resonances has not been met. This is due to the selected capacitor for *stage 1*. The value and number of packages for *stage 1* has been increased to meet the requirements of the power supply. The value of capacitance selected for *stage 4* is a minimum value and, as can be seen from *Figure 5.10*, just meets the goal of 10 mΩ.

The overall performance of the impedance is quite acceptable for the entire range of frequencies. Each stage will need additional resistance to flatten the impedance profile in order to see the effects of having the correct value of series resistance. Added resistance is determined by the value of the series Q required for each stage to provide a zero resonant frequency. An interesting fact is that *stage 1* needs additional inductance to bring its impedance to 0.009 Ω. In fact, *stage 2* and *stage 3* need some small amount of resistance to bring the overall impedance to the desired level.

5.13 Graphical Results with Added Resistance

Figure 5.11 shows that with added resistance, the resultant impedance curve improves considerably, almost reaching an ideal. The goal of 10 mΩ maximum for each stage has been met and the overall bandwidth, more than estimated. *Figure 5.11* also shows the parallel resonant points, the impedance intersections of each stage and the resultant impedance as represented by the black line. The summary line shows very little deviation with added resistance. In addition, *Figure 5.11* shows the impedance needed for each stage, particularly the amount of the added series resistance needed to obtain a flat impedance.

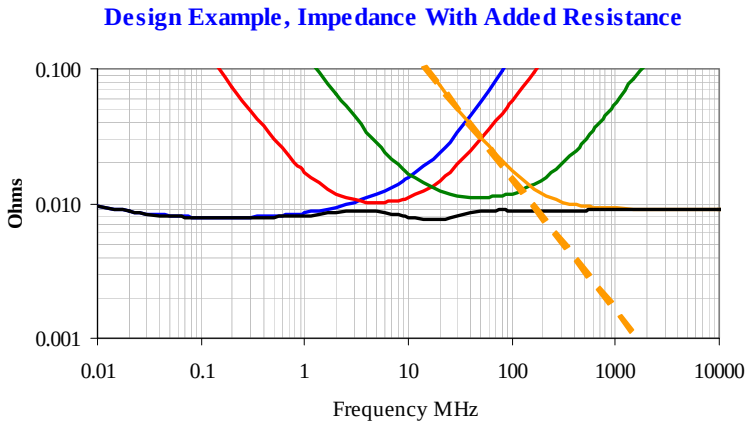

Figure 5.11: *Impedance with Added Resistance*

The actual *ESR* value of the capacitor is much lower than required. With a lower *ESR* value the temperature rise in each capacitor will be lower, increasing its useful life. Since the power dissipated in each capacitor is related to I^2R, if the resistance is increased by a factor 5, then the power dissipated within the capacitor is increased by the same factor. The dynamic current is 10 amperes for the system and there are 37 capacitors in stage 3. If the capacitors share the current equally, then each capacitor supports 270 mA. With the *ESR* of each capacitor being 167 mΩ, the amount of power being dissipated is 12 mW for each capacitor.

The method of adding resistance or impedance to each stage is accomplished by adding resistance to each capacitor for stage 2 and 3, and some inductance to stage 1. The effect as shown in *Figure 5.11* is the reduction of the overall variation in the series impedance between the power supply and the load or chip. The series impedance in *Figure 5.11*, varies from about 8.0 mΩ to 9.47 mΩ..At specific frequencies, where the impedance is the lowest, there is the lowest series voltage drop to the chip or load. This method does have the problem, however, of finding resistance values low enough which result in more components, more opportunities for failures, and an increase in both cost and cost of ownership.

5.14 Sensitivity

Added Resistance

The next obvious question is: to what degree is the overall impedance degraded with changes in some of the other parasitics? The changes in resistance to *stage 2* and *stage 3* have been shown in *Figure 5.11*. The value of resistance is based on the number of capacitors in each stage. The value of resistance is divided by the number of capacitors used. Each of the added resistors has some inductance and this inductance has to be added to the total inductance of each stage. As a result, some additional capacitors may have to be added in order to maintain the proper inductance value.

Added Inductance

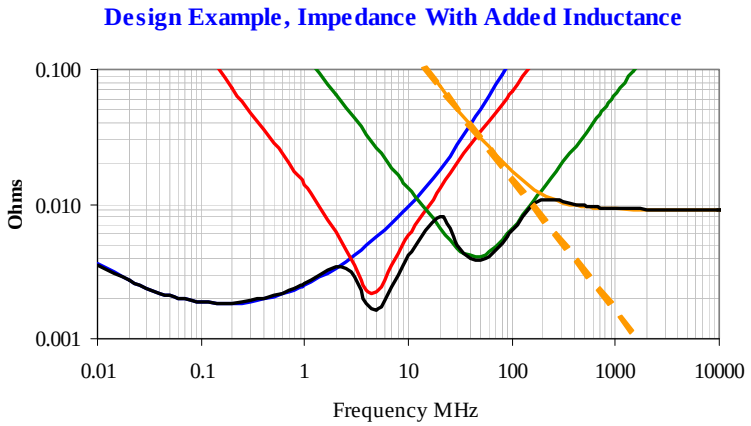

Figure 5.12: *Impedance with Added Inductance.*

The effect of adding more inductance is not necessarily intuitive. *Figure 5.12* shows the effects with just 20 percent more inductance in *stage 2* and *stage 3*. The result of the increase in inductance is a shift in the resonant frequencies to the left and an increase in the values of impedance. The circuit now fails to be acceptable in the range of 150 MHz to 350 MHz. The value of impedance in this range is above the 10 mΩ goal. The value of inductance estimated is the maximum value and a lower value should be used, requiring the addition of a few capacitors.

Figure 5.13 shows the results with 20 percent less inductance. The resonant frequencies have shifted to the right just a little and also provide slightly lower impedance. Again, the system is still quite well behaved. The system *Q* is improved and can be readily seen in the 100 MHz to 1000 MHz region. This region, as represented by the line of composite impedance, is considerably smoother than in *Figure 510* or *Figure 5.12*.

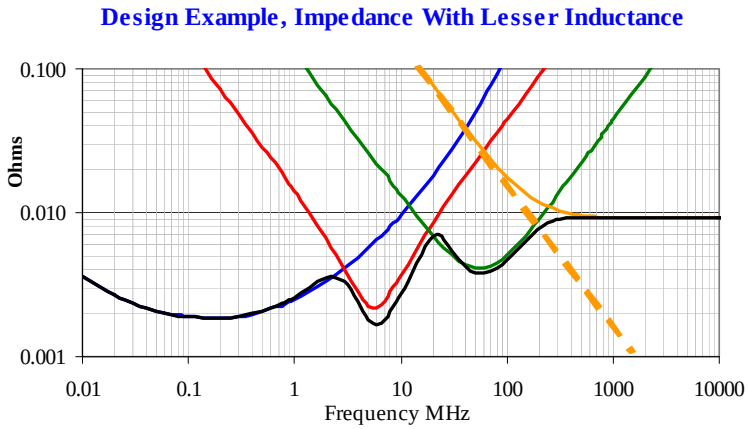

Figure 5.13: *Impedance with Less Inductance.*

Added Capacitance

The advantage of adding more capacitance to *stage 2* is extremely low because it would interact with the inductance of *stage 1* whose impedance is already lower than required. Adding capacitance to this stage would shift the intersection of the blue line to a lower frequency. However, adding more capacitance to *stage 3* and *4* would produce a lower peak impedance of the parallel resonance between *stages 2* and *3,* and it would shift the resonance to the left.

Adding more on-die capacitance to *stage 4* would lower the impedance and shift the parallel resonant frequency to the left. Adding capacitance to just *stage 3* alone has some interesting effects. *Figure 5.13* shows that with the current capacitance, the impedance relative to *stage 1* and *stage 2* is much higher. If the number of *stage 3* capacitors were to be doubled, then the resonant

frequency would remain the same and the value of the total *ESR* would be halved. The doubling effect would provide an *ESR* value that is close to the values of *stage 1* and *stage 2*. The doubling effect also produces twice as much capacitance for this stage and half the inductance. The new parallel resonant frequency would be 70 percent of the previous frequency. Looking at *Figure 5.13*, at the point of about 23 MHz, the new frequency is about 16 MHz and the peak impedance would be about 6 mΩ. Doubling the number of capacitors would also reduce the inductance. The inductive portion that would intersect with the on-die capacitance has a new parallel resonant frequency which is 30 percent higher in value and whose impedance would be reduced at the new resonant frequency.

A reduction of capacitance could have detrimental effects and would significantly increase the impedances of *stage 2*, *stage 3* and *stage 4* at their resonant frequencies. The effect of reducing the on-die capacitance will cause the impedance to increase to the point of failure in meeting the required goals. This also points to the fact that the value of capacitance estimated is a minimum value, and therefore the tolerance of these devices should be accounted for. Typically, a 20 percent tolerance for X5R or X7R capacitors should be used to keep costs to a minimum. The estimated value of capacitance should be increased by the tolerance level and will lower the inductance by the same amount. From a design point of view, a check should be made with minimum capacitance and maximum inductance.

5.15 Summary of the Design

Given the design factors that described the input parameters (that is, the loop response of the power supply; the static and dynamic currents of the load; the load voltage, as well as its switching characteristics) a certain number of stages and a selection of different capacitors were determined. The value of noise voltage was provided and was used to determine the maximum value of series resistance that will satisfy the needs of the design. The value of capacitance and inductance for each stage has been determined. The inductance, resistance, and capacitance requirement of each capacitor within each bank has been determined by the quantity of each capacitor type used.

The design was plotted to see the curves for each capacitor bank and to see if the design met the goals. It was found, as expected, that the actual impedance was lower than required in some areas. The results were due to the lower series resistance of the capacitors themselves. The design was found to be acceptable and met all the requirement goals except for flatness of the impedance curve.

Resistors were added to each stage to bring the series resistance up to 9 mΩ. The result was plotted, and it was found that the impedance curve was considerably flatter. It was also found that the advantage of adding resistors to each capacitor was that a smaller variation of the impedance resulted over the entire frequency range of the distribution network. In addition, one big disadvantage of adding resistors to each capacitor was that it doubled the number of components, increased opportunities for failure in the manufacturing process, the increased probability of failure over time, and increased cost of ownership and the additional board space to accommodate the resistors whose real estate costs are already considerable.

The design methodology has been proven both theoretically and by simulation results, representing two parts of the Iron Triangle. A practical implementation of the design is achieved by building prototype boards to prove the results obtained by simulation. An aspect of the design that was not incorporated into this simulated system is the inductance and resistance of the planes between the different capacitor banks. The position of each of these capacitor banks to each other will add inductance and both alternating current (AC) and direct current (DC) resistances. In the case of the stage 3 capacitor bank, the distance relative to the package of the chip is fixed. The components will be placed next to or as manufacturing will permit, as close as possible to the package. Stage 1 capacitors are typically located as close as possible to the point of entry to the board of the power supply.

Finally, board inductance, due to the manufacturing processes, will vary approximately ten percent. In addition, the inductance of the capacitors and their series resistances is a strong function of the variation in the length, width, and thickness in the capacitor

package. Typically, these dimensional variations are between five percent to ten percent depending on the original equipment manufacturer (OEM) supplier. These dimensional variations can be as much as ten percent at the extreme and should be accounted for. The series resistance of the added on-die capacitor has a tolerance value and the maximum value of resistance should be used. In addition to the tolerance of the series resistor, the operating temperature range effects of the resistance of the on-die capacitor should be factored into the overall tolerance study.

Table 5.1 shows the requirements for this simulated design and has no information about the package inductance or DC resistance of the load. No attempt has been made to estimate its real values. Although the load may be a memory chip, a central processing unit (CPU), or some other device, the inductance and resistance from its pin(s) to the actual die in the center of the package is very important. Some of these devices have gull wing type pins around the periphery of the device or they may have short stubs all along its underside. It is to have equal current sharing between the board and the pins or pads of the application-specific integrated-circuit (ASIC), CPU, or any other integrated circuit. The goal is to provide a voltage to the center of the die that has a very small variation due to the switching action of the load. The value of inductance and resistance of the package has a strong influence on the voltage that the die will actually see. It has not been the practice of OEM suppliers to provide data about the parasitic elements. If the package inductance, resistance, and capacitance were known, then the work of the signal integrity engineer would be much easier, and there would be no guessing as to the value of these elements. This information would further the quest to minimize simulation failures, reduce the cost and bring the product to the market place sooner.

The value of the signals, that is, the quality of the edges and amplitudes of the signal, is dependent on the quality of power delivered to the load. This is the responsibility of the power integrity engineer, and without power integrity, there is no signal integrity. The purpose of a power distribution system should be quite clear, as its design has been demonstrated to work in the simulator. However, the evidence clearly shows that there is an

urgent need for power integrity which another compelling reason for a good power distribution system.

Important Points to Remember Are:

- On-die resistance, the value estimated is a maximum value and should be reduced by its tolerance value.
- The inductance estimated for each capacitor stage is a maximum value, and should be reduced by adding more capacitors.
- The value of on-die capacitance is a minimum value and should be increased by its tolerance level.
- The value of capacitance for each stage is a minimum value and should be increased by 20 percent.
- Each stage is represented by a different type of capacitor. Each type of capacitor has its own characteristics that differ from the others. This essentially prevents the designer from meeting the perfect goal of a maximally flat impedance line.