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# Impact of Regulator Sense-point Location on PDN Response

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## Abstract

Sense points optimally placed on a system to allow a feedback path for a DC–DC converter to regulate the DC voltage at that sense point. Typically this is done with only DC drop compensation in mind. This paper looks at how the stability and transfer function of the converter is affected by the location of the sense points with respect to the converter, the load, and the decoupling capacitors. The stackup will also be looked at, too, as it may affect each element of the PDN.

## Author(s) Biography

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# I. Introduction

Our modern electronic circuits require low supply voltages, sometimes with sub-volt nominal values, with very tight tolerances over part-to-part variations in the Power Distribution Network (PDN), temperature and load-current fluctuations. To avoid excessive power loss in the distribution, the raw input voltage, especially for the high-current systems, has to be high. To generate stable DC power for the low-voltage supply rails with high efficiency, non-isolated or isolated step-down switching regulators are commonly used [1]. Most commonly used today are the non-isolated step-down converters, also called Buck converters. These switching regulators are also called DC-DC converters (though this class of regulators strictly speaking also contains linear, non-switching regulators), or Voltage Regulation Module (VRM), or if implemented with discrete components, Voltage Regulator Down (VRD). The general block schematic of the power conversion circuit and their typical waveform sketches are shown in *Figure 1*.

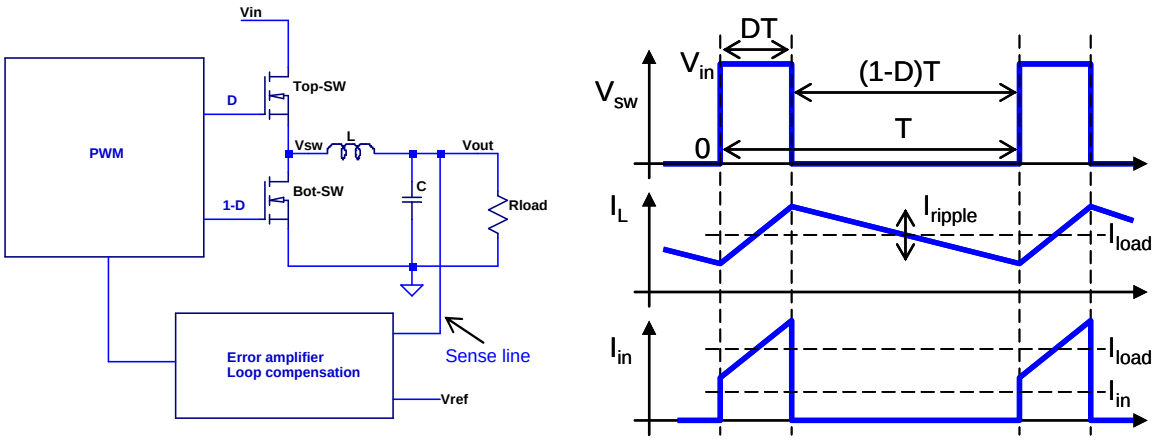


***Figure 1:*** *Block diagram of the generic power conversion stage.*

In most practical implementations today, the *C* capacitor shown in *Figure 1* must be a collection of different-valued capacitors, covering the full frequency range determined by the operation of the DC-DC converter and the load. These capacitors have to serve multiple purposes: they have to handle the output ripple current generated by the switching converter stage and also have to provide the required mid- and high-frequency impedance for the load. This means when multiple capacitors are used, some of them should be close to the converter output and some of them should be closer to the load(s). It is also very typical today that the entire circuit, power conversion, capacitors and load alike, are on the same printed circuit board. The power source and the load(s) are connected by appropriately sized traces and/or plane shapes. For single load applications (Point of Load or POL) and when the PCB layout is compact and robust enough that the voltage drop between the converter output and load points is negligibly low, the entire circuit can be viewed as a lumped network and therefore the locations of components, load and sense-point connection –within the small physical boundaries- matter very little. In such cases, and when we use off-the-shelf converters, we may not even realize that there is a 'remote' sense point in the circuitry as it is then connected inside the converter

module to its own output point. The other extreme case is when the converter output and load are separated by larger distance and may be connected through resistive cables. In this extreme the remote sense circuit has to employ some other tricks to minimize the impact of the voltage drop and at the same time to keep the control loop stable [2].

In the huge parameter space in between the above extremes, remote sense points are used to allow the feedback path for a DC–DC converter to compensate for the voltage drop between the DC source output and the loads. In many applications we can afford and have to use a higher total copper weight for our return (ground) connections and therefore many converters provide only high-side remote sense connection. In the most demanding applications, as shown in *Figure 2*, remote sense is used both on the high and low sides.

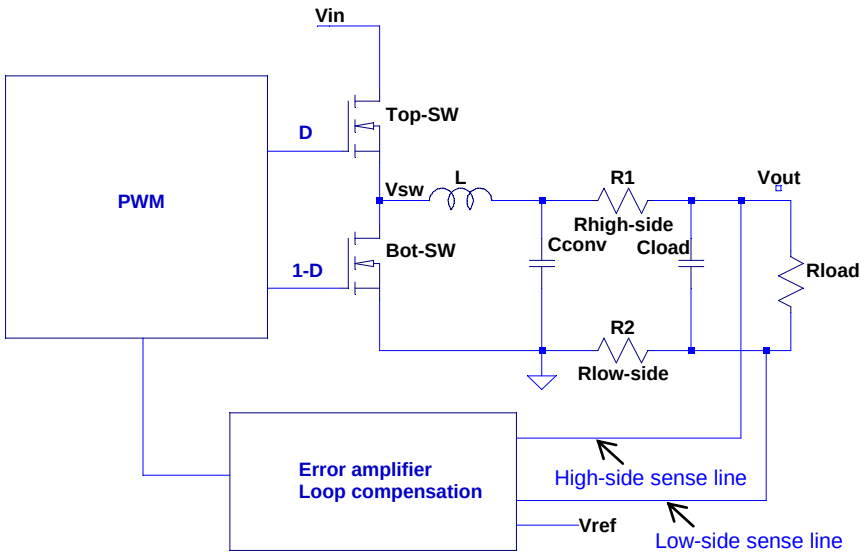


***Figure 2:*** *Block diagram of a PDN with differential remote sense. The equivalent circuit separately identifies the high- and low-side connection resistances and the separate capacitor banks for the converter output and load(s).*

Many times the remote-sense circuit analysis is done with only the DC drop compensation in mind. This paper looks at how the transfer function of the switching converter may be affected by the location of the sense points with respect to the converter, the load, and the decoupling capacitors [3]. A common application across various industries where such compensation happens and it may impact the dynamic behavior of the PDN is when we have to feed large memory arrays. In a competitive design the number of PCB layers and the total copper weight are limited and many times layout designers have to chop up the otherwise already crowded plane layers to accommodate additional supply rails, leaving the memory PDN with higher resistance and therefore higher voltage drop. The remote-sense connection of the converter will readily compensate for the DC voltage drop, but the increased series impedance of the weakened planes and the additional phase shift created by the series plane impedance and parallel capacitor impedance will alter the dynamic response to the worse: additional

phase shift in the feedback loop lowers the phase margin and increases the distortion of time-domain response. In recent publications memory –and DDR in particular- has gained a lot of attention by analyzing interaction between signal and power integrity issues, namely the impact of power-plane referencing [4].

To illustrate this point, *Figure 3* shows the comparison of two large memory PDNs living on the same board side by side and therefore sharing the same common board stackup. Both memory PDNs had the same schematics and nominally the same components. The multi-phase DC-DC converter had digitally adjustable loop control compensation and for this test both sides had identical tap settings. Furthermore the intent was to create identical layout as much as possible, but due to unavoidable constraints, the component placements and plane shapes had minute differences between the two sides.

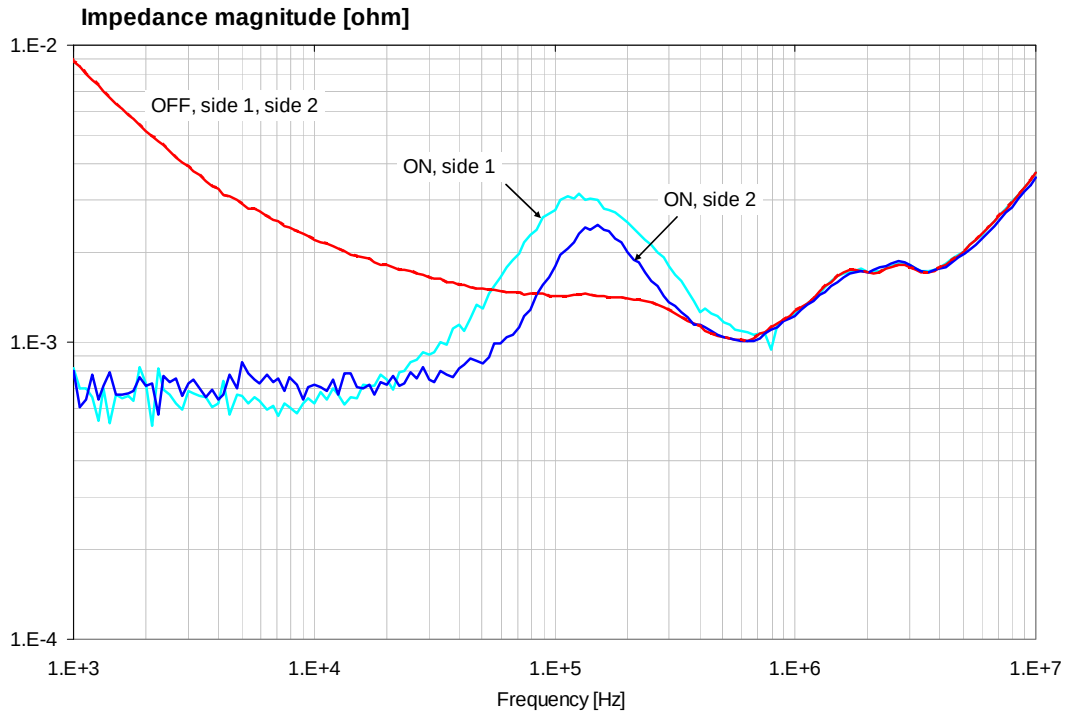


***Figure 3:*** *Two instances of a memory array on the same PCB, with the same number and types of capacitors and same converter compensation setting.*

The two instances had impedance-measuring test points at symmetrically identical locations. The impedance at those test points looks identical without power turned on, but differs significantly when the converters power on. It was eventually verified that the impedance difference was not caused by unit-to-unit variations of the power converters; it was caused by the minute layout and placement differences. Note also that it was not possible to find a single common tap setting that could produce nearly identical impedance profiles between the two sides.

## II. Detailed Problem Statement

Remote-sense connections have to be routed and connected away from the output of the power converter when the converter can not be placed in the center of gravity of load connections. To study the effect of spatial phase shift on the converter's dynamic behavior, we chose a large board with memory banks where the converter output was several inches away from the center of gravity of load connections and therefore the remote sense connection spanned a considerable phase shift. The board had an overall 16" x 20" outline and the multi-layer board had, in addition to the dedicated signal and signal-reference layers, six dedicated layers for high-current power-ground connections. *Figure 4* shows the approximate component placement and board top view.

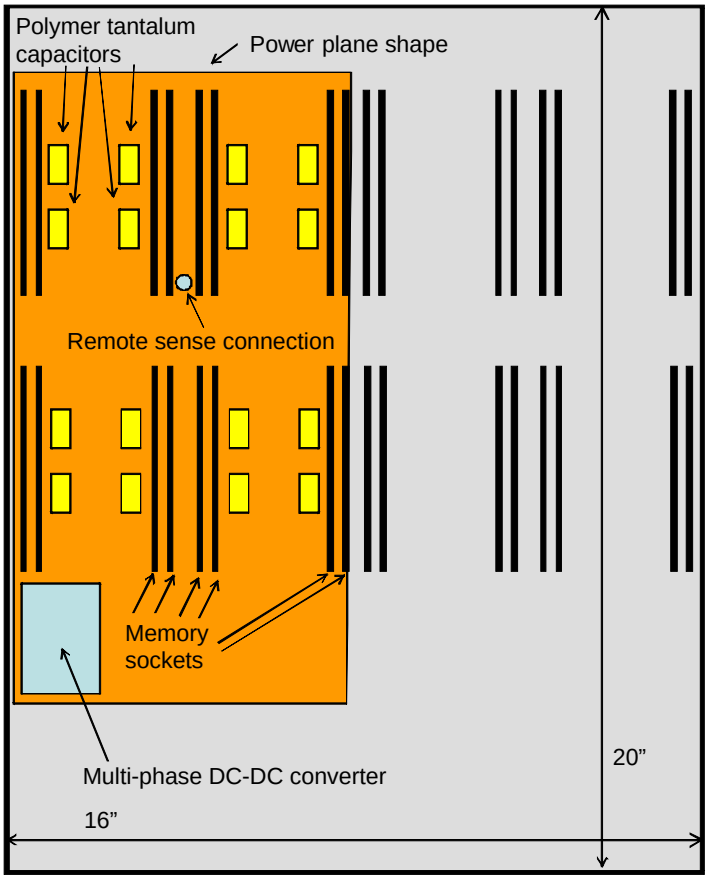


***Figure 4:*** *Approximate component placement and layout of the memory array used in the study.*

The black vertical bars indicate the memory sockets, which consume most of the power on this rail. There are two sets of memory circuits; the plane shape feeding the memory sockets on the left side of the board is shown by the yellow shape. There are other, smaller power consumers on the same rail; those are fed on another layer by a smaller plane shape, optimized for balanced DC drop among the loads. The blue rectangular

shows the location of the multi-phase DC-DC converter. There are three different capacitors on the rail: high-capacitance low-ESR polymer tantalum capacitors serving as bulk capacitors to support the low-frequency response and converter output ripple, high-valued multi-layer ceramic capacitors (MLCC) to support the mid-frequency response, and smaller-valued ceramic capacitors in the pinfields of the low-current additional consumer chips to support their high-frequency response. The right side of the board carries an identical copy of the circuit; for sake of simplicity *Figure 4* shows only the locations of memory sockets on the right side.

## II. 1. Measurement setup

There were different kinds of measurements performed for this study:

- Component level measurement
- Impedance measurement of unpowered supply rail
- Impedance measurement of powered supply rail
- Voltage transfer function from converter output to sense point, unpowered
- Voltage transfer function from converter output to sense point, powered.

To make sure that the simulation models represent the circuit as best possible, every polymer tantalum capacitor and high-valued MLCC was marked, numbered and measured on a small PCB test fixture. The setup for these measurements was the Two-port Shunt-through connection, defined and described in [5], [6] and [7]. The photo on the left of *Figure 5* shows the toroid common-mode choke with the instrument from [7] with twelve feet of coaxial cable on the toroid core to reduce the cable-braid loop error and common-mode noise pickup. The photo on the right of *Figure 5* shows two pot-core based common-mode inductors in the instrumentation from [5] and [6]. More details can be found about the instrumentation in [8].

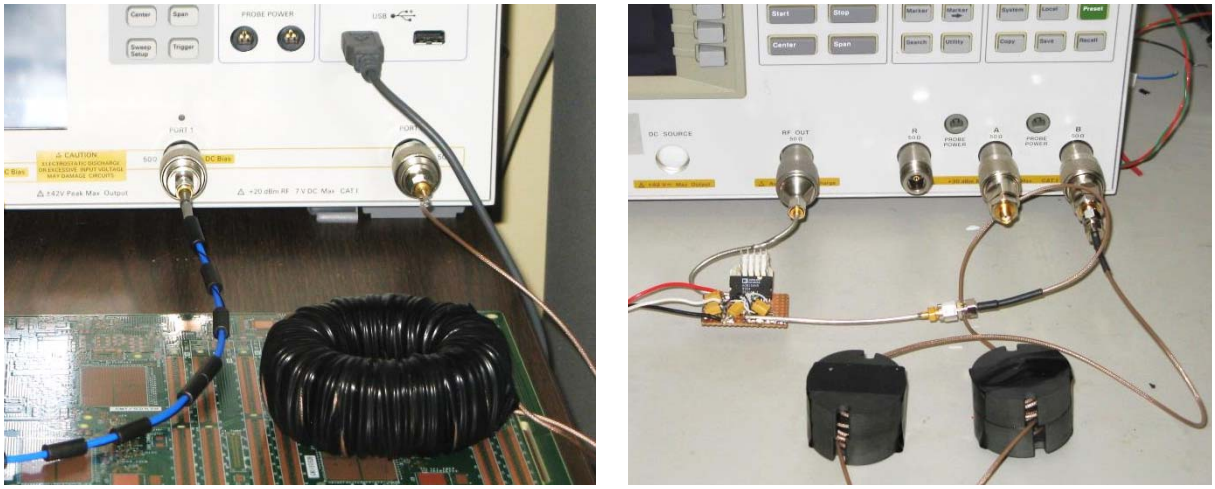

***Figure 5:*** *Common-mode toroid choke on Port 2 on instrumentation from [7] (left photo) and isolation amplifier as well as two pot-core based common-mode chokes on instrumentation from [5].*

The impedance measurements of unpowered and powered rails had the same instrumentation as described in [5], [6] and [7]. As shown on the right of *Figure 5*, powered measurements required extra common-mode chokes to suppress noise induced by the large cable loops connecting all the necessary instruments: power supply, electronic load, oscilloscope and VNA.

A slightly different setup was used to measure the voltage transfer function from the converter output to the remote sense point connection. Though the voltage transfer function could be obtained also from the post-processing of the impedance matrix, taking the measurement that way requires at least two separate setups, to measure $Z_{11}$ and $Z_{21}$, and it is also noisier at low frequencies, where the impedance values are low. Data that can be obtained this way is illustrated in *Figure 6*. Note that the OFF condition, when the converter is not running, is clean and noise free in the entire frequency range, whereas it gets very noisy below 100 kHz when the converter is running.

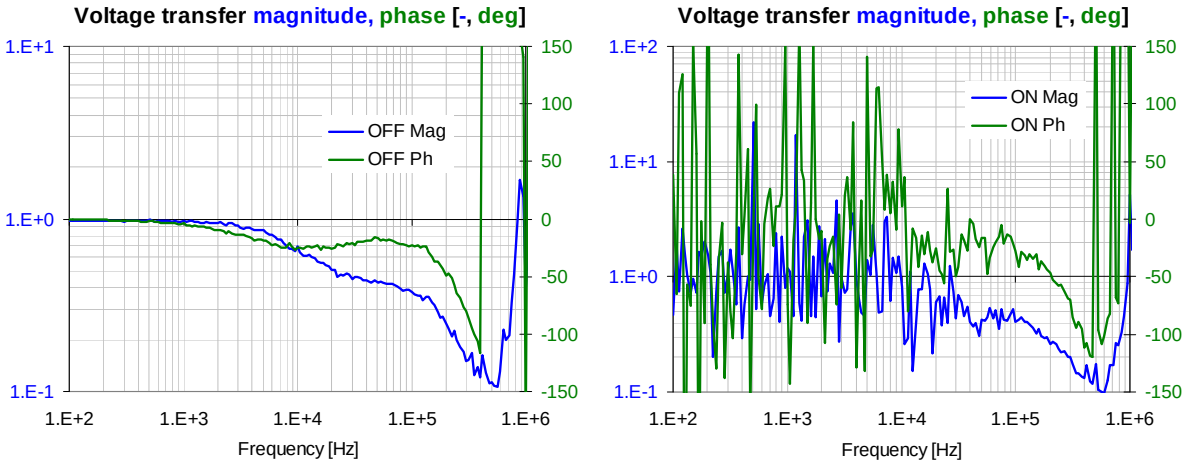


***Figure 6:*** *Voltage transfer function from the DC-DC converter output to the sense point measured through impedance-matrix elements:* $V_{out}/V_{in} = - Z_{21}/Z_{11}$.

It is simpler and cleaner to measure the voltage ratio directly. With the instrumentation from [7] we can use the T and R inputs of the Gain-Phase side of the instrument; with the instrumentation from [5] any two of the R, A and B inputs can be conveniently used. These setups work well with unpowered circuits [6], but still may become too noisy at low frequencies when the circuit is powered up. This happens because now the output is the ratio of two voltages, where each can pick up in-band noise from the converter ripple and jitter. To reduce the noise floor, a simple and efficient approach is to boost the test current with a one-quadrant amplifier, what we can also call dynamic load. A one-quadrant amplifier works well for DUTs with a fixed polarity source voltage, but it can not work with passive circuits. For various options, see for instance [9]. The circuit schematics of the home-made one-quadrant circuit and its physical implementation are shown in *Figure 7*. We need a bias DC source to set the operating point of the FET to Class A. With a 0.1-Ohm Rsense resistor in the source path of the power FET, we can

conveniently draw at least a couple of ampere peak-to-peak AC current from a 1.2V memory rail. The noise improvement is illustrated in *Figure 8*.

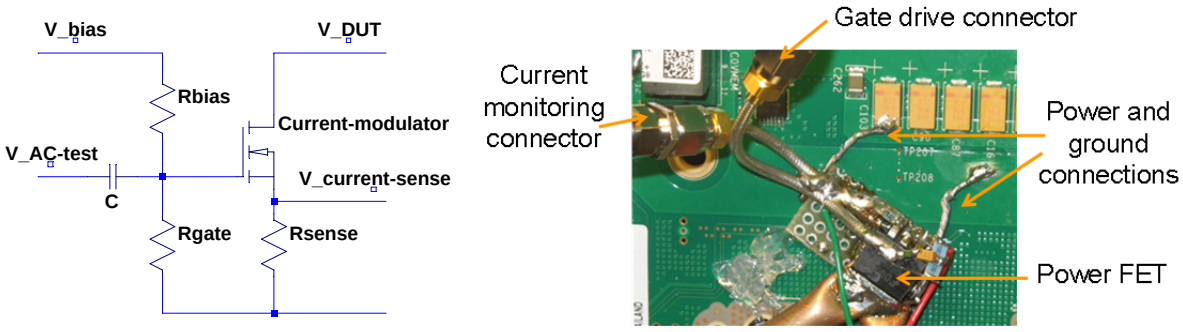


***Figure 7:*** *Schematics (on the left) and physical implementation (on the right) of the current-boost amplifier. The AC test signal input and the current-monitoring output connections are coaxial connectors on semirigid cables. To reduce inductance, the Rsense source resistor of the power FET is created from a set of ten SMD resistors in parallel. The power and ground load connections are short wires.*

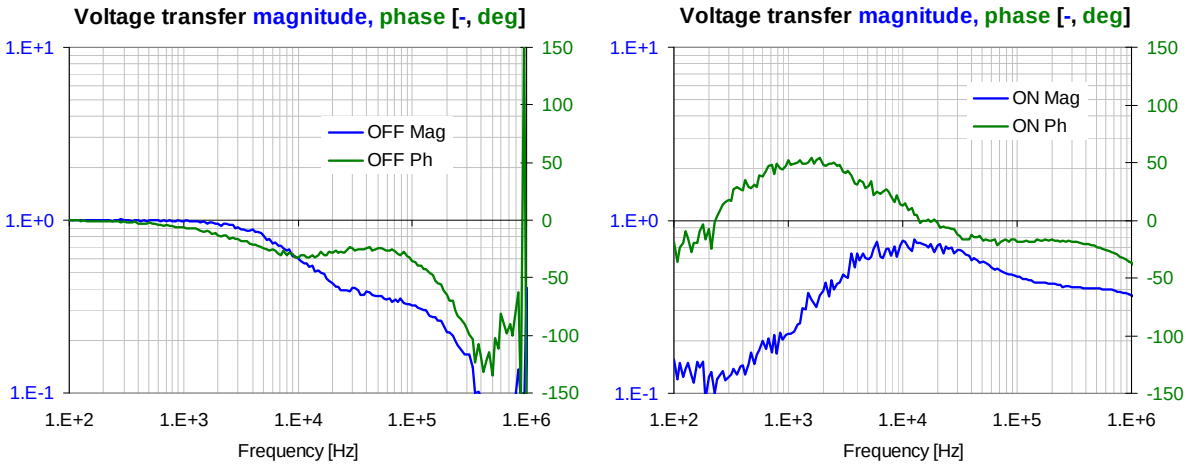


***Figure 8:*** *Illustration of the noise reduction of the current-boost amplifier on the measurement of voltage transfer functions in powered supply rails. Compare to Figure 6.*

Note that the voltage transfer function with the DC-DC converter unpowered starts out at low frequencies with unity magnitude and zero phase. This is because under these circumstances there is no low-resistance DC load on the rail to form a voltage divider with the plane resistance. When the converter is turned on and its remote sense lines are connected to a distant location, the converter's active loop tries to maintain the low impedance at the remote-sense point as opposed to the output of the converter. This creates a voltage divider and a phase shift at low frequencies, where the loop gain is high. From *Figure 3* we can conclude that the estimated control-loop crossover frequency is somewhere in the 50 to 90 kHz frequency range.

## II. 2. Simulation setup

A hybrid solver was used to simulate the board in different configurations. Ports were defined on the board at all of the capacitor locations, each output phase of the converter, the existing sense connection, and a new sense location; essentially all of the measurement and test points. The DC-DC converter outputs were left open. The bulk and ceramic capacitors were simulated with their measured S parameters. The components were measured on a small fixture and the shorted fixture's impedance was subtracted to approximately represent the impedance of the capacitor loop associated with the capacitor body [6]. The simulation was done with adaptive sweep over a large frequency range, but the focus of interest was the 10 kHz to 1 MHz frequency range, where we have the crossover frequency of most DC-DC converters. The hybrid solver offers S, Z or Y matrix output. The parameter of interest in our case is the magnitude and phase of the voltage transfer function from the converter output to the remote sense point: this was calculated externally by post-processing the network matrix output. Simulations were run for different capacitor population options. *Figure 9* shows the approximate location of the measurement and test ports for the output phases of the converters, the original remote sense location, and a new sense location.

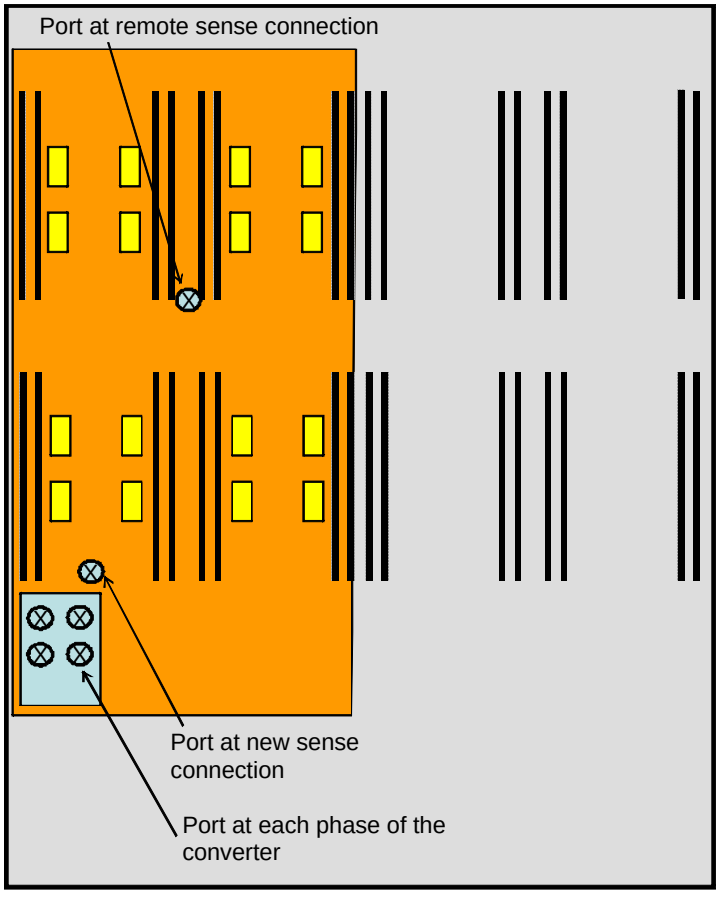


***Figure 9:*** *Sketch of the board with ports and bulk capacitor locations.*

The ports shown were setup in duplicate with one port on the top layer of the pcb and one port on the bottom layer of the pcb to allow for complete processing of the network matrix to obtain self impedance and the transfer gain and phase by performing Two-port Shunt-through measurements..

# III. Measured and Simulated Results

## III. 1. Component characterization and allocation

*Figure 10* shows the impedance plots for the polymer tantalum capacitors, *Figure 11* contains the similar data on the high-value MLCC.

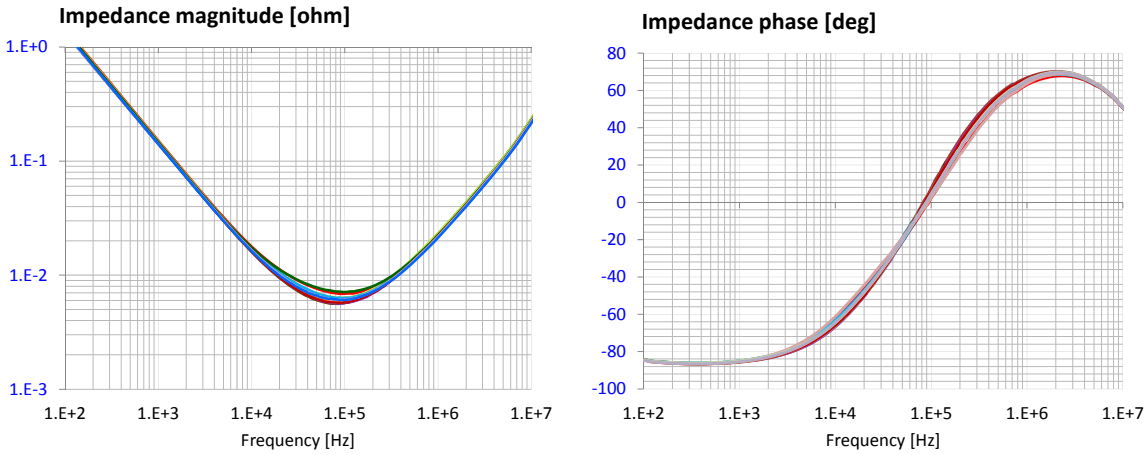


***Figure 10:*** *Impedance magnitude and phase of the polymer tantalum capacitors on the left and right, respectively.*

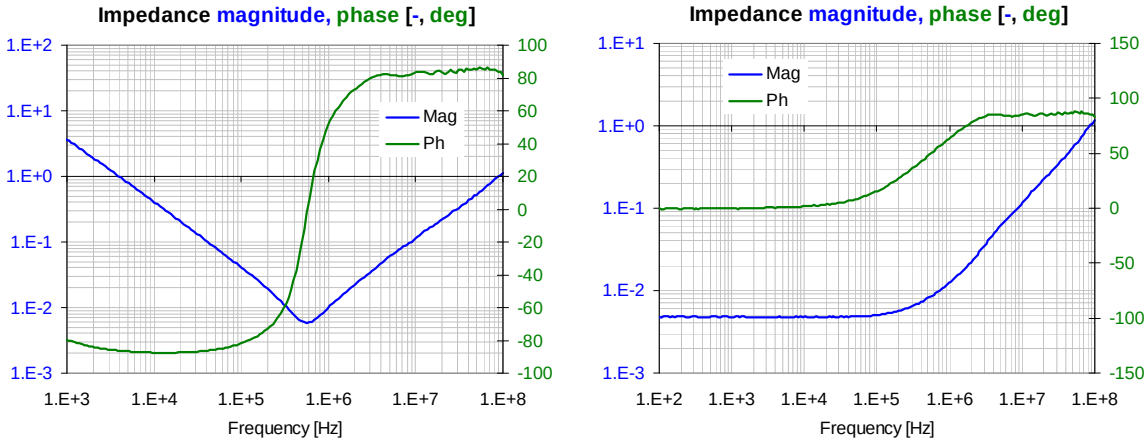


***Figure 11:*** *Representative impedance magnitude and phase of a ceramic capacitor (on the left) and of the shorted fixture (on the right).*

The capacitors showed sufficiently tight impedance across the individual parts, but nevertheless each component was marked and its location noted to provide the possibility to include each capacitor's actual measured S parameters.

*Figure 12a* shows the various configurations of bulk capacitors. The different population options are *Case 1*: all 16 capacitors, *Case 2*: the upper eight capacitors, *Case 3*: eight randomly distributed capacitors (identified by green color), *Case 4*: the lower eight capacitors and *Case 5*: none of the 16 bulk capacitors. The partially populated bulk capacitor configurations mimic the cases when for DC-drop adjustment the planes may be shaped or slotted.

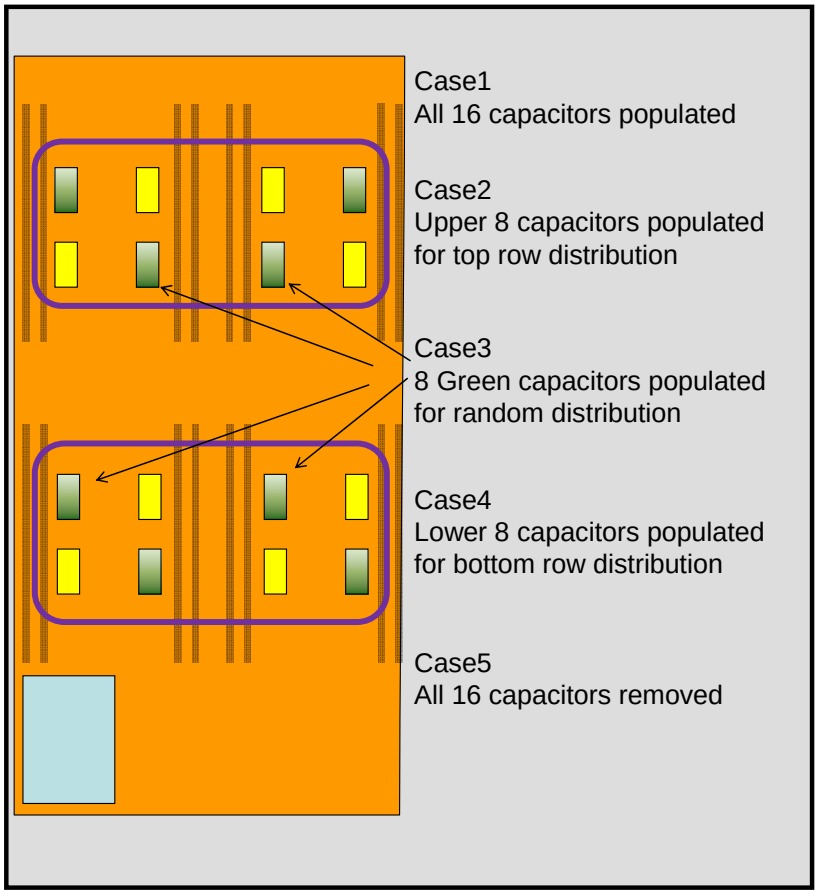


***Figure 12a:*** *The five configurations of the bulk capacitor arrangements.*

*Figure 12b* shows the simplified equivalent circuit of the voltage transfer function between the DC-DC converter output and the remote-sense connection point. Only the power output (high) side of the PDN structure and remote sense line are shown; this represents the equivalent loop of the high- and low-side losses and remote-sense circuits. For DC-DC converter stability considerations the equivalent circuit needs to cover only low frequencies, up to and little above the cross-over frequency of the converter. Since

today most buck converters have a crossover frequency at or below 100 kHz, this equivalent circuit does not need to be valid beyond a megahertz. With this in mind, the planes (single-layer or paralleled multi-layer planes) are represented with their series resistance and inductance only. Static plane capacitance is ignored for this low-frequency equivalent circuit. The parallel shunt element is the cumulative low-frequency equivalent circuit of all of the bypass capacitors on the supply rail. With a large number of different-valued bypass capacitors the single C-R-L equivalent circuit with frequency-independent C, R and L values may not be a good wideband representation of the bypass network, but below 100 kHz even a C-R equivalent circuit may provide sufficient accuracy.

The $R_{plane}$ and $L_{plane}$ components will be the same for Case 1 through Case 5, because we assume that the converter output points and remote sense points are fixed. As the array of bulk bypass capacitors is modified for the five cases, the shunt element values change. Physically the bypass capacitors represented by the C-R-L network are not located at the remote-sense point, their values are transformed through the series plane impedance between their locations and the remote-sense point, and this is why the transfer functions for the five cases are different.

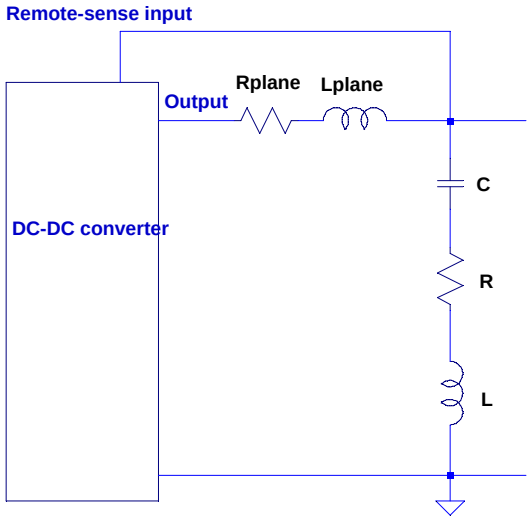


***Figure 12b:*** *Simplified equivalent circuit illustrating the elements of the voltage transfer function. $R_{plane}$ and $L_{plane}$ represent the low-frequency plane impedance, C, R and L represent the cumulative sum of all bypass capacitors' impedances transformed to the sense-point location.*

## III. 2. Measurement results

*Figure 13* and *Figure 14* show the voltage transfer function magnitude and phase for the five different bulk-capacitor population cases. Case 1 is shown also with the multi-phase DC-DC converter turned on, cases 2 through 5 are shown only with converter off. To prove the integrity of the collected data, selected voltage-transfer measurements were done with multiple instruments and with different methods: they showed good agreement.

Note that at low frequencies all response traces with converter off start out from unity magnitude and zero phase. This matches our expectations, because the input and output points are connected through low-resistance planes and at DC the passive components do not represent any loading. When the converter is powered on, the active control loop regulates at the remote-sense point, thus creating a low-frequency low-impedance load. This shows up in the <1 voltage transfer magnitude: its value is approximately 0.5 at 1 kHz. This suggests that at 1 kHz the closed-loop output impedance of the converter equals the plane resistance.

As frequency increases, the voltage transfer magnitude begins to drop and an increasing phase shift also shows up. The magnitude and phase response curves show noticeable differences among the five cases. With no bulk capacitor on the rail (Case 5), the smaller total capacitance of the ceramic capacitors does not produce any significant magnitude drop up to about 30 kHz, and up to 200 kHz its gain loss is the smallest among all cases.

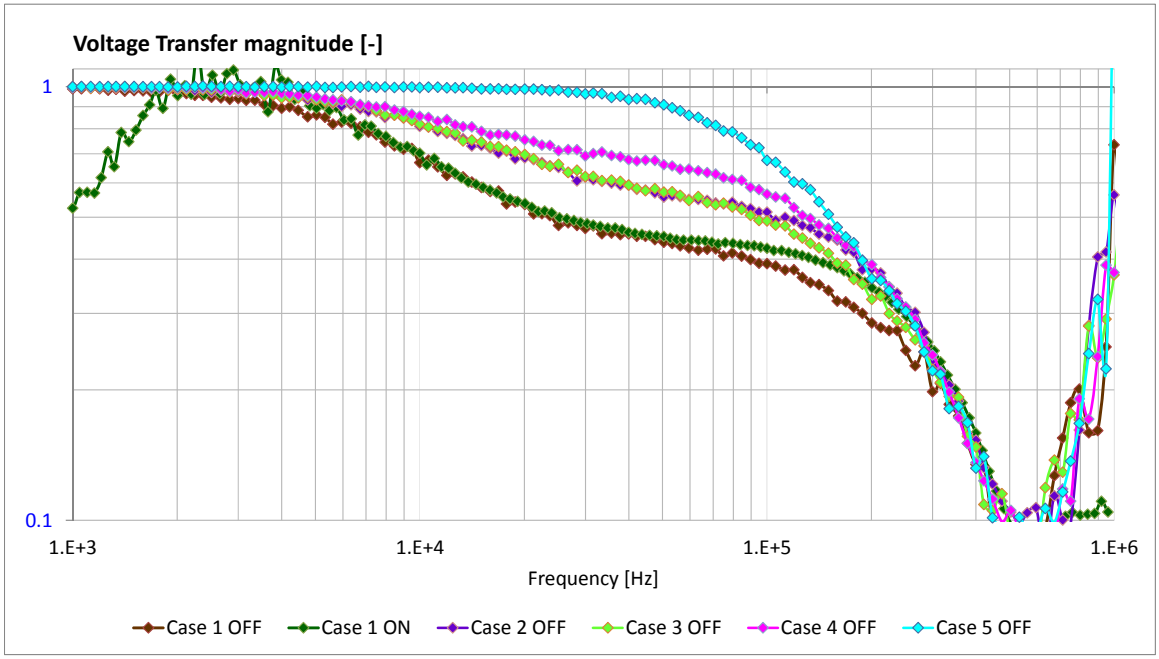


***Figure 13:*** *Voltage transfer magnitude with the original sense point location.*

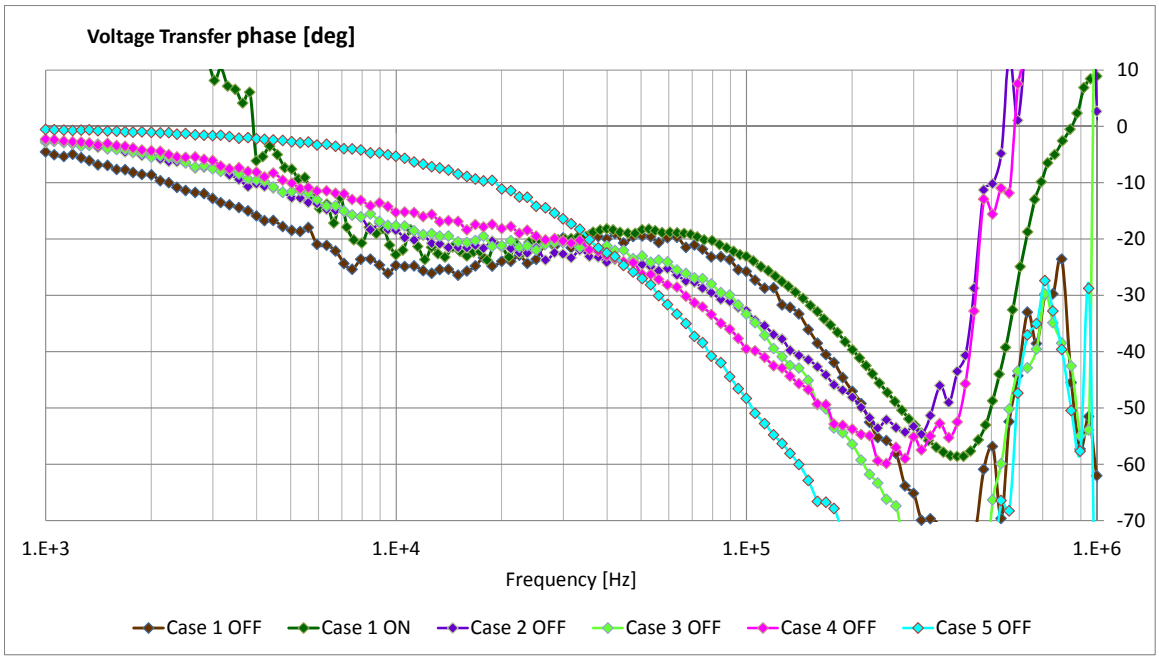


***Figure 14:*** *Voltage transfer phase with the original sense point location.*

The phase response, however, shows a very different picture. In the most important 10 kHz to 100 kHz frequency range there is significant phase shift in all five cases. The phase response curves seem to have a convergence point around 30 to 40 kHz with a phase shift of -20 degrees. Interestingly the trend among the five cases is different below and above this convergence point. While the case with no bulk capacitor (Case 5) has the least phase shift below 30 kHz, at higher frequencies Case 5 yields the highest phase shift, reaching -50 degrees at 100 kHz. The reason for this seemingly counter-intuitive result is that the series resonance frequency of the ceramic capacitors on the board was way above 100 kHz, and therefore with no bulk capacitors and at very low frequencies, the equivalent circuit of *Figure 12.b* reduces to the series plane resistance and parallel MLCC capacitance. When we add bulk capacitors with series resonance frequencies around 100 kHz or lower, they produce an almost resistive load around their resonance frequency and this reduces the phase shift.

Note also that the phase curve of Case 5 produces the steepest phase change, explaining why PDNs with only ceramic capacitor bypassing may be more sensitive to component values and component locations. Another observation worth mentioning is that the flattest phase curve comes from Case 4, where all of the bulk capacitors are in the lower half of the plane, closer to the DC-DC converter output. The overall phase variation or uncertainty, over these five cases is up to 20 degrees at 10 kHz and approximately 30 degrees at 100 kHz.

*Figure 15* and *Figure 16* show the same five cases with the new sense point location, where the remote-sense is connected to near the DC-DC converter output. As expected,

in this case there is no noticeable difference among the cases, there is no gain loss and no significant phase shift below 100 kHz.

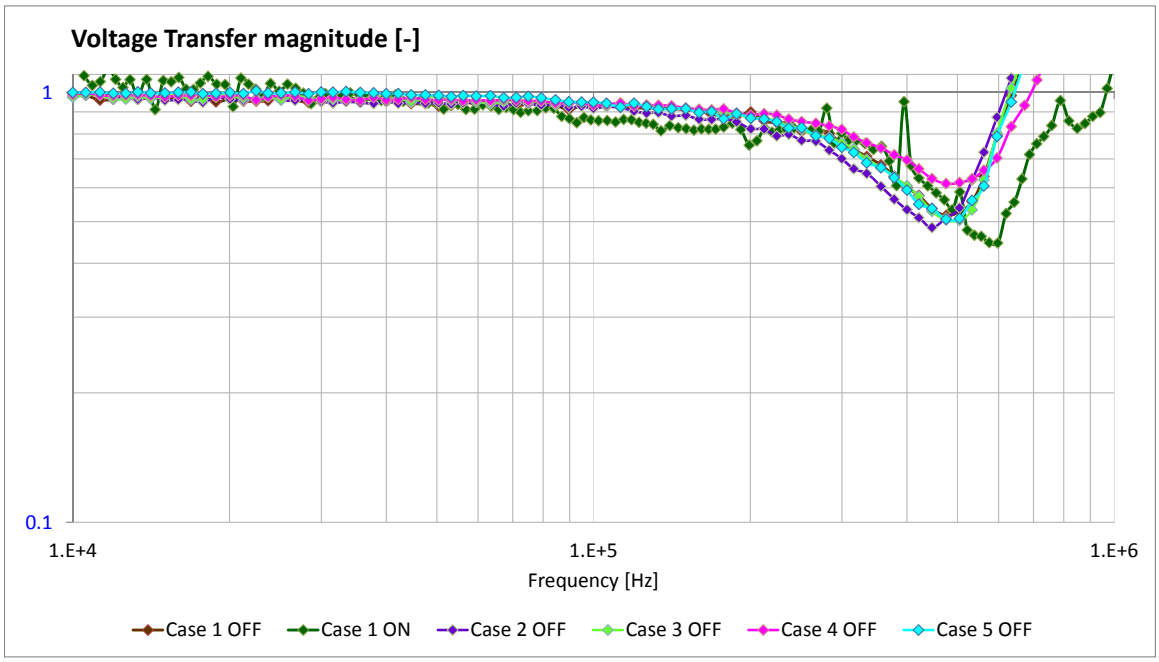


***Figure 15:*** *Voltage transfer magnitude with the new sense point location.*

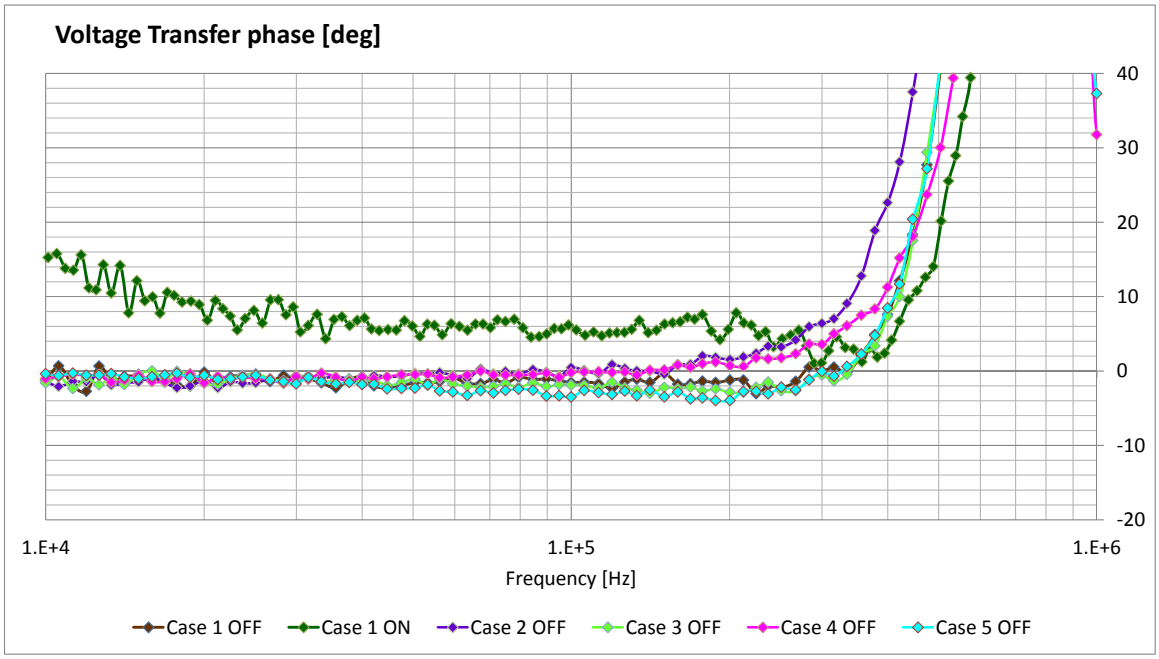


***Figure 16:*** *Voltage transfer phase with the new sense point location.*

## III. 3. Simulation results

The simulated voltage transfer magnitude and phase with the original sense point location and for the above five cases are shown in *Figure 17* and *Figure 18*, respectively. Though fine details are not reproduced with high accuracy, the overall trend and the main signatures correlate well. The simulation predicts a slightly higher phase shift at 100 kHz, and the convergence frequency is around 20 kHz, but the order of traces for the five cases is well preserved.

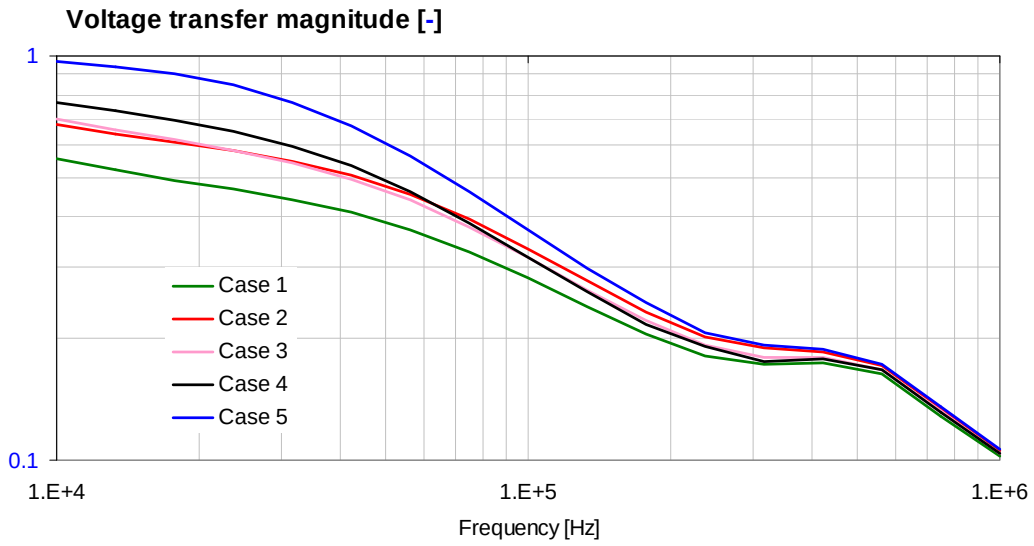


***Figure 17:*** *Voltage transfer magnitude for the five bulk-capacitor allocation cases with the original sense point location.*

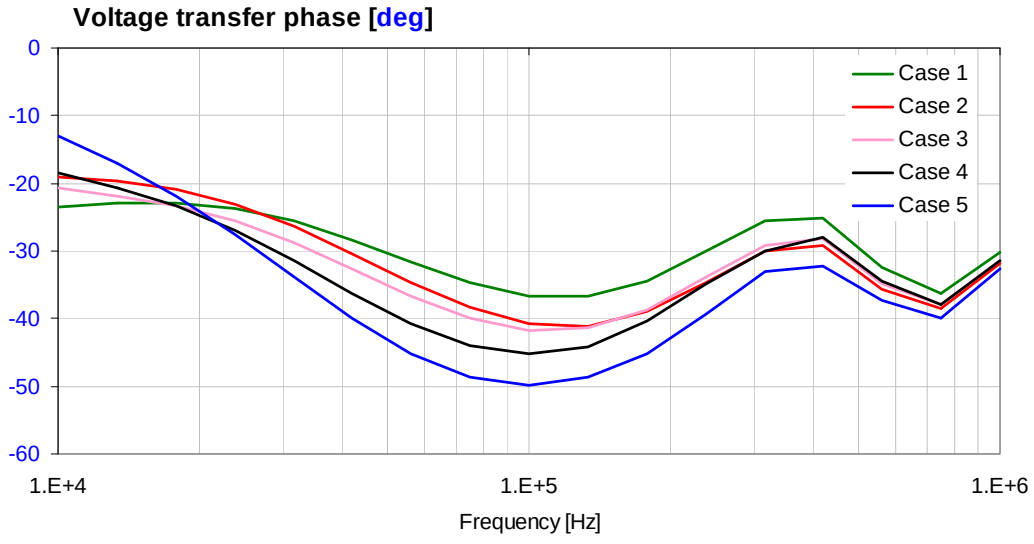


***Figure 18:*** *Voltage transfer phase for the five bulk-capacitor allocation cases with the original sense point location.*

The simulated voltage transfer magnitude and phase with the new sense point location and for the above five cases are shown in *Figure 19* and *Figure 20*, respectively.

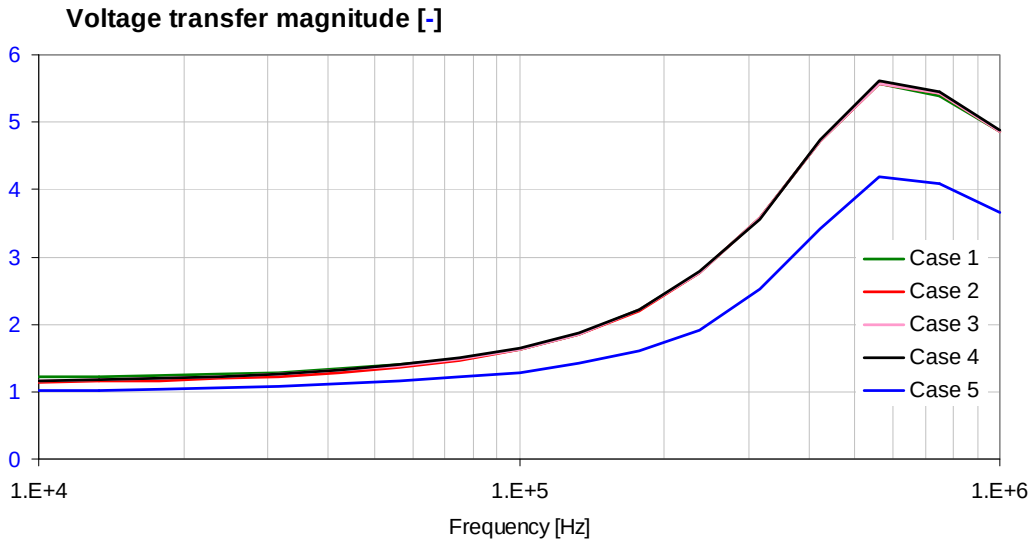


***Figure 19:*** *Voltage transfer magnitude for the five bulk-capacitor allocation cases with the new sense point location.*

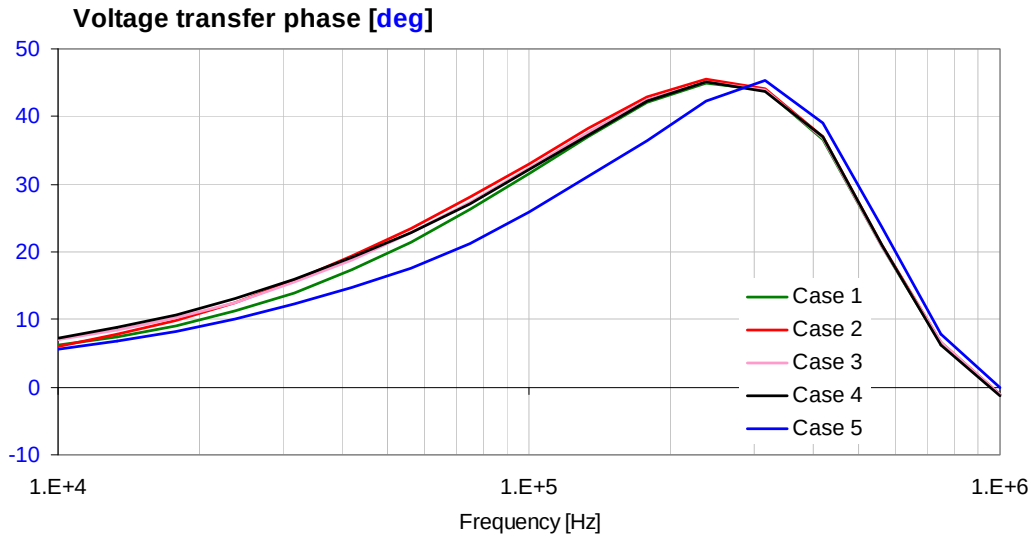


***Figure 20:*** *Voltage transfer phase for the five bulk-capacitor allocation cases with the new sense point location.*

An additional set of simulations were performed to gain insight into another common change made on a pcb to compensate the dc drop or to reduce power loss on the power planes. Simulations with all of the capacitors populated (Case 1) were run with different copper weights for the power and return planes.

Simulations were run with 1/2oz, 1oz and 2oz planes. Intuitively we can show that the magnitude of the voltage transfer would change inversely to the copper weight change. However, since the real part of the transfer response changes, the phase of the voltage transfer will also change. *Figures 21* and *22* show the results of these simulations.

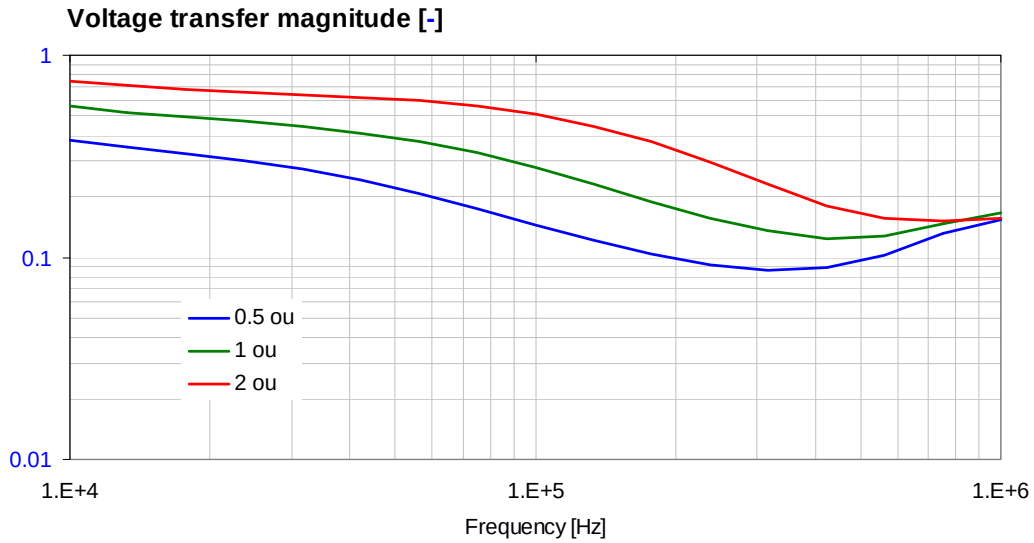


***Figure 21:*** *Impact of copper weight on voltage transfer magnitude with original sense point location and all capacitors.*

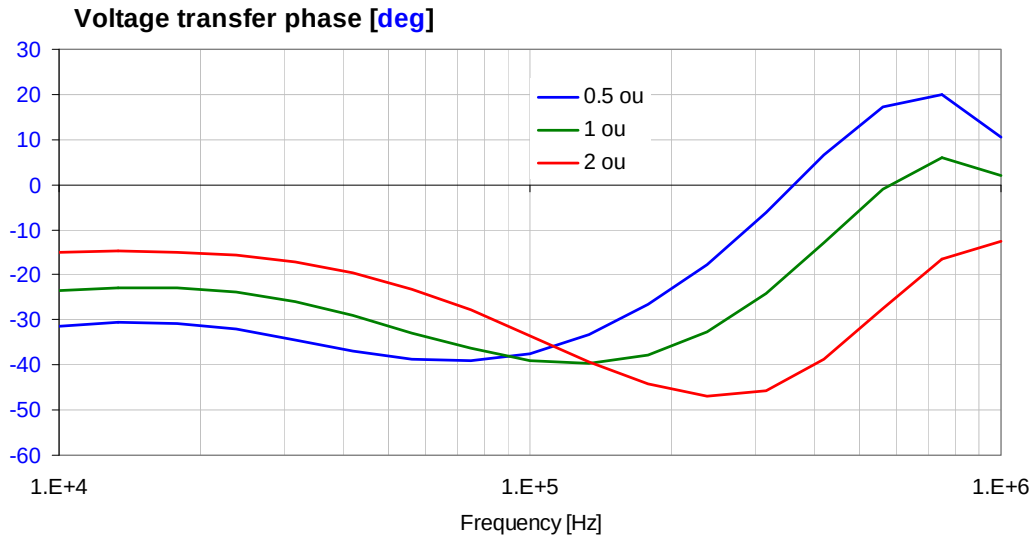


***Figure 22:*** *Impact of copper weight on voltage transfer phase with original sense point location and all capacitors.*

## IV. Conclusions

From both the measurement data and simulation results, a clear trend is shown that the change in capacitor locations and population creates a phase shift in the voltage transfer from the DC-DC converter to its remote sense connection. As shown, this phase shift can occur in the critical frequency range of the DC-DC converter's crossover frequency possibly reducing the phase margin. As illustrated in *Figure 3*, any reduction in the phase margin may contribute to the increase of PDN impedance and potentially the DC-DC converter may become unstable. In the selected DUT and in the 10 kHz to 100 kHz frequency range, the additional phase shift was up to -50 degrees. It was also shown that with all ceramic capacitors, which tend to have series resonance frequencies above the converter's cross-over frequency, the gradient of phase shift is higher in the typical range of crossover frequencies, making the dynamic behavior and the transient response of the design more sensitive to component tolerances and component as well as layout changes.

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