DesignCon 2004, TecForum TF9

Thin and Very Thin Laminates for Power Distribution Applications: What Is New in 2004?

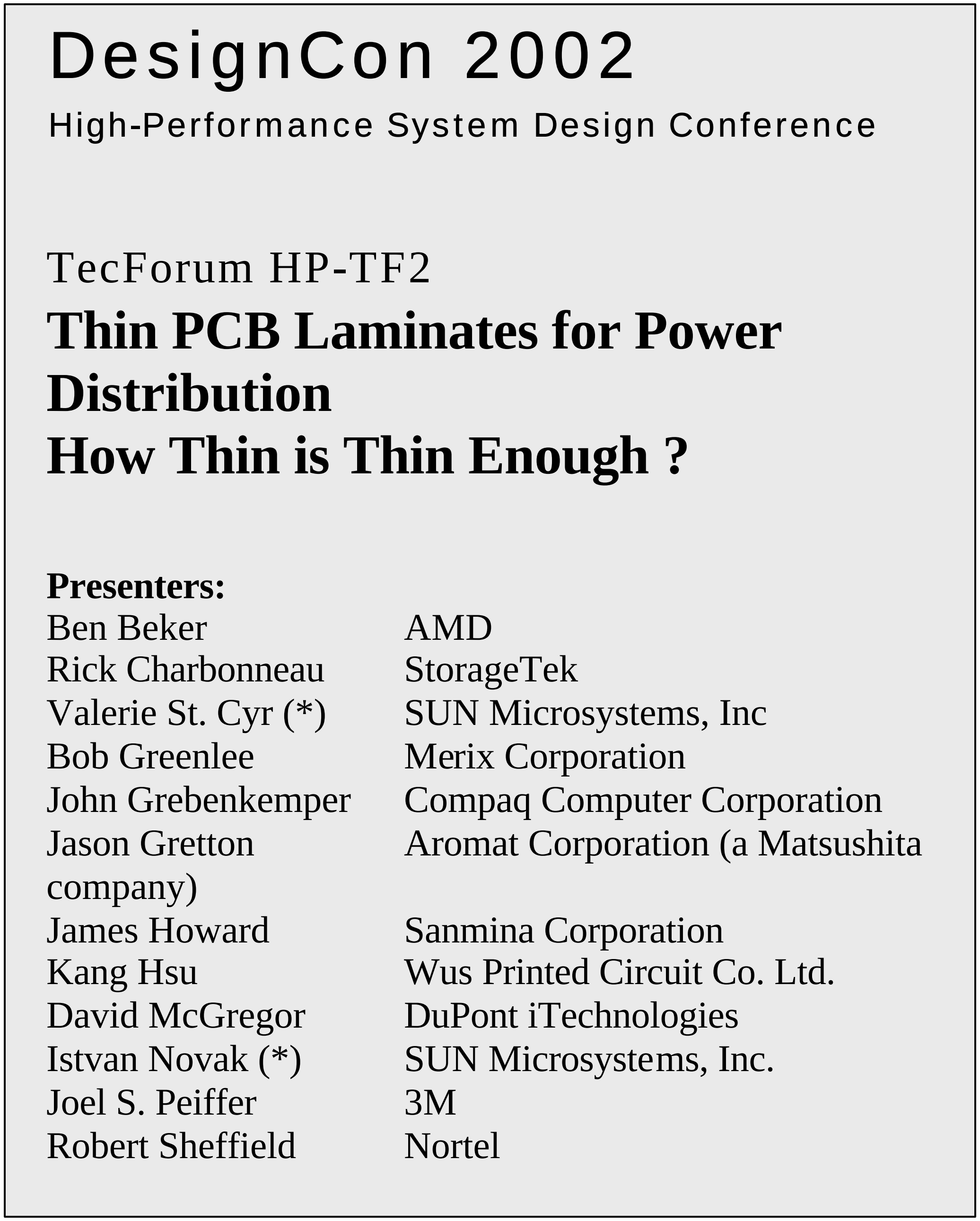
Frank Alberto	SUN Microsystems, Inc., ***session chair***
David McGregor	DuPont iTechnologies
Bill Balliette	3M Electronic Solution Division
John Andresakis	Oak-Mitsui Technologies, LLC
Cindy Gretzinger	Sanmina-SCI, Owego
Bob Greenlee	Merix Corporation
Lance P. Riley	Unicircuit, Inc.
Steve Patrick	Benchmark Electronics, Inc.
John Grebenkemper	NonStop Enterprise Division, Hewlett-Packard Company
Istvan Novak	SUN Microsystems, Inc.

Abstract

At DesignCon 2002, a TecForum titled "Thin PCB Laminates for Power Distribution: How Thin Is Thin Enough?" brought together five representative OEMs, three PCB fabricators, and three material suppliers to answer these questions: How thin is thin enough? When will these thin laminates be needed? Will the industry be ready? Since then there has been progress in the available laminates, in their agency approval status, and in the experience collected with them.

This TecForum reviews the thin laminate availability in 2004.

Background



DesignCon 2002

High-Performance System Design Conference

TecForum HP-TF2

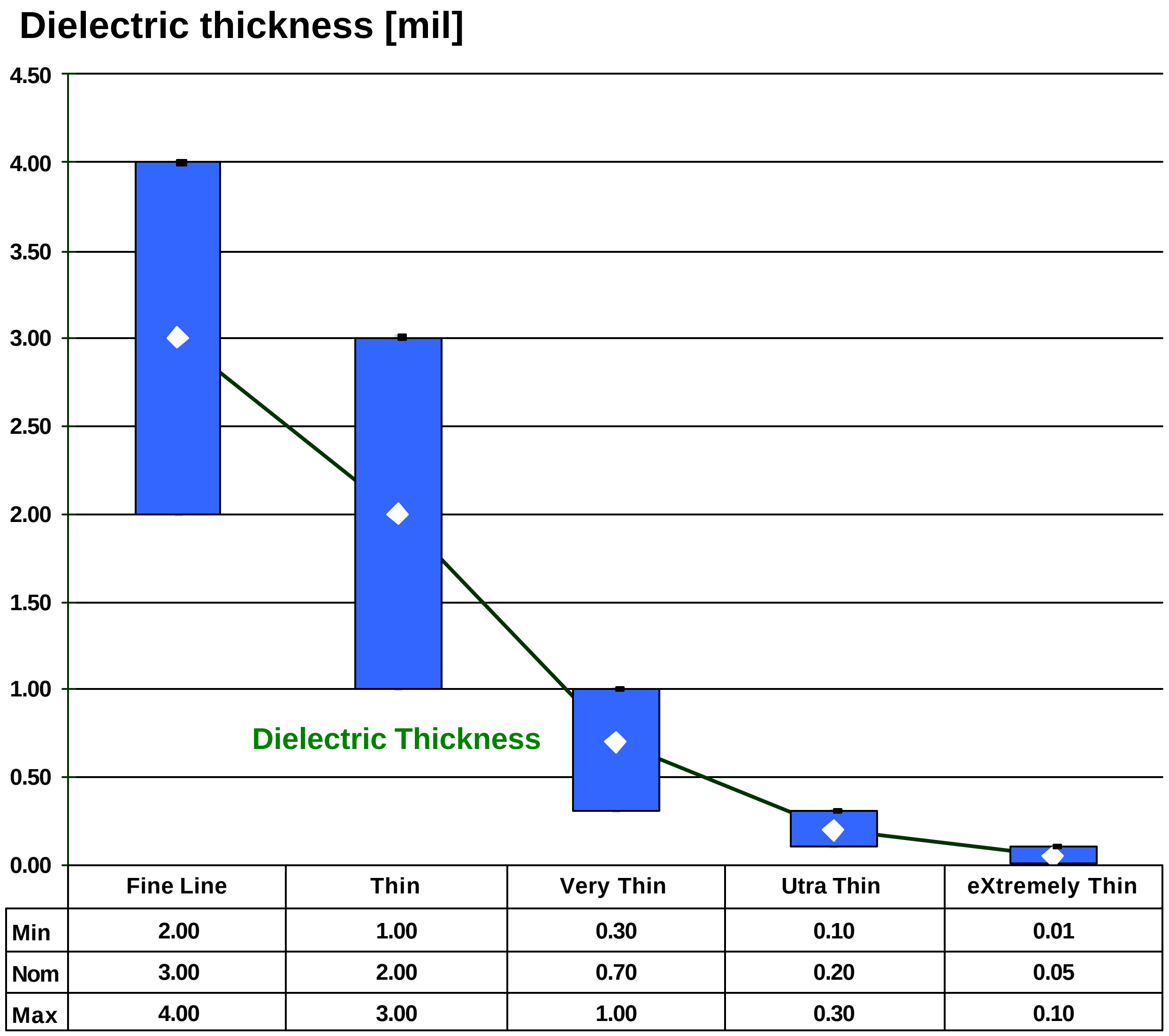
Thin PCB Laminates for Power Distribution

How Thin is Thin Enough ?

Presenters:

Ben Beker	AMD
Rick Charbonneau	StorageTek
Valerie St. Cyr (*)	SUN Microsystems, Inc
Bob Greenlee	Merix Corporation
John Grebenkemper	Compaq Computer Corporation
Jason Gretton	Aromat Corporation (a Matsushita company)
James Howard	Sanmina Corporation
Kang Hsu	Wus Printed Circuit Co. Ltd.
David McGregor	DuPont iTechnologies
Istvan Novak (*)	SUN Microsystems, Inc.
Joel S. Peiffer	3M
Robert Sheffield	Nortel

Thin Laminate Nomenclature

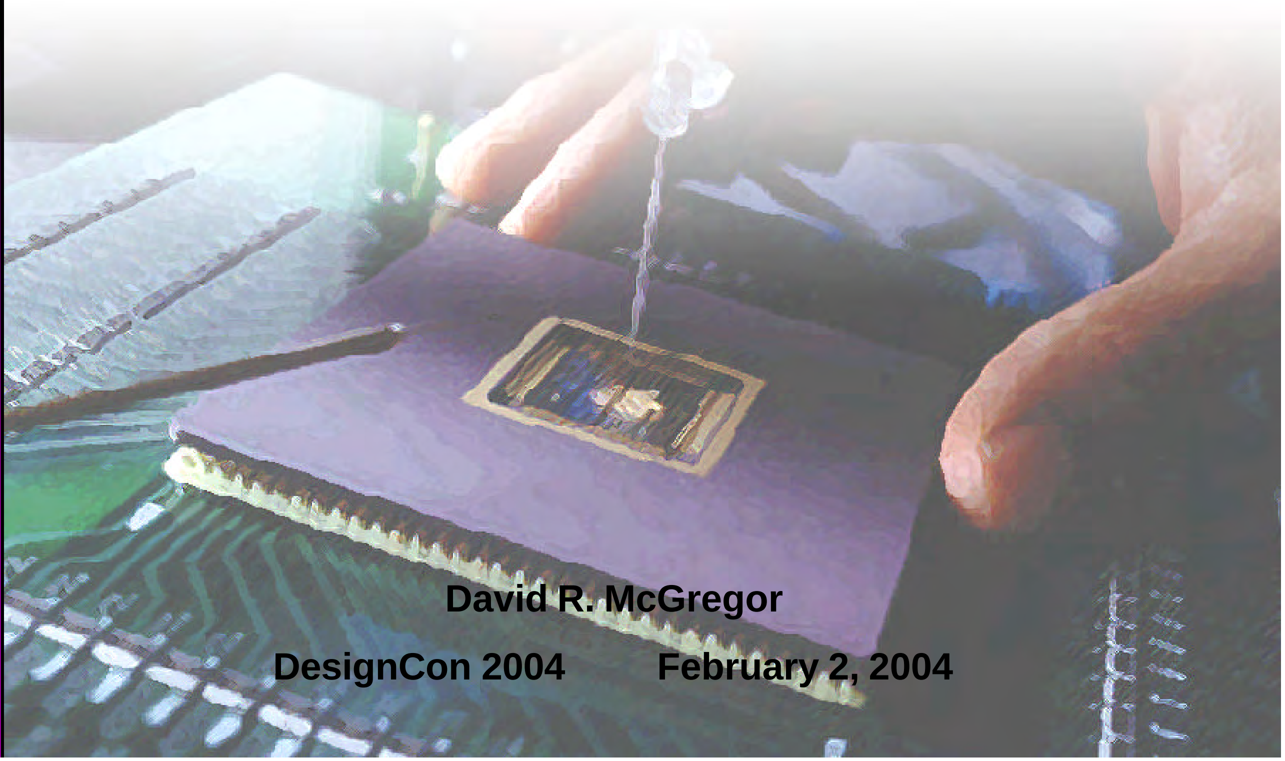


	Fine Line	Thin	Very Thin	Utra Thin	eXtremely Thin
Min	2.00	1.00	0.30	0.10	0.01
Nom	3.00	2.00	0.70	0.20	0.05
Max	4.00	3.00	1.00	0.30	0.10

The miracles of science

DuPont Electronic Technologies

Thin and Very Thin Laminates



David R. McGregor

DesignCon 2004 February 2, 2004

Planar Capacitor Thin Laminates

Available Laminates

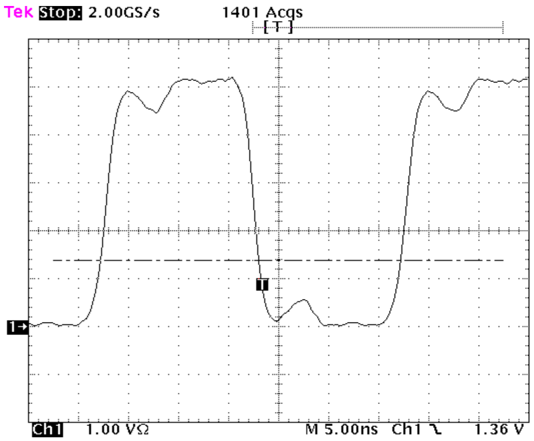
- 18* and 25 μ unfilled laminates
- 14 and 25 μ filled laminates

* Developmental

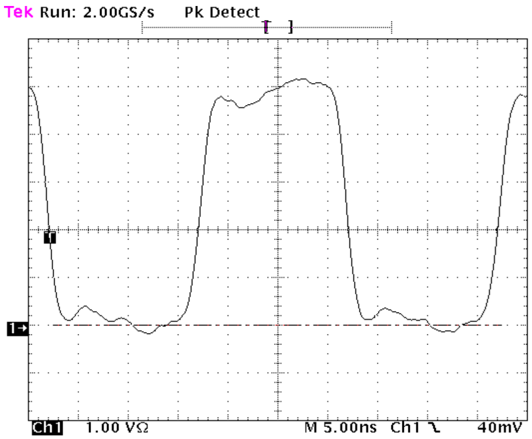
Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Impact of Thin Laminate on SMT Capacitor Removal

- High Speed Video board made conventionally and with 25 micron unfilled polyimide laminate.
- Removed over 400 bypass capacitors on thin laminate board.
- Board operated identically without these capacitors when using the thin laminate (Active devices worked as designed, radiated EMI improved, signal noise reduced).



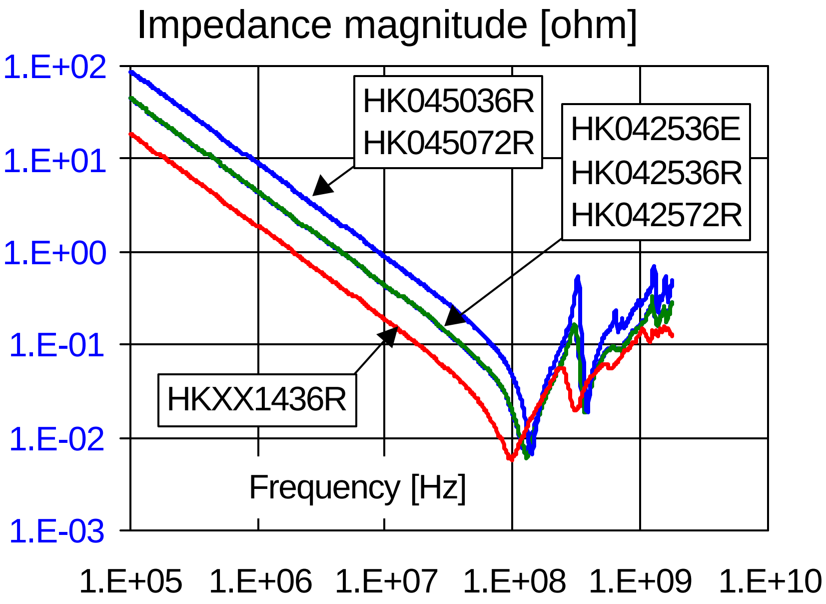
Conventional Board with SMT Caps

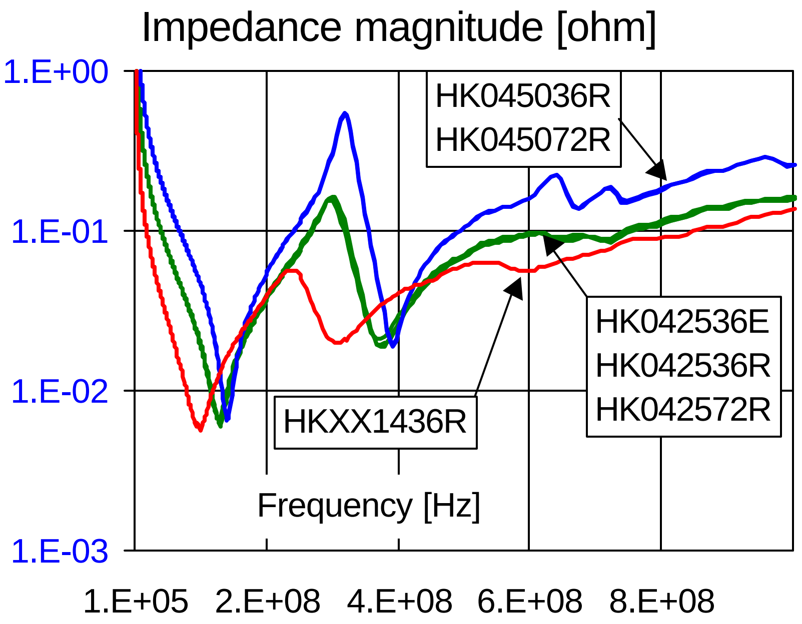


Board with thin laminate and SMT Caps Removed

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Thinner Dielectric Reduces Impedance

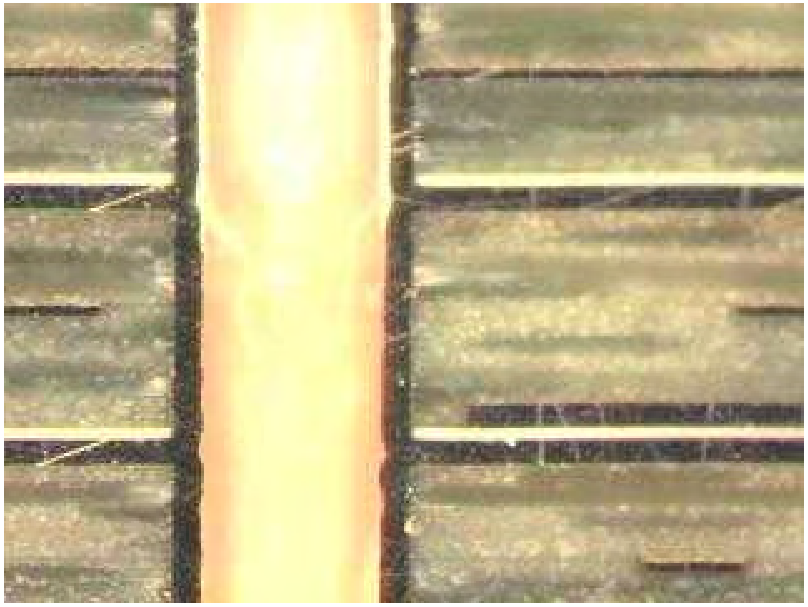




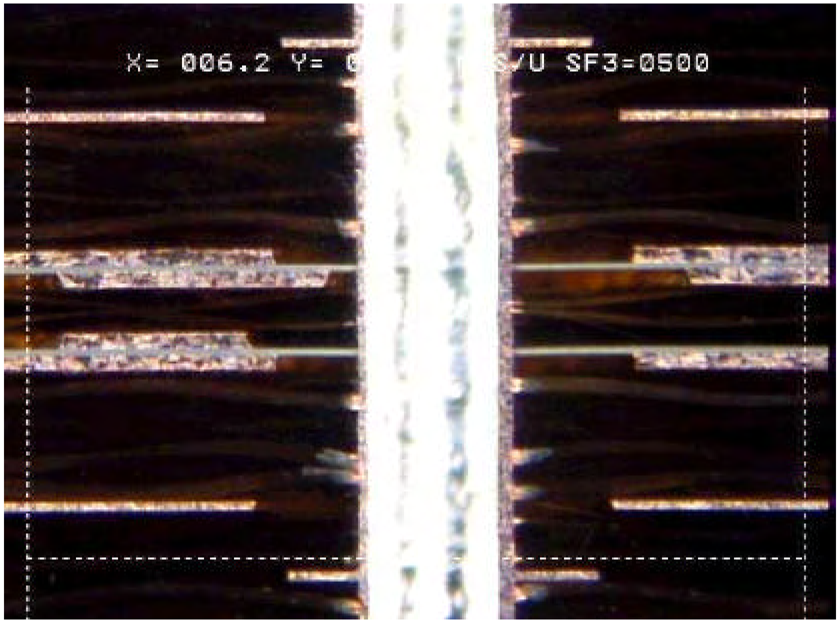
Courtesy of Sun Microsystems

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Interra™ HK 111436R



Courtesy EIT



Courtesy Merix

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Unfilled Thin Laminate:
Interra™ HK 04

Physical Properties:

Dielectric:	Polyimide
Peel Strength:	10 pli
CTE:	25 ppm/°C
Water Absorption:	0.8% (100% RH for 48 hours)
UL	
Flammability:	UL94 V-0
RTI, mech/elec:	200° C / 240° C
Dissimilar Materials w/FR-4:	Complete. This test not required for fabricator.
Debond/Delam:	This test required to be done by each fabricator.

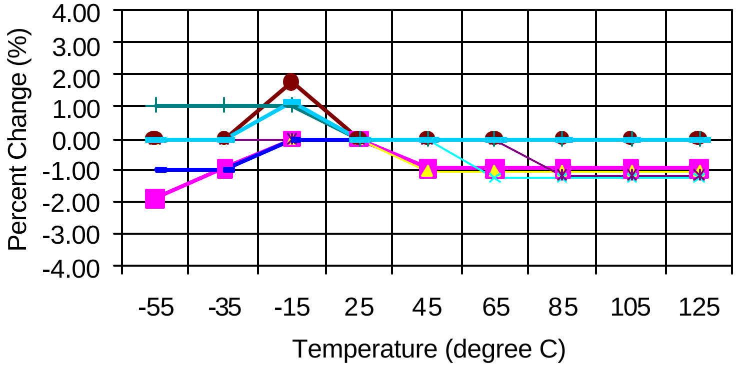
Electrical Properties:

Dielectric Constant:	3.4
Capacitance Density:	0.8 nF/in^2 (measured at 1 MHz)
Dissipation Factor:	0.003 (measured at 1 MHz)
Breakdown Voltage:	6000 Volts/mil
HiPot Voltage:	>1500 Volts DC

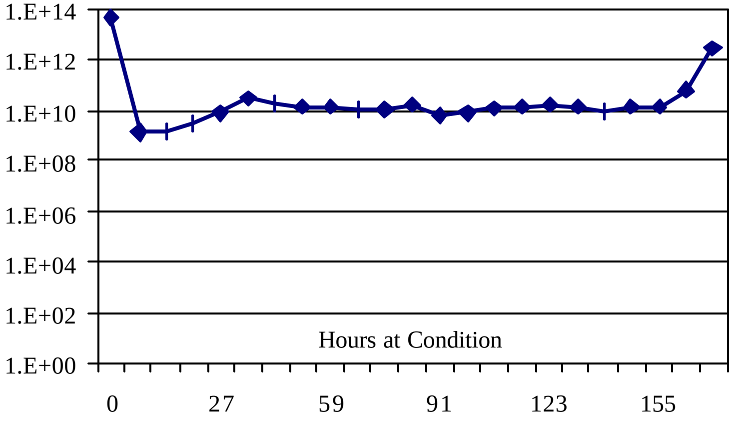
Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Unfilled Thin Laminate: Interra™ HK 04

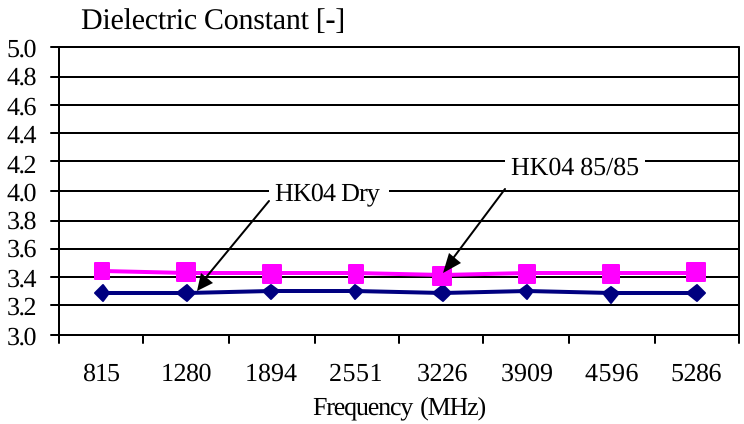
Temperature Coefficient of Capacitance for Interra(tm) HK 04

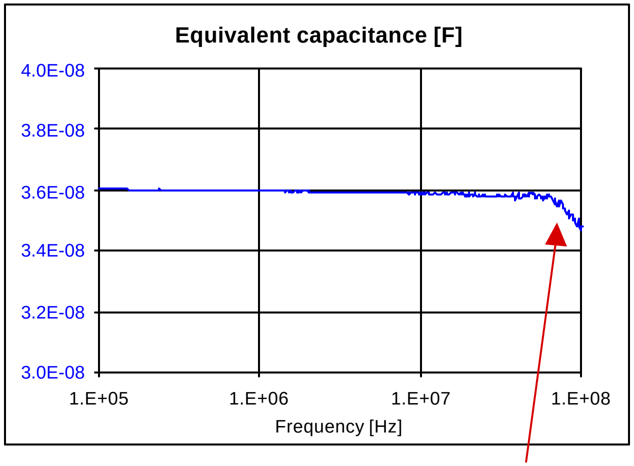


Moisture and Insulation Resistance Interra(tm) HK 04 [ohm]



Moisture Effect on Dk





Courtesy of Sun Microsystems

Measurement artifact

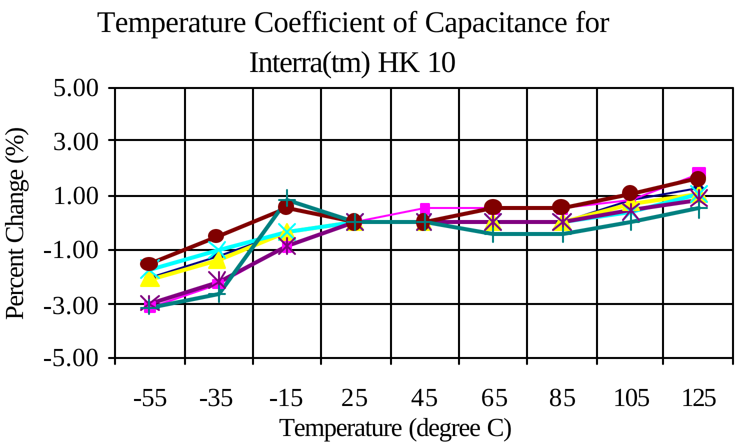
Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

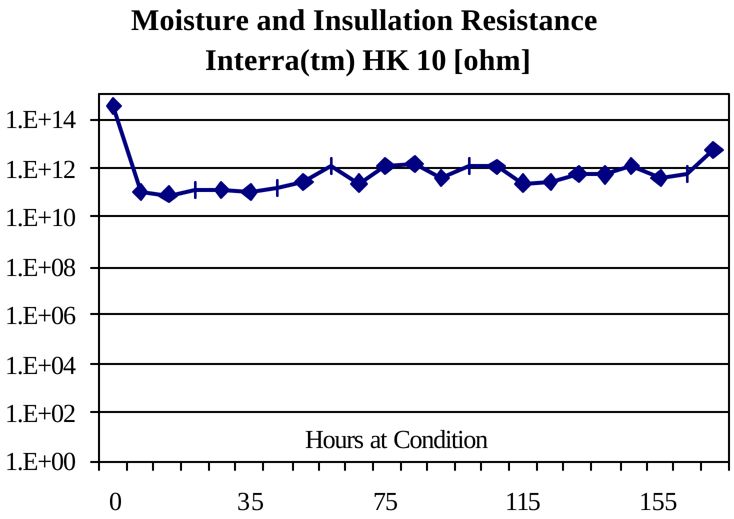
Filled Thin Laminate:
Interra™ HK 10

Physical Properties:	
Dielectric:	Polyimide with Barium Titanate Filler
Peel Strength:	8 pli
CTE:	46 ppm/°C
Water Absorption:	0.7% (100% RH for 48 hours)
UL	
Flammability:	UL94 V-0
RTI:	130° C
Dissimilar Materials w/FR-4:	Pending.
Electrical Properties:	
Dielectric Constant:	10
Capacitance Density:	2.2 nF/in^2 (measured at 1 MHz)
Dissipation Factor:	0.01 (measured at 1 MHz)
Breakdown Voltage:	3100 Volts/mil
HiPot Voltage:	250 Volts DC

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Filled Thin Laminate: Interra™ HK 10





Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Filled Very Thin Laminate:
Interra™ HK 11

Physical Properties:

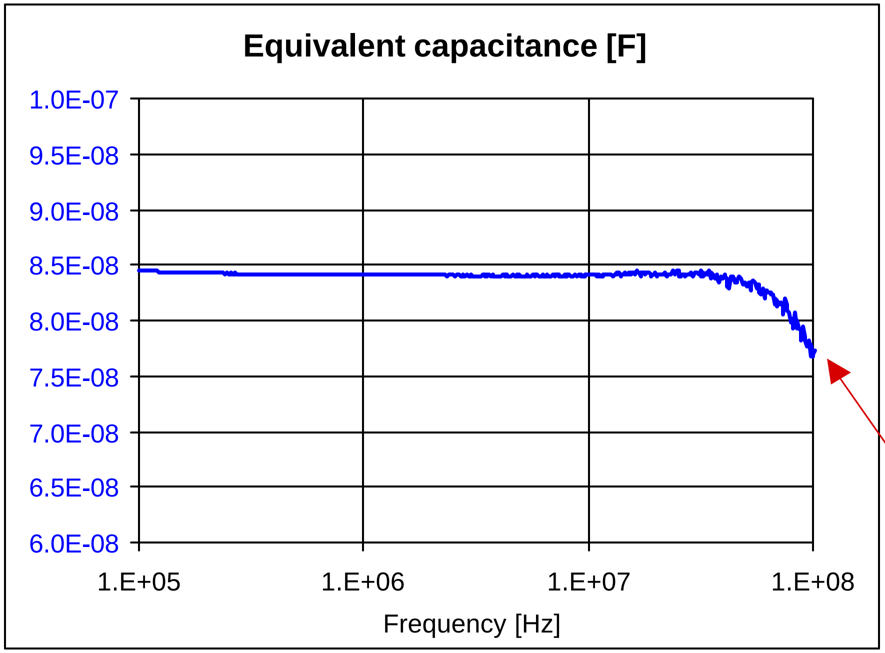
Dielectric:	Polyimide with Barium Titanate Filler
Peel Strength:	13 pli
Water Absorption:	0.5% (100% RH for 48 hours)
UL	
Flammability:	UL94 V-0
RTI:	130° C
Dissimilar Materials w/FR-4:	Pending.

Electrical Properties:

Dielectric Constant:	11
Capacitance Density:	4.5 nF/in^2 (measured at 1 MHz)
Dissipation Factor:	0.02 (measured at 1 MHz)
Breakdown Voltage:	2500 Volts/mil
HiPot Voltage:	100 Volts DC

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Filled Very Thin Laminate: Interra™ HK 11



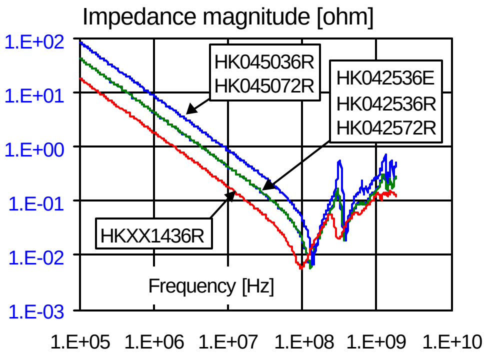
Measurement artifact

Capacitance Response with Increasing Frequency

Courtesy of Sun Microsystems

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Planar Capacitor Highlights

Excellent overvoltage protection	Unfilled > 6000 V BDV > 1500 V HiPot
High capacitance density	HK 11 = 4.5 nF/in^2 (0.7 nF/cm^2)
Low impedance	
Reduced EMI	
Excellent peel strength	All > 6 pli
Frequency Response	Capacitance stable with frequency
Significant product history	HK 04 built on Pyralux® AP technology
Commercial products	3 commercial laminates; 1 in development

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

Summary

- Planar capacitor laminates are commercial products offering superior overvoltage protection, high capacitance density, reduced impedance, and high reliability.

Copyright © 2002 E.I. du Pont de Nemours and Company. All rights reserved.

DUPONT®

The miracles of science™

Ultra-Thin, Loaded Epoxy Materials for Use as Embedded Capacitor Layers

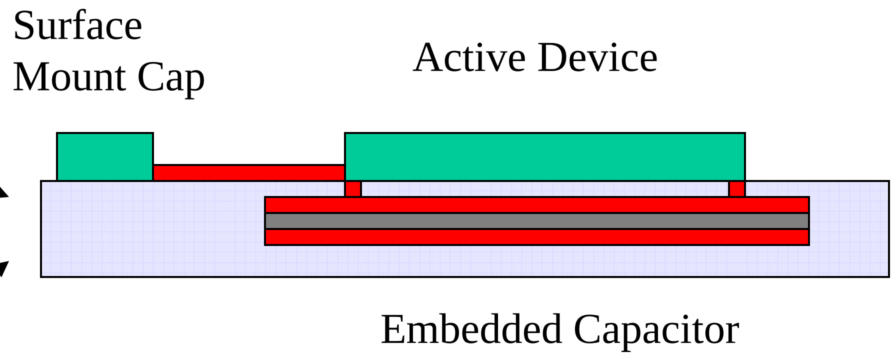
Bill Balliette
3M - Austin
(512) 984-7324
wmballiette@mmm.com

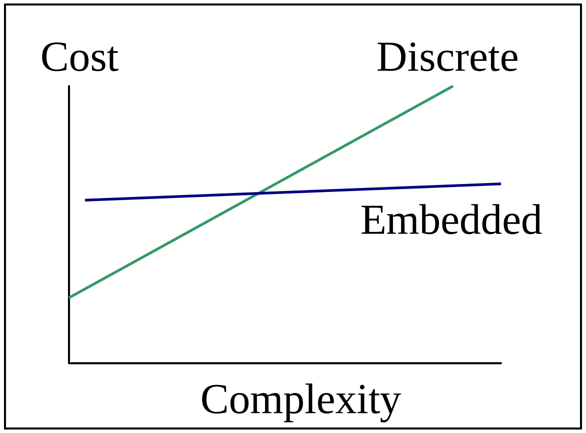
Why Embedded Capacitance?

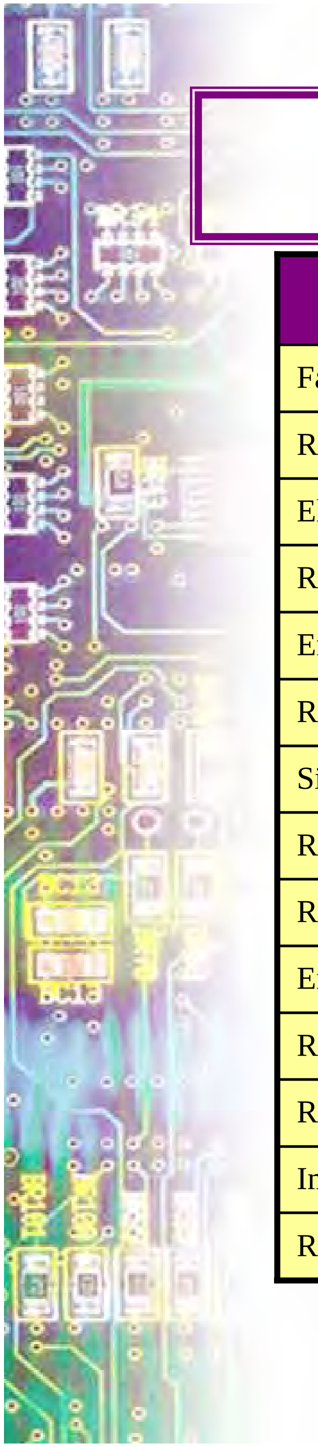
1. Performance

2. Space

3. Cost

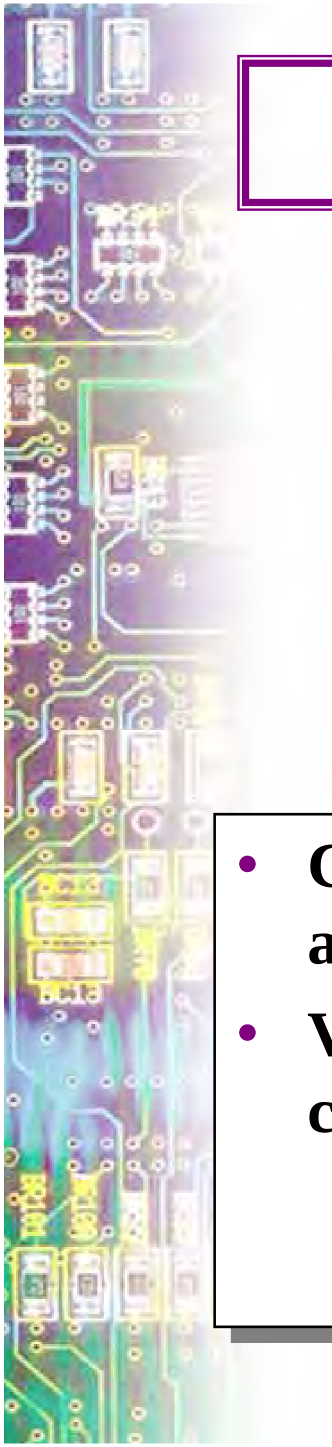




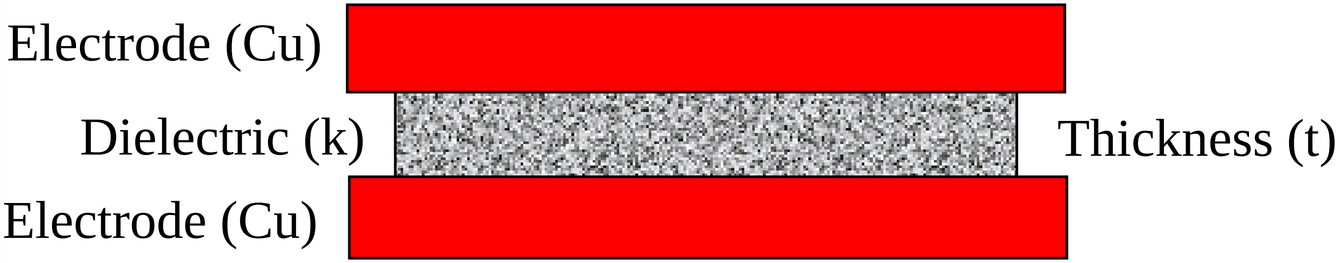


Reasons for Embedded Capacitance

Potential Benefits	Performance	Space	Cost
Faster signaling/Reduce power bus noise	√		
Reduce design time & redesigns	√		√
Eliminate capacitors		√	√
Reduce layer count			√
Enable DS to SS assembly			√
Reduce via count		√	√
Simplify rework			√
Reduce board size, thickness		√	
Reduce assembly time			√
Enable decoupling w/back-side heat sinks	√		
Reduce weight	√		
Reduce opportunities for damaged components	√		√
Improve PWB panel utilization			√
Reduce EMI	√		√



Thin-Film Capacitor Technology



Electrode (Cu)

Dielectric (k)

Thickness (t)

Electrode (Cu)

- **Capacitance per unit area (C/A) is proportional to k and inversely proportional to t**
- **Vary C/A by varying thickness (t) or dielectric constant (k)**

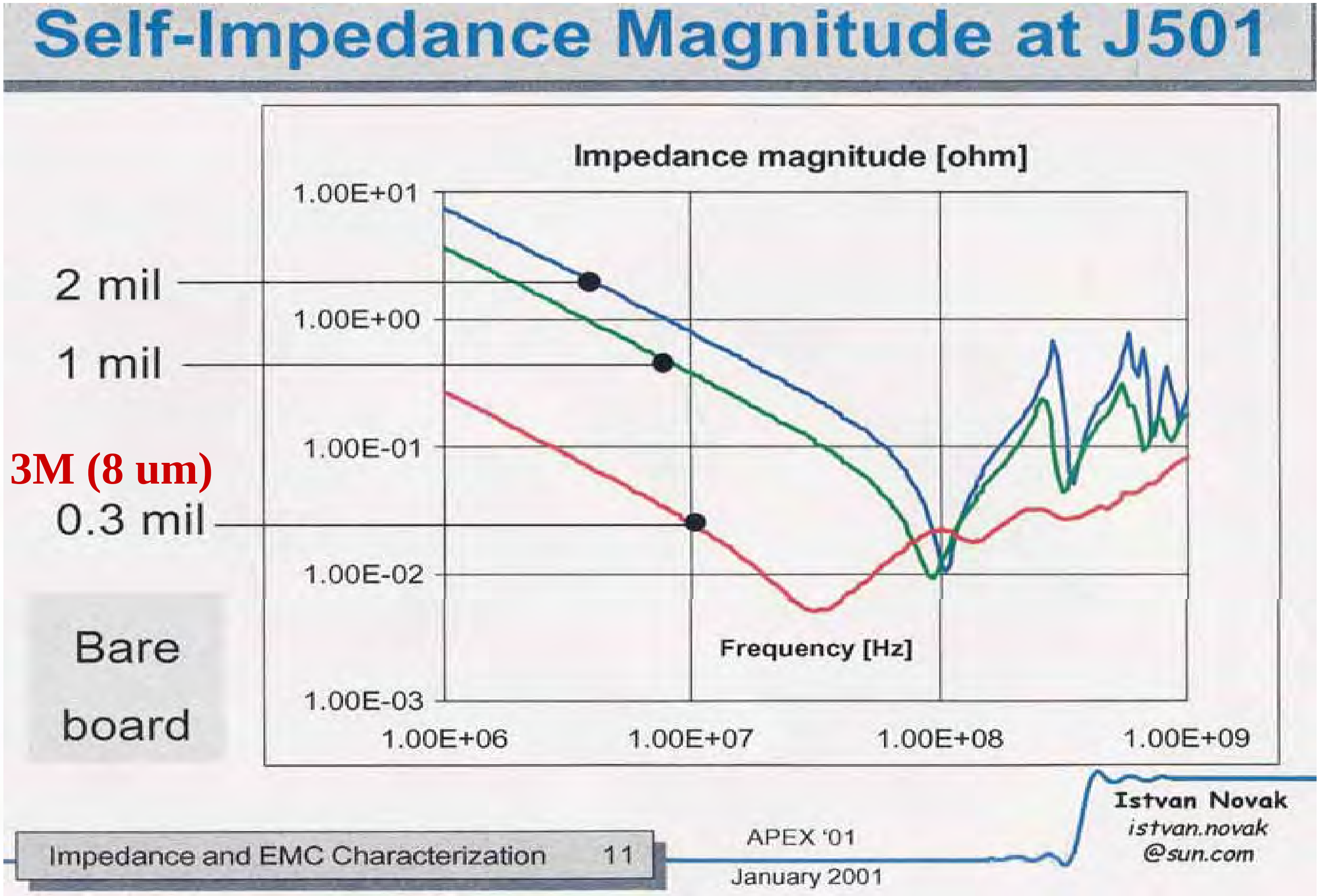
3M^{TM} Embedded Capacitor Material Key Properties

Attribute	Value
Capacitance /area	5.5 nF/in2*
Dielectric Constant	16
Dielectric loss @ 1GHz	0.03
Resin system	Epoxy, ceramic filler
Freq., Voltage, Temperature	Meets X7R
Dielectric Strength	~130V/um
Breakdown Voltage	>100V**
Copper Thickness	35 um
Flammability Rating	94V-0

*** For 16 um dielectric thickness. Thinner dielectrics in development**

**** Higher breakdown voltages in development**

Impedance Comparison



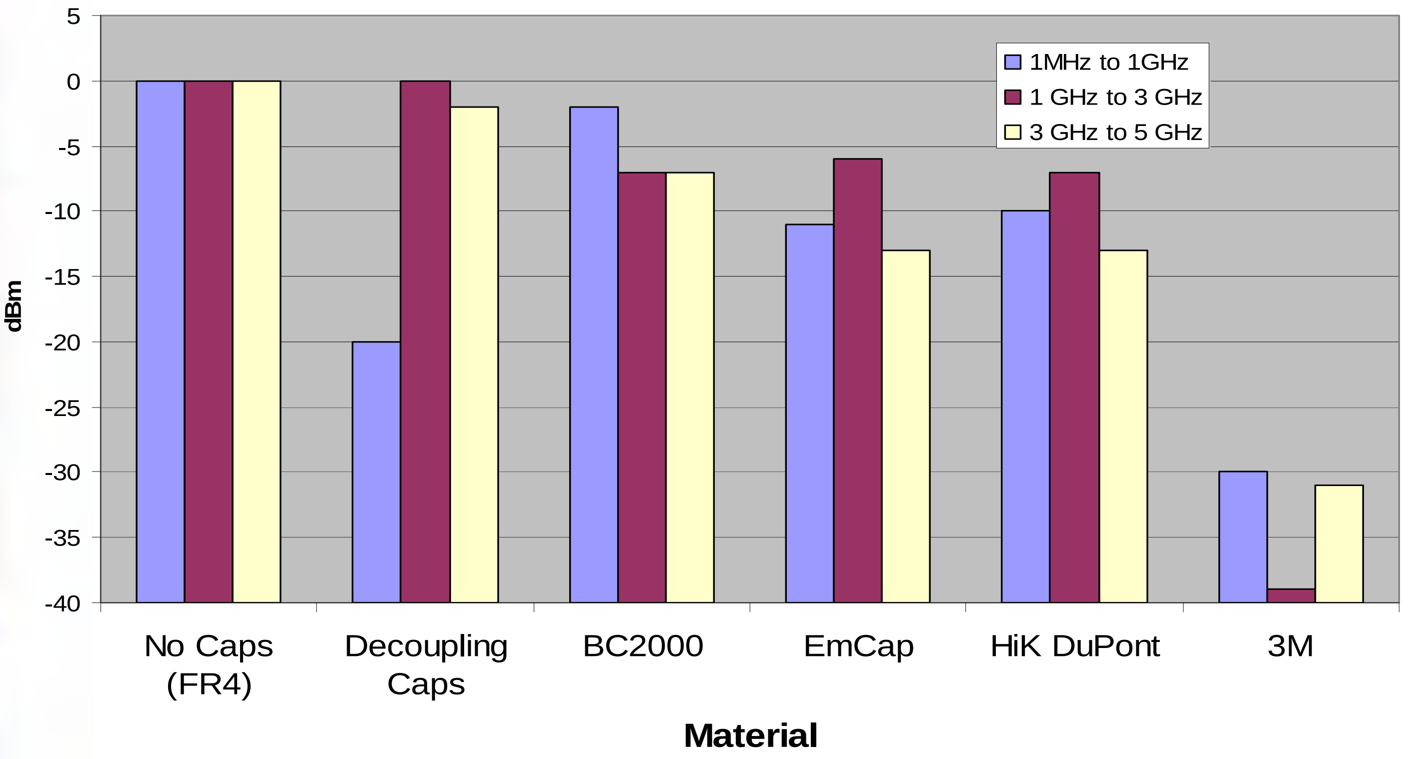
Self-Impedance Magnitude at J501

Impedance and EMC Characterization 11

APEX '01
January 2001

Istvan Novak
istvan.novak
@sun.com

Power Bus Noise on Test Vehicle



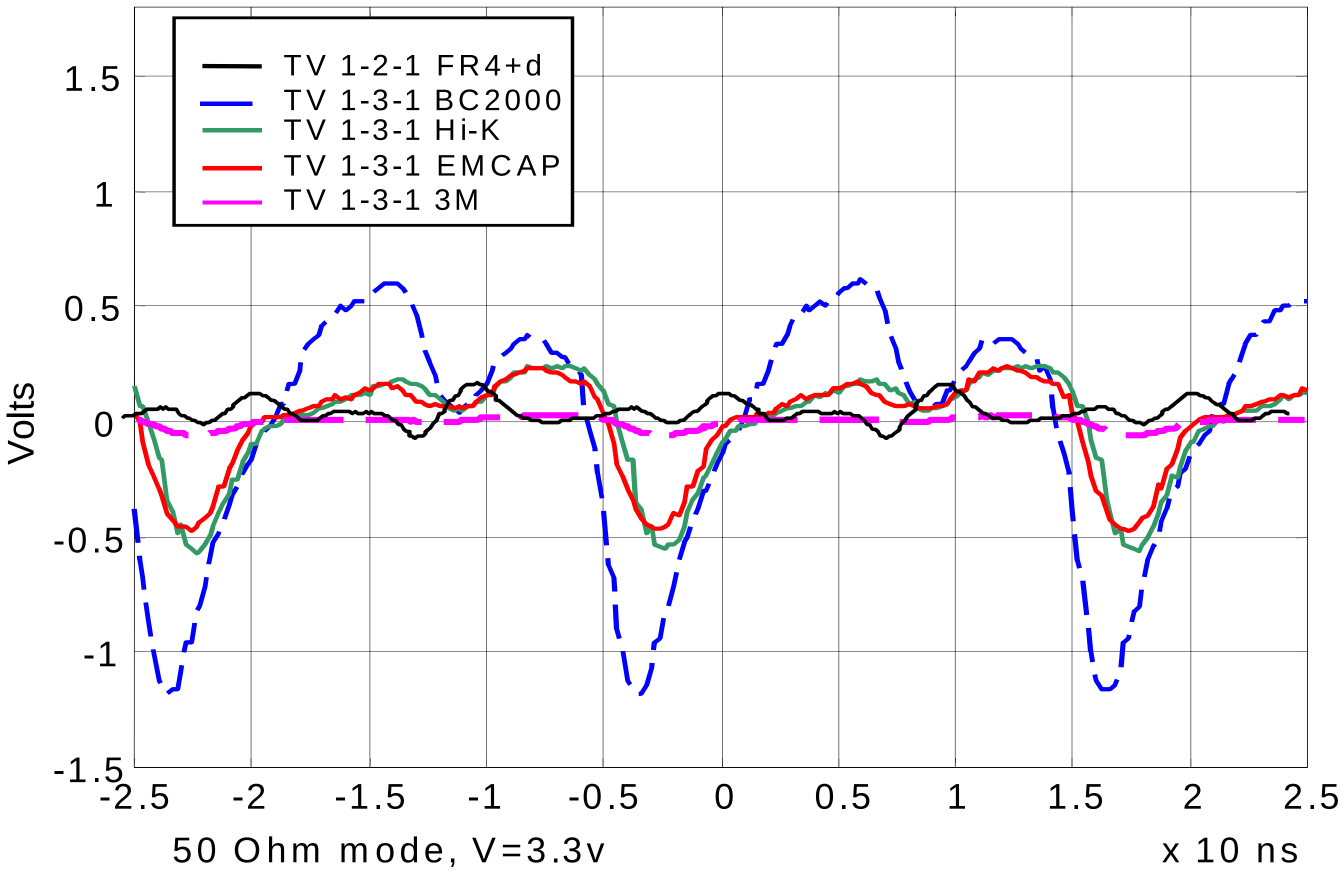
Less Noise

- **Traditional decoupling capacitors are not effective at frequencies above 1 GHz**
- **3M has excellent performance to 5 GHz**

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

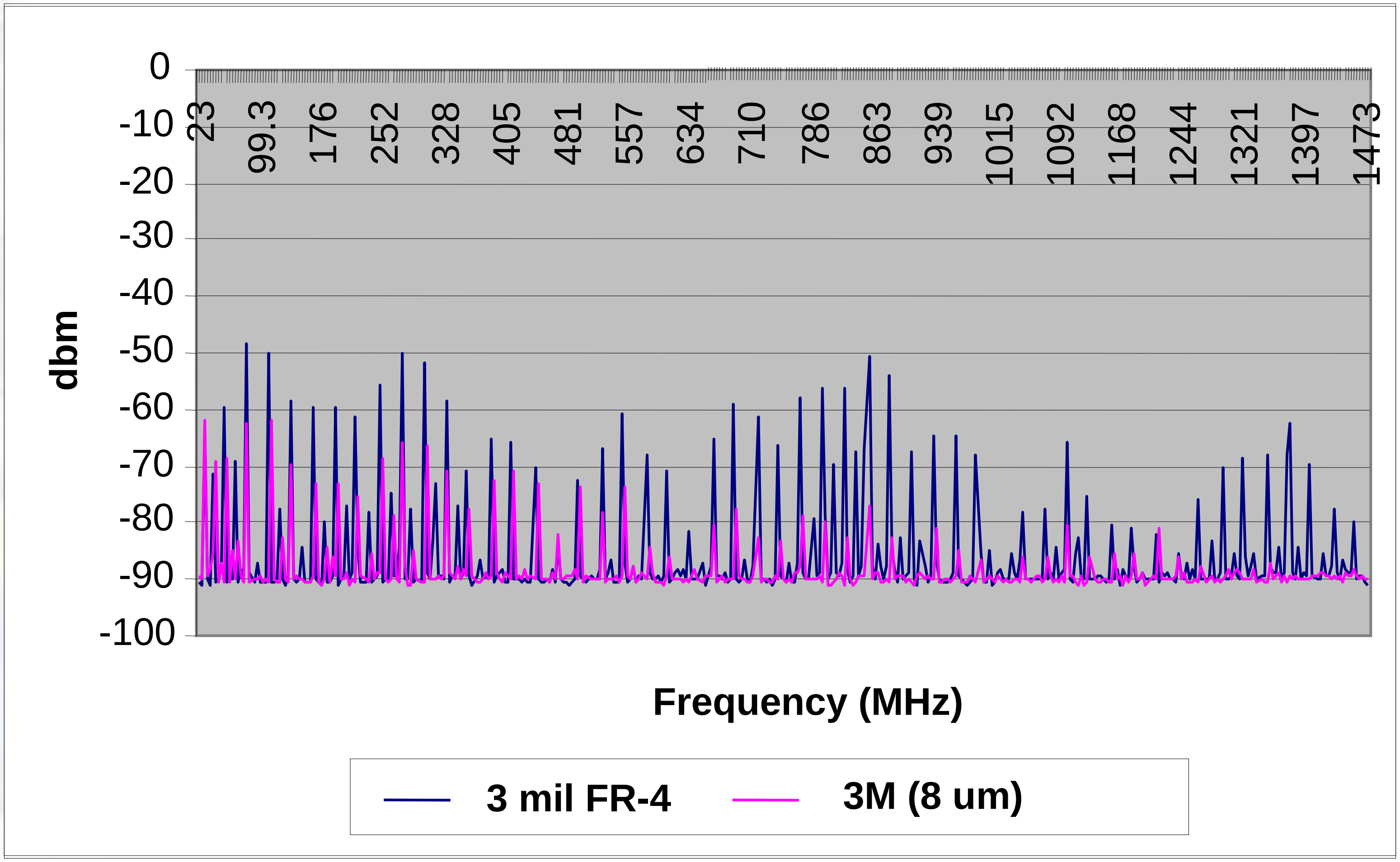
Power Bus Noise

(Time Domain - 50 MHz)

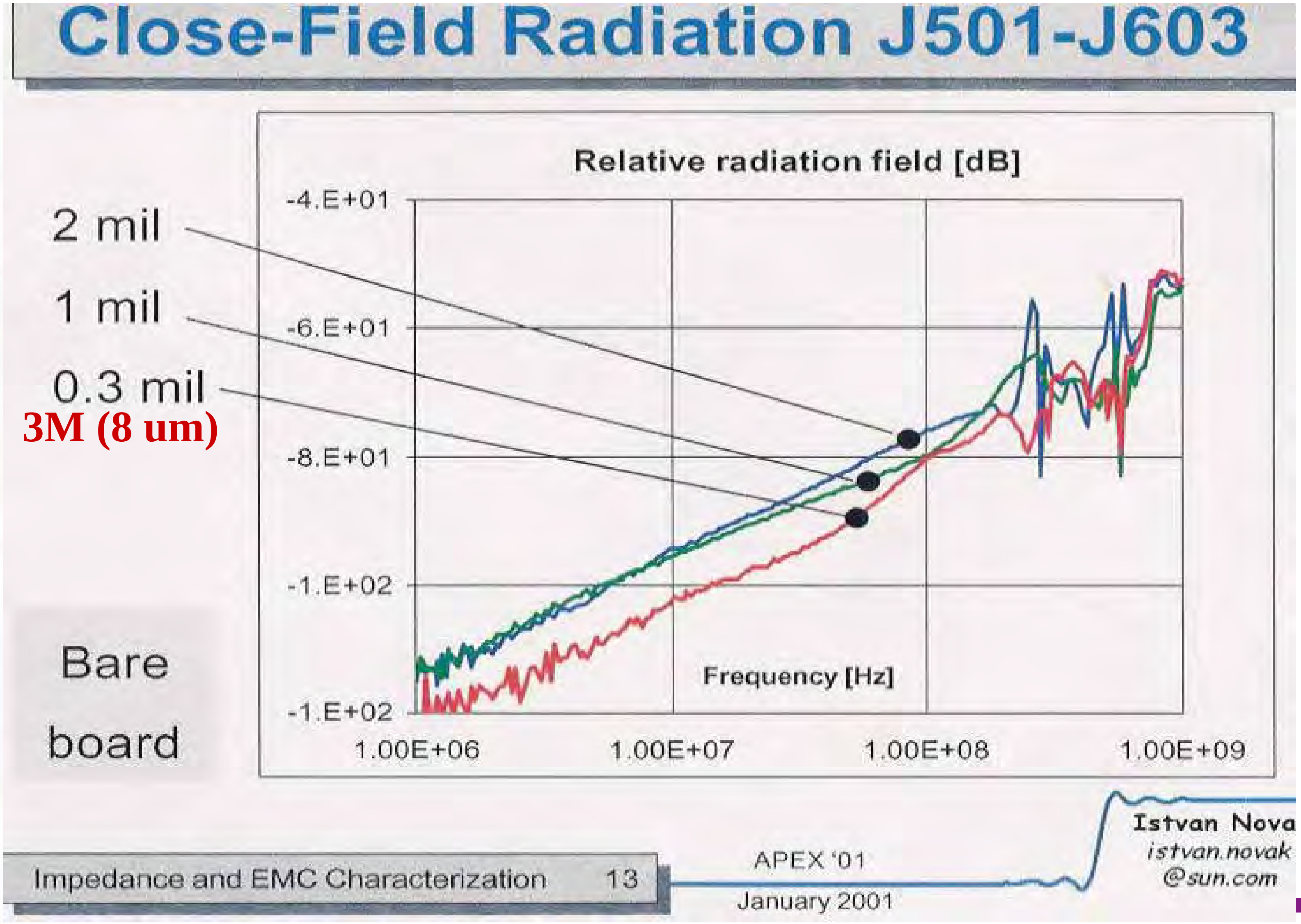


Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

Power Bus Noise vs. Frequency (H.P.)



Radiated Emissions Comparison



Close-Field Radiation J501-J603

3M (8 um)

Impedance and EMC Characterization 13

APEX '01

January 2001

Istvan Nova

istvan.novak

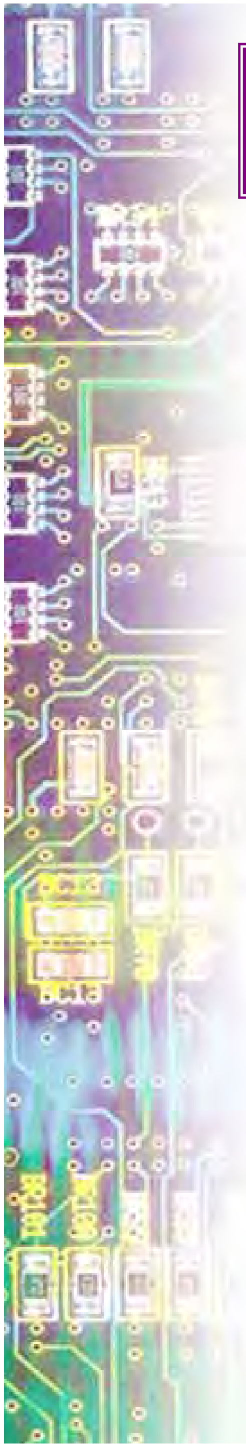
@sun.com

Examples of Embedded Capacitance Replacing Discretes

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Capacitance Removed
EDC TV1	**330** *33 x 0.01 uF*	**105**	**3.1**	**100%**
OEM A	**12,600** *126 x 0.1 uF*	**300**	**42.0**	**NA**
OEM B	**6,310** *62 x 0.1 uF* *11 x 0.01 uF*	**210**	**30.0**	**>60%**
OEM C	**3,180** *29 x 0.1 uF* *28 x 0.01 uF*	**~300**	**~10.6**	**>75%**
OEM D	**52,900** *529 x 0.1 uF*	**1969**	**26.9**	**>75%**

Benefits of Embedded Capacitance for Power-Ground Decoupling

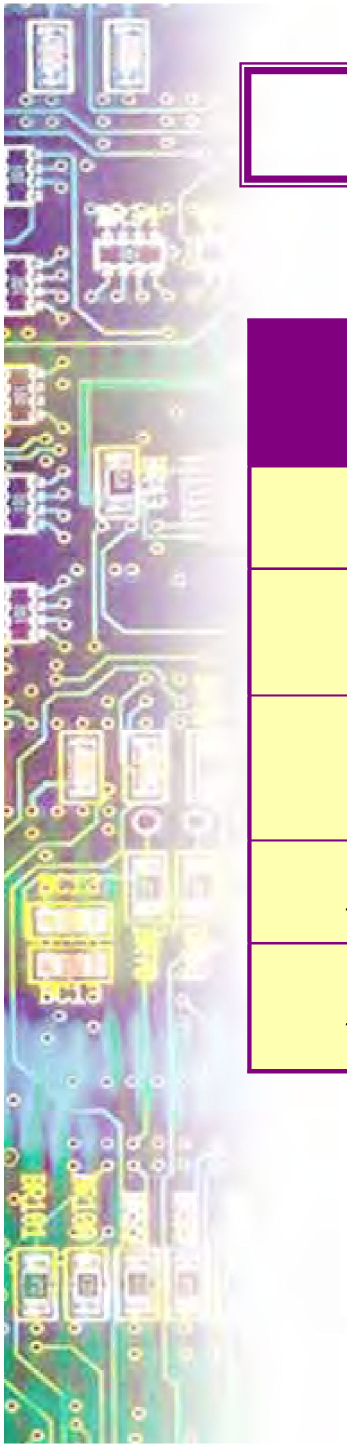
- Lowers impedance of power distribution system
- Dampens board resonances
- Reduces noise on power plane
- Reduces radiated emissions
- More effective than discrete capacitors for decoupling high frequencies. Can replace large numbers of capacitors in high speed digital designs



Environmental Testing

Test	*Property*	*Result*
High Temp (125°C)	Capacitance	No Change (1000 hrs)
Thermal Cycle Thermal Shock	Capacitance	No Change (1000 cycles)
High Humidity (85°C/85% RH)	Capacitance Dissipation Factor	10-15% Increase* 0.4% to 0.9%*
TMA (T260)	Life	>5 minutes
THB **(85C/85%RH/15 V)**	Life	>1000 hrs
ESD (2-25 kV)	Capacitance/D.F.	No change
Bend Test	Capacitance	No change (200 cycles)
Multiple Reflow (3X)	Capacitance	No change

***Returned to pre-test level after bake**



UL Testing

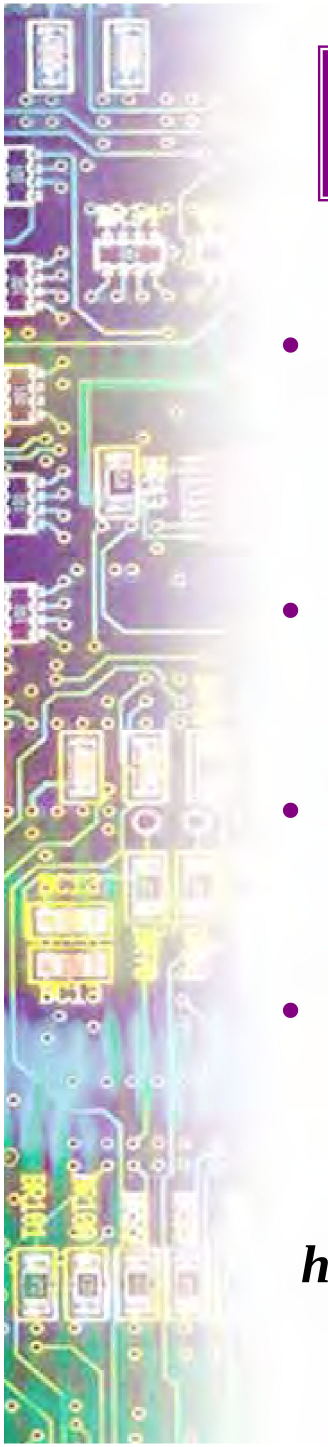
Test	***Property***	***Result***
Laminate	Flammability	94V-0
Laminate	Solderability Limits	288C/30 sec
Laminate	Relative Thermal Index	130C
Board (Merix)	Flammability	94V-0
Board (Merix)	Max Operating Temp	130C

PCB Processing - 1

- Compatible with all rigid and flex PCB processing (including laser ablation)
- Material handling is most significant issue (compares to bare 2 ounce copper)
- A sequential lamination process is recommended
  - Pattern 1st side copper
  - Laminate patterned side to another layer of prepreg
  - Pattern 2nd side copper

PCB Fabrication - 2

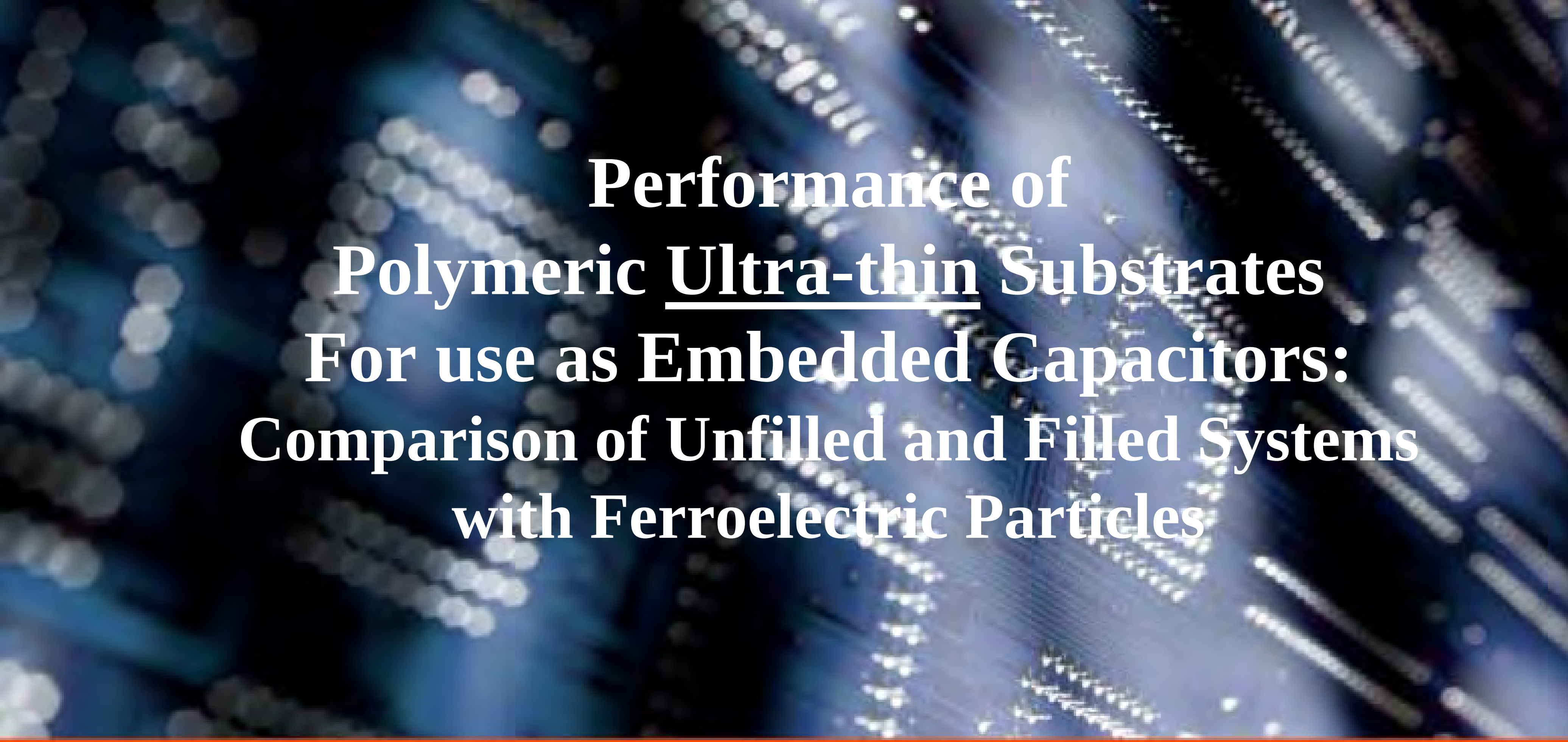
- If a sequential lamination process is utilized, there are no design limitations
- Many high end fabricators have successfully fabricated numerous prototype lots
  - Over 25 board designs have been manufactured by a dozen fabricators for 17 different OEMs
  - Additional fabricators have demonstrated process capability



Conclusion

- **3M Embedded Capacitance Material offers a high capacitance density of 5.5 nF/in2. (Future products will offer even higher capacitance density.)**
- **Delivers many electrical benefits when used for power-ground decoupling**
- **Compatibility with fabrication has been demonstrated multiple times**
- **The product is available for sale, has UL approval, and can be manufactured in volume**

For more information:
http://www.3m.com/us/electronics_mfg/microelectronic_packaging/



Performance of Polymeric Ultra-thin Substrates For use as Embedded Capacitors:

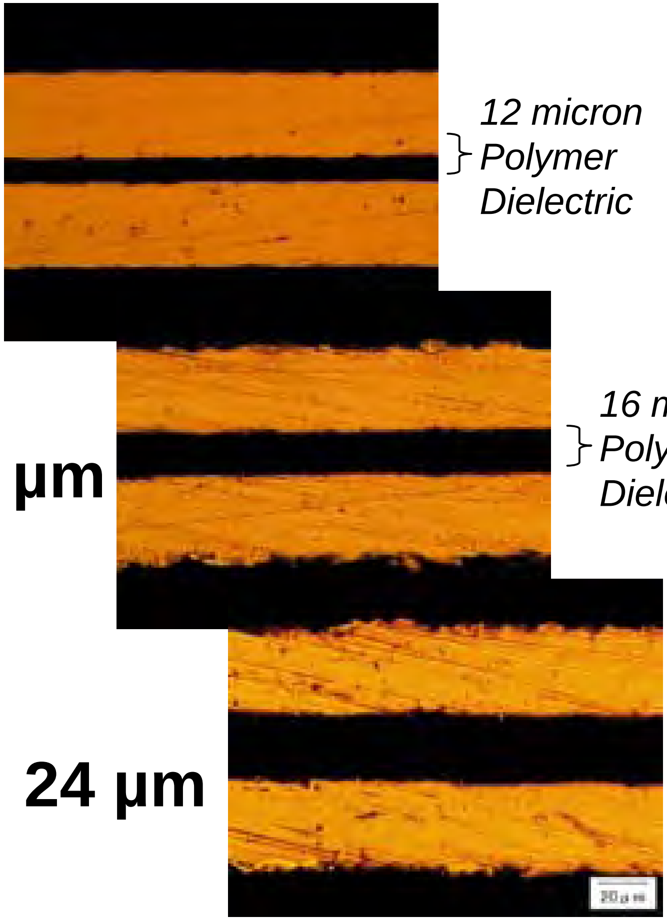
Comparison of Unfilled and Filled Systems with Ferroelectric Particles

John Andresakis, Takuya Yamamoto, Pranabes Pramanik
Oak-Mitsui Technologies,LLC
Nick Biunno
Sanmina-SCI Corporation

DesignCon 2004
February, 2004

Product Design

Construction



12 µm

12 micron Polymer Dielectric

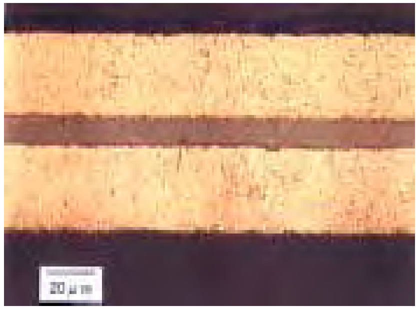
16 µm

16 micron Polymer Dielectric

24 µm

24 micron Polymer Dielectric

16 µm



16 micron Polymer Dielectric ***with Hi-Dk Filler***

(16 µm with Filler is under development)

-Standard Copper thickness is 35 µm

Product Data

Electrical Properties

Characteristics	Condition	Unit	24µm	16µm	12µm	8µm	16µm-Filler
Capacitance	1GHz	nF/cm^2	0.14	0.23	0.31	0.45	1.75
Dk	1GHz	N/A	4.4	4.4	4.4	4.4	30.0
Df	1GHz	N/A	0.015	0.015	0.015	0.016	0.019
Dielectric Thickness	Nominal	Micro-Meter	24	16	12	8	16

Product Data

Physical Properties

Characteristics	Condition	Unit	24µm	16µm	8&12µm	16µm-Filler
Tg	DMA	Celsius	200	200	200	200
Peel Strength	As received	lb/in	8.0	8.0	8.0	6.0
Young's Modules	JIS 2318	GPa	4.8	5.8	7.2	NA
Tensile Strength	JIS 2318	MPa	180	180	180	NA
CTE (x,y)	IPC TM650	PPM	23	23	28/23	TBD
Breakdown	1kV/sec	V	>5000	>4000	>4000	TBD
Insulation Reliability	85C/85%/35V	hr	>1000	>1000	>1000	>1000

NA- Not Applicable since material is not self supporting

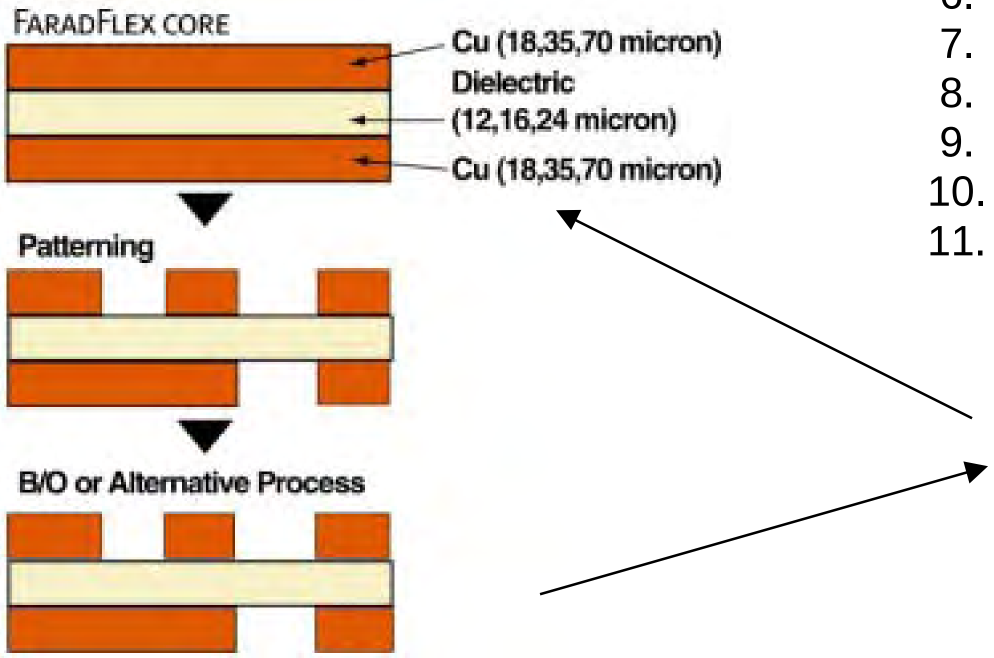
PWB Manufacturing Process

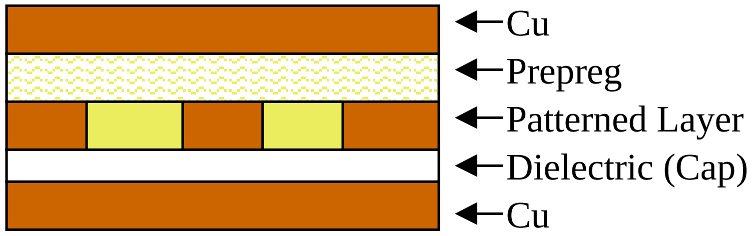
Thin Substrate without Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative

Thin Substrate with Particles

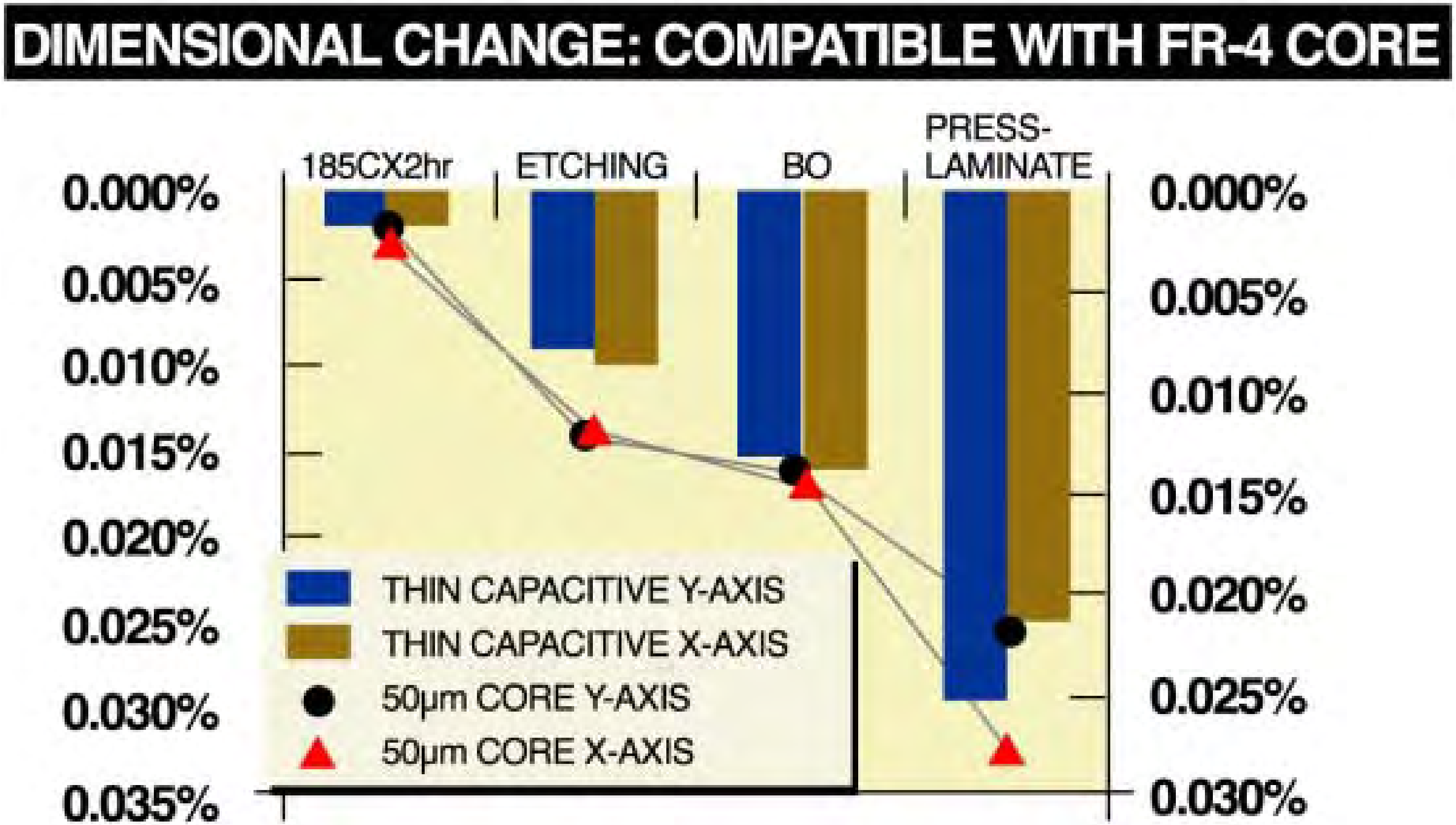
1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative





Subassembly

PWB Manufacturing Process



12 µm CAPACITOR

PWB Manufacturing Process

Summary of Unfilled Substrates (approx. 1200 panels)

- Substrates Processed at 10 Major PCB Facilities
- Standard I/L Processing
- Results
  1. **No loss** due to jams
  2. **No “blow out”** of Clearance holes
  3. **No separation** from border pattern
  4. **99+ % Yield (due to material issues)** at Hi-Pot (500 Volts)
  5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
- PWBs available from ZBC^{TM} Licensed Fabricators

ZBC^{TM} - Is a trademark of HSCI

PWB Manufacturing Process

Summary of Filled Substrates(<110 panels)

- Substrates Processed at 2 Major PCB Facilities
- Standard I/L Processing with additional steps
- Results
  1. **No loss** due to jams
  2. **No “blow out”** of Clearance holes
  3. **No separation** from border pattern(Cu to edges)
  4. **100 % Yield** at Hi-Pot (100 Volts) (limited quantity)
  5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
  6. **Registration between *buried* and outer core layers on subassembly critical**
- PWBs available from ZBC^{TM} Licensed Fabricators

ZBC^{TM} - Is a trademark of HSCI

Availability

- 12,16 and 24 micron unfilled materials are commercially available
- 1 oz. Copper is standard and can be delivered quickly (other copper weights will take longer initially until inventory established)
- 8 micron unfilled and 16 micron filled materials available for testing (commercially available by 2Q04)

Cost/ft^2

- Quotes available upon request
- Competitive with other sub 1 mil materials
- Price reductions in future based on production optimization and reduced raw material prices.

Reliability Tests

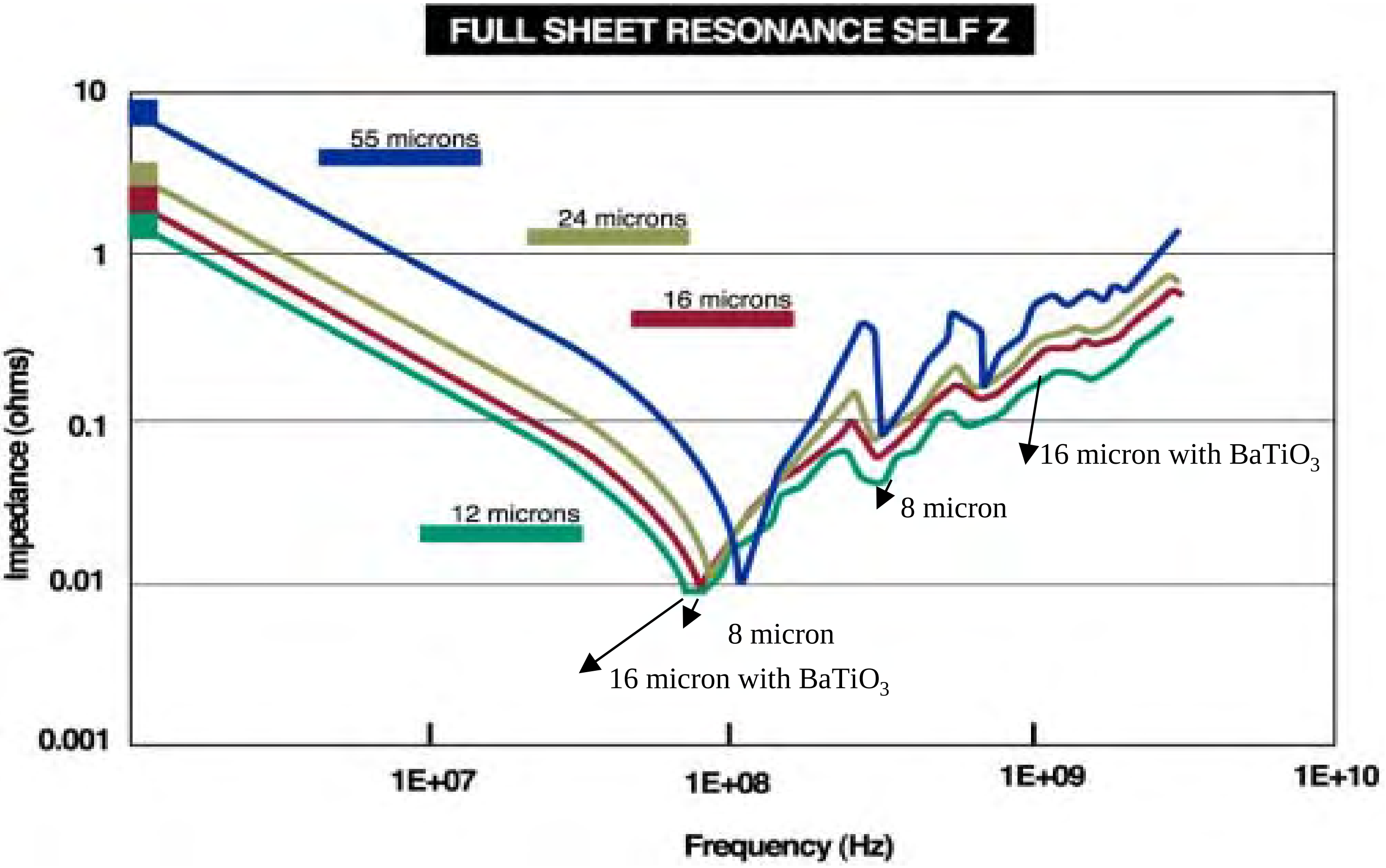
- Dielectric Withstanding Voltage : 500V Passed, No failure
- T-260 Time to Delamination : 1*2 µm-* 6.3min, *24 µm-* 5.2min
- Blind Via Plating Defects : No defects found
- Thermal Solder Shock (288^{o}C)– 10x : No defects found
- Liquid-Liquid : *24 µm* 4.2%(500 cycle)
- IST Testing: Passed 500 Cycles

Approvals

- Unfilled 12, 16 and 24 micron materials are UL approved (94VO, 130 Operating Temp.)
- PCB Shops submitting their UL samples (2 already submitted)
- Telcordia samples being prepared
- 8 micron unfilled and 16 micron filled materials are in for UL approval

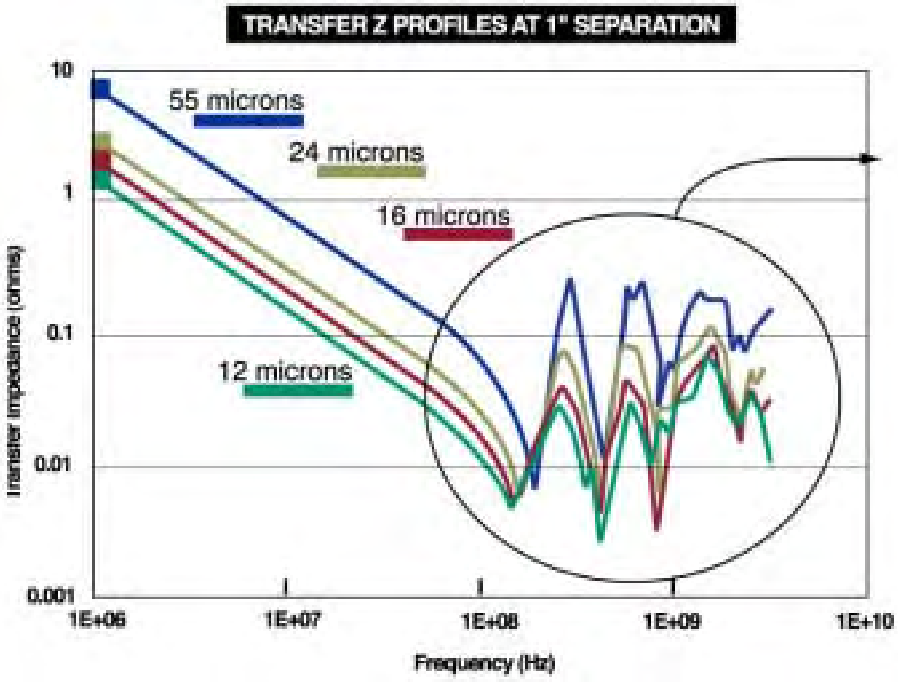
PWB Electrical Performance (Self Z)

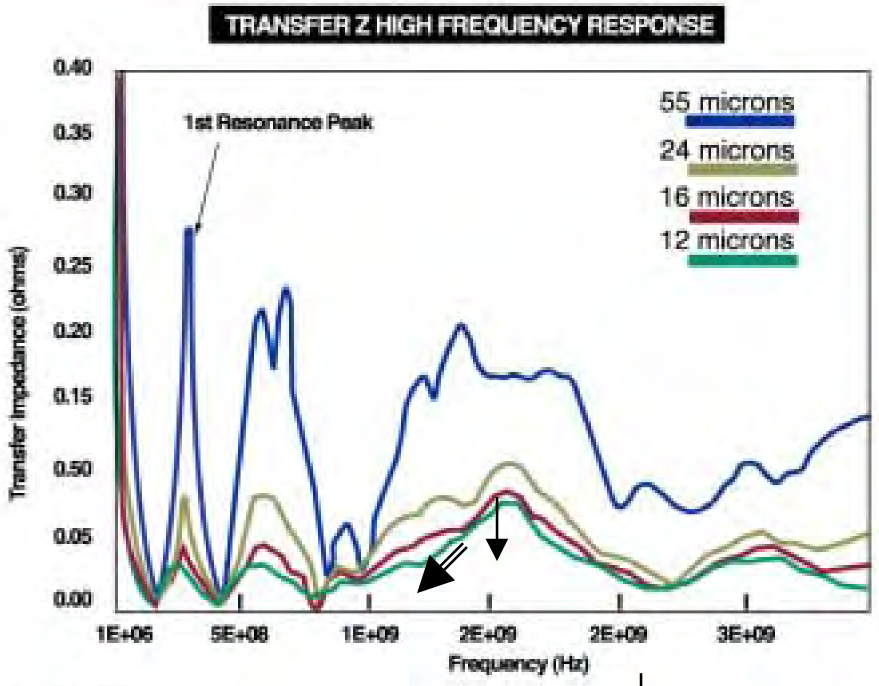
Significant Reduction on Impedance



PWB Electrical Performance (Transfer Z)

Significant Reduction on Impedance


TRANSFER Z PROFILES AT 1" SEPARATION


TRANSFER Z HIGH FREQUENCY RESPONSE

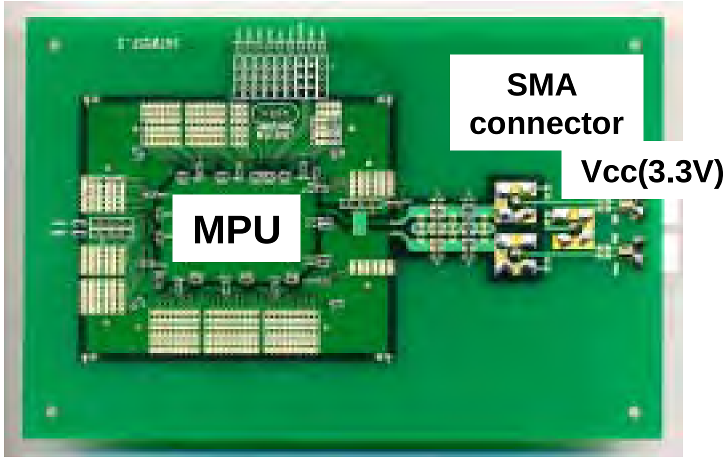
Data Coutesy of Sanmina-SCI Corp.

↓ 8 micron

↙ 16 micron with $BaTiO_3$

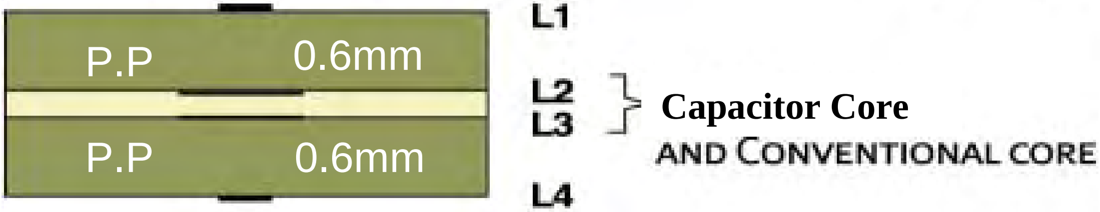
PWB Electrical Performance (Transfer Z)

Significant Reduction of EMI

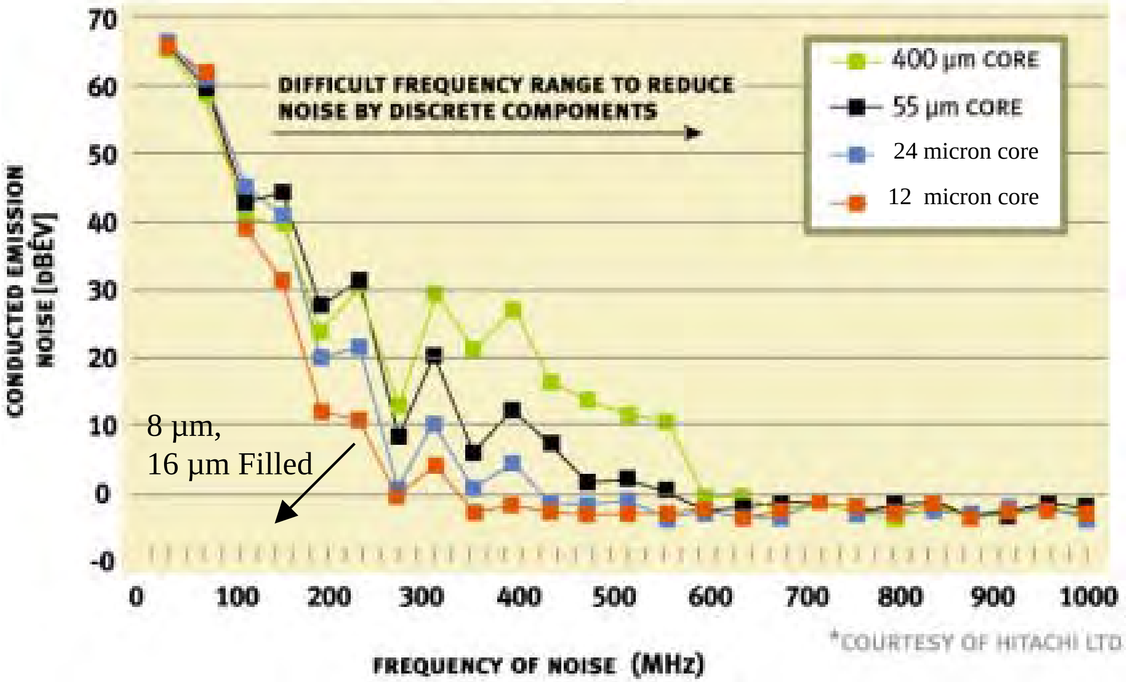


MPU (40MHz) is mounted on the other side of the board.

4 LAYER BOARD



SIGNIFICANT NOISE REDUCTION ON PWBs USING THIN CAPACITOR LAYER



*COURTESY OF HITACHI LTD

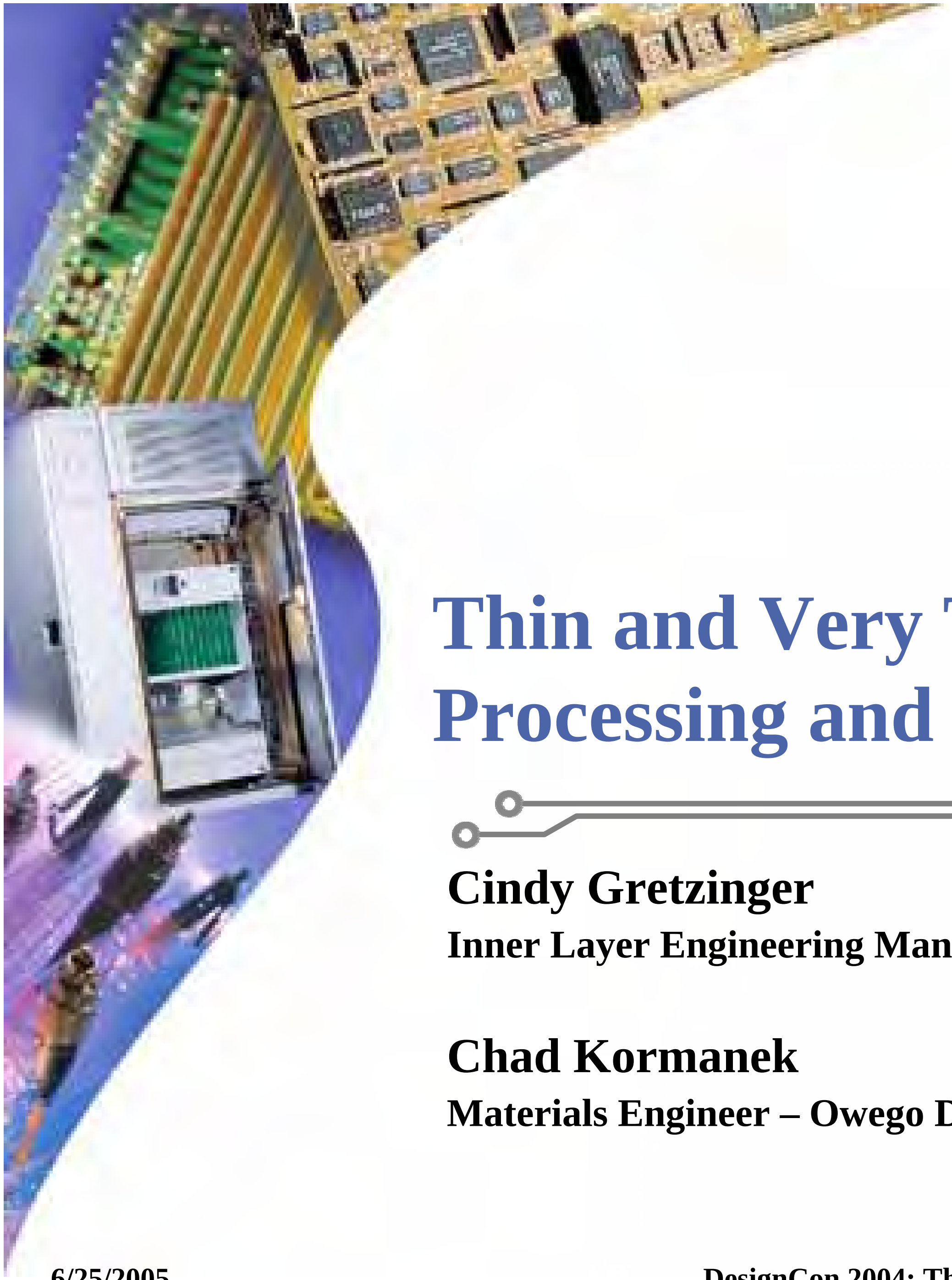
Comparison Summary

Unfilled Substrates Versus Filled Substrates

Property	Unfilled Thin Substrates	Filled Substrates
Impedance Reduction/lower noise		+
Electric Strength/ High Potential Testing	+	
Ease of PCB Processing	+	
Cost of Substrate/Raw Board	+	
Cost of Assembled Board	?	?

Conclusion

- Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency
- New Substrates have demonstrated *excellent* electrical performance and physical properties.
- They are *compatible* with PWB processing; a truly “drop in” material.
- Materials are commercially available from Licensed Fabricators
- The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
- The Technology can Improve System Price/Performance by
  - Reducing Discrete Caps
  - Reducing PWB size
  - Increasing Functionality
- Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PWBs
- Additional work is ongoing to
  - Improve PWB manufacturing process of filled substrates



SANMINA-SCI

Thin and Very Thin Core Laminates: Processing and Reliability

Cindy Gretzinger
Inner Layer Engineering Manager – Owego Division

Chad Kormanek
Materials Engineer – Owego Division

Topics of Discussion

- **Manufacturability**
  - ***Thin Core Material Experience***
  - ***Thin Core Processing Capabilities***
  - ***Material UL Status***
- **Reliability**
  - ***Thermal Analysis –T260***
  - ***Interconnect Stress Testing (IST)***
    - **Test Equipment**
    - **Test Design**
  - ***Assembly Rework Simulation***
    - **Solder Float Testing**
    - **Multiple Pass Through Reflow**

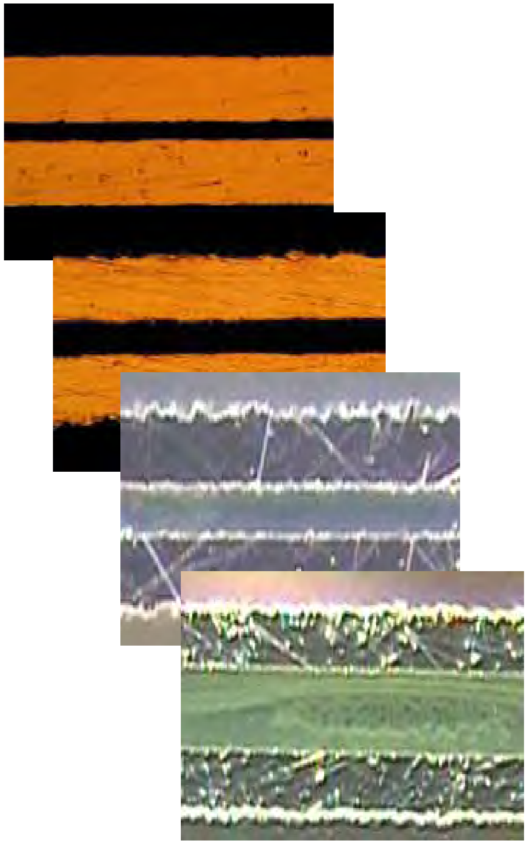
Manufacturability:
Thin Core Material Experience

ZBC-2000®: 2 mil thick material

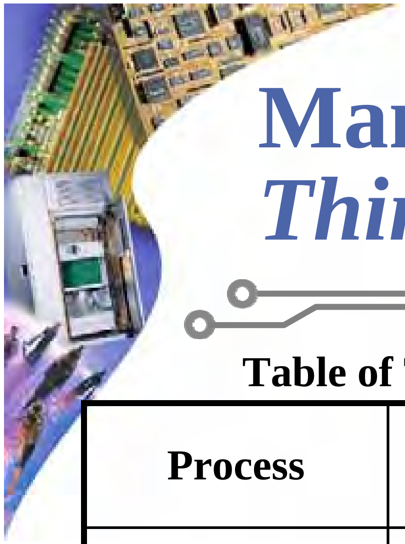
- **Over 10 years experience in processing**
    - >10 million square feet processed
    - Known & established material in the market
- **Versatile:** Worldwide network of licensed laminators and fabricators.
  Full range of material thickness, resin types and copper foils.
  Comprehensive Design Guidelines and Application Support.
- **Quality Controlled:**
  Patented: 9 US Patents, 22 Foreign Patents
  Common standards guarantee quality and consistency of material.
  Material testing and qualification program.
  Web site being established for sharing of BC™ information.
  Fully tested, high frequency electrical performance of BC materials.

Manufacturability:
Thin Core Material Experience

SANMINA-SCI



- **< 0.5 mil Cores – Very Thin - Ultra Thin**
  - Oak Mitsui BC12™ (12 micron core)
  - Oak Mitsui 8 -10 micron cores
  - 3M C-Ply (8 micron core)
- **0.6 mil Core – Very Thin**
  - Oak Mitsui BC16™ (16 micron core)
- **1 mil Core – Thin**
  - ZBC-1000™ (25.4 micron core)
  - Oak Mitsui BC24™ (24 micron core)
  - Dupont HK04 (25 micron core)
- **2 mil Cores – Fine Line**
  - ZBC-2000® (2 mil [50.8 micron] core)



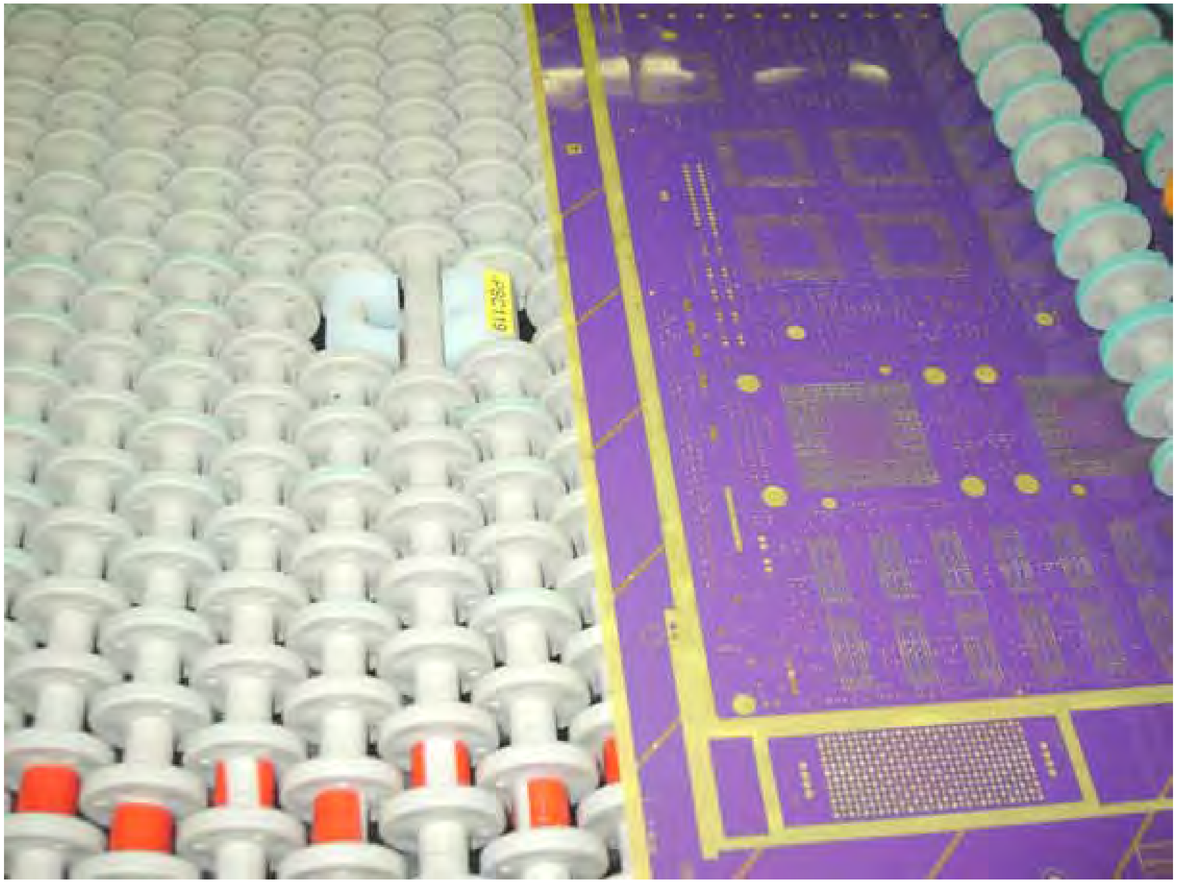
Manufacturability:
Thin Core Processing Capabilities

Table of Thin Core Processing Capabilities as Compared to a ZBC-2000 Baseline

Process	ZBC-1000	24 Micron Non-Reinforced	16 Micron Non-Reinforced	8-12 Micron Non Reinforced
Preclean/ Lamination	Thin core equipment required – no leaders	Thin core equipment required – no leaders	Thin core equipment required – Laminate one side at a time	Thin core equipment required – Laminate one side at a time
Expose	Standard process	Standard process	Standard process	Standard process
Develop, Etch, Strip	Thin core equipment required – no leaders	Thin core equipment required – no leaders	Thin core equipment required – leaders required	Thin core equipment required – leaders required
Post Etch Punch	Front/Manual Unloading Required	Front/Manual Unloading Required	Front/Manual Unloading Required	Front/Manual Unloading Required
AOI	Standard process	Standard process	Standard process	Standard process
Oxide	Horizontal or vertical acceptable	Horizontal or vertical acceptable	Horizontal or vertical acceptable, support needed in baskets	Horizontal or vertical acceptable, support needed in baskets
Lay Up	Standard process	Standard process	Modified Handling	Modified Handling

Manufacturability:
Thin Core Processing Capabilities

Thin Core Conveyor Transport



Manufacturability:
Thin Core Processing Capabilities

SANMINA-SCI

Dimensional Stability

	Repeatability – Width	Repeatability - Length	Movement Deviation – Width (from baseline)	Movement Deviation – Length (from baseline)
ZBC-2000 (Baseline)	**+/- 1.0 mils**	**+/- 0.5 mils**	**N/A**	**N/A**
FaradFlex BC24 µm	**+/- 0.7 mils**	**+/- 0.7 mils**	**- 0.07 mils/in**	**0.02 mils/in**
Faradflex BC16 µm	**+/- 0.8 mils**	**+/- 0.6 mils**	**- 0.06 mils/in**	**- 0.02 mils/in**
Polyimide 25 micron	**+/- 0.9 mils**	**+/- 1.0 mils**	**-0.07 mils/in**	**0.04 mils/in**

** Based on one Commercial Part Number, 24 layer board

Manufacturability:
Thin Core Processing Capabilities

Thin Core Yields

	ZBC 2000 (50 micron)	Interra HK04 (25 micron)	Farad Flex BC24 (25 micron)
Foreign Material	Rework 6.1% Scrap 0.6%	Rework 28% Scrap 2%	Rework 7.7% Scrap 0%
Material Damage	Scrap 2.6%	Scrap 8.0%	Scrap 3.8%
Core Material First Pass Yield	90.7%	62%	88.5%
Core Material Second Pass Yield	96.8%	90%	96.2%

Yields are based on one Commercial part number with 2 Thin cores

Manufacturability:
Thin Core Processing Capabilities

Foreign Inclusion Testing

The higher the inclusion rate, the longer the processing time in AOI & increased chance of scrap at Electrical Test.

Manufacturability:
Material UL Status

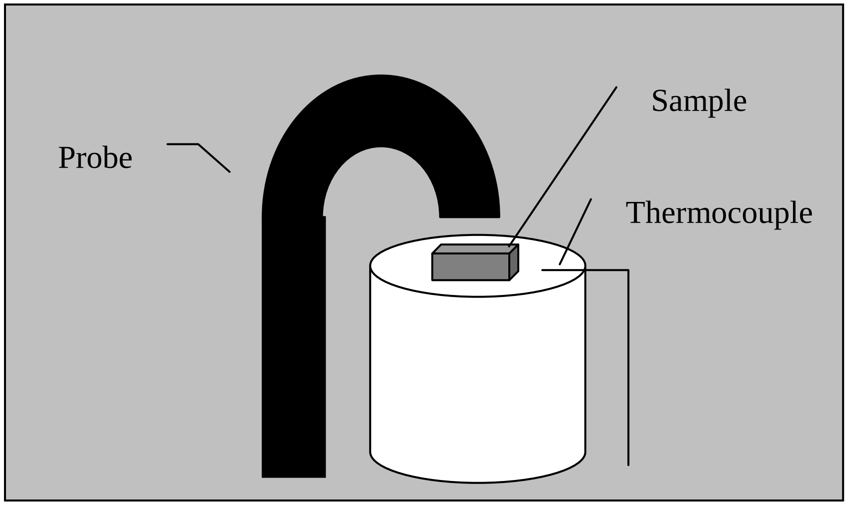
SANMINA-SCI

- ZBC-2000 – *Approved*
- ZBC-1000 – *Approved*
- Oak-Mitsui FaradFlex:
    - BC12 – *Approval March 04*
    - BC16 – *Approval March 04*
    - BC24 – *Approval March 04*
- DuPont Interra HK04 - *Approved*

Reliability:
Thermal Analysis - T260

Thermal Mechanical Analysis TMA

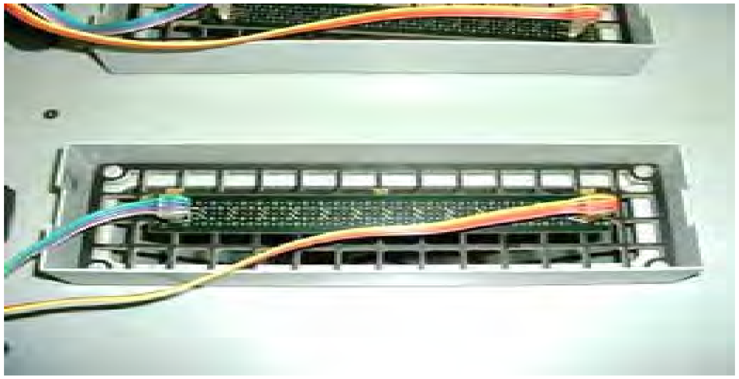
- ➔ **Measure expansion of a sample (X,Y, or Z) as a function of temperature**
- ➔ **Measure % Z-axis Expansion from 50º C to 260º C**
- ➔ **Time to Delamination at 260º C**
- ➔ **No Failures found on any Thin Core Materials to date**
- ➔ **Goal: Further test the thermal reliability of Thin Laminates to induce possible failures on the Thin cores using phenolic materials and TMA up to 288º C**



Reliability:
Interconnect Stress Testing (IST) Test Equipment

SANMINA-SCI

- ➔ Test the reliability of PTH and innerlayer post to barrel connection over a period of thermal cycles
- ➔ Thermal cycles are made using DC current to heat up the coupon and air cooling to reduce the temperature.
- ➔ Resistance changes are checked through the PTH and across the post to barrel connection
- ➔ Testing is coupon design dependant



Reliability:
IST Test Design

SANMINA-SCI

IST Testing

- **IST Test Design : 8 layer Sun Test Vehicle and 26 layer Commercial Part with two Thin Core Layers, 24 layer Commercial Part with four Thin Core Layers.**

- **Results: IST cycles average the same as with standard FR4 layers. No failures found at the Thin core layers.**

- **Further Testing: Test through hole reliability by using Phenolic Materials and new Coupon Designs to induce failures on the Thin Core Layers**
  - **Final board thickness of ~ 0.095” (18 Layers)**
  - **Heater cores positioned at the 4/5 and (n-3)/(n-4) layers**

Reliability:
Assembly Rework Simulation

- Solder Float Testing
  - 6 x Solder Shock Blind Vias
  - 6 x Solder Shock Through Holes
  - No failures on testing done to date

- Further Testing
  - Solder Shock Testing with Phenolic Materials
  - Multiple Pass - 8x Through Reflow
  - Process at a local assembly shop in a 10 zone convection oven

Reliability:
Assembly Rework Simulation

SANMINA-SCI

- **6x Solder Float Testing on Through Holes**

ZBC-1000

Faradflex
24 µm

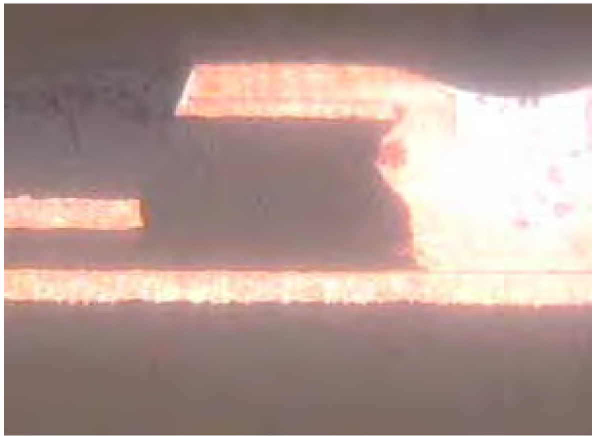
Faradflex
16 µm

Dupont
25 µm

Reliability:
Assembly Rework Simulation

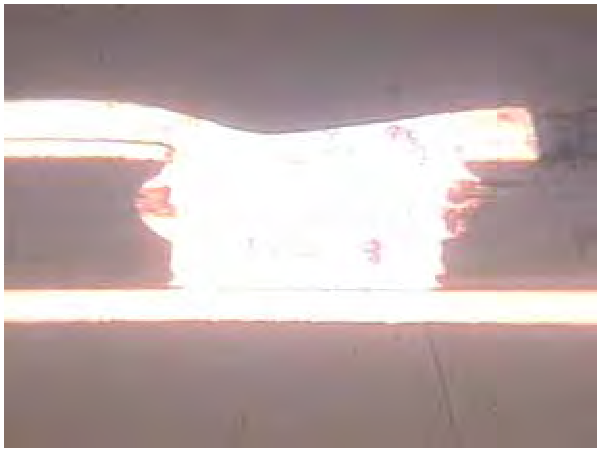
- **6x Solder Float Testing on Blind Vias**

ZBC-1000



Faradflex
24 µm

Faradflex
16 µm

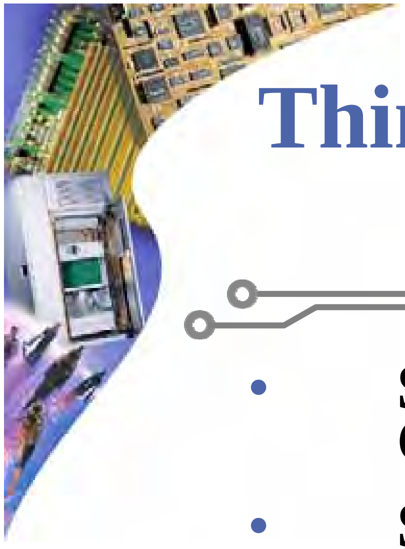


Dupont
25 µm

Reliability:
Test Summary

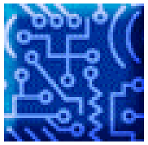
SANMINA-SCI

Test Description	ZBC-2000	ZBC-1000	FaradFlex	Dupont HK04
6x Through Hole Solder Shock IPC 6012 Cross section review	Pass	Pass	Pass	Pass
6x Blind Via Solder Shock IPC 6012 Cross section review	Pass	Pass	Pass	Pass
Dielectric Thickness per Cross Section within +/-10%	Pass	Pass	Pass	Pass
T-260 (>4 min)	Pass	Pass	Pass	Pass
IST Testing	Pass	Pass	Pass	Pass
Core Level Hi-pot Testing 100 Cores (100V/sec ramp; 500 V max)	Pass	Pass	Pass	Pass
Finished Circuit Level Hi-pot 50 circuits (100V/sec ramp; 500 V max)	Pass	Pass	Pass	Pass



Thin Core Processing Summary

- Sanmina-SCI is capable of manufacturing Thin Cores down to 8 µm.
- Sanmina-SCI has extensive experience with ZBC-2000 (>10,000,000 core square feet produced)
- Reliability testing indicates that Thin Cores packages are as thermally reliable as the dicy cured FR4 material
- Initial yield data suggests a difference in foreign material inclusion rates between the suppliers
- Initial yield data suggests a higher rate of material damage on the 24 µm material
- Sanmina-SCI is continuing comparison testing of the materials for reliability and material yield improvements



Processing Thin and Very Thin Laminates:
What Is New in 2004?

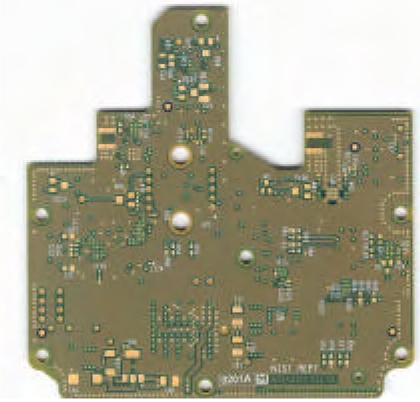
This work was performed under support of the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025

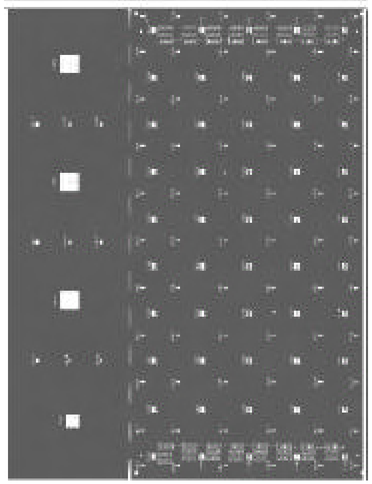
Introduction

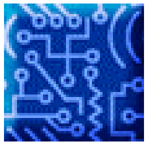
- At DesignCon 2002 reported on:
  - 3M C-Ply: 8 μm $BaTiO_3$ filled epoxy
  - DuPont: thin $BaTiO_3$ filled polyimides
- Since then, have gained experience with:
  - Oak-Mitsui FaradFlex: 12 μm epoxy/polymer
  - 16 μm version of 3M's C-Ply
  - DuPont HK-4: 25 μm polyimide
  - DuPont HK-10: 25 μm $BaTiO_3$ filled polyimide
  - DuPont HK-11: 12 μm $BaTiO_3$ filled polyimide
- Future work planned with:
  - Oak-Mitsui BC16T: $BaTiO_3$ filled epoxy/polymer

Thin Laminate Board Builds

- NIST AEPT test vehicles (TV1-C and TV2-C)
- Two emulators with the C-Ply material:
  - Nortel high-speed emulator
  - Hewlett-Packard iPaq emulator boards
- Impedance test boards for Sun with C-Ply and DuPont HK materials.

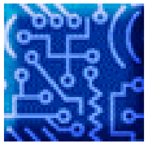






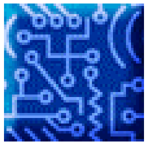
Thin Laminate Board Builds

- As interest has grown, we have built prototypes and production boards with both filled and non-filled materials for customers
- Materials used in combination with Isola, MEM, and Nelco materials, some with embedded resistors
- These thin laminates stretch the capability of our equipment but also improve our ability to process standard materials



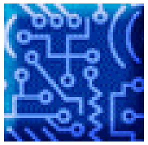
Processing Challenges

- Differences between filled and non-filled materials:
  - Filled laminates require subpart processing
  - Non-filled materials generally able to withstand etcher spray pressure, so both sides can be etched simultaneously.
  - Thin, filled dielectric materials have a lower breakdown voltage, and so must be HiPot tested at a lower voltage.



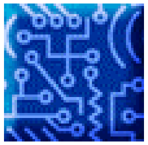
Processing Challenges

- Non-filled laminates may be *more* difficult to convey through an etcher than filled laminates
  - With filled laminates, the copper is completely left on one side of the panel, which provides extra support
  - With non-filled laminates, depending on the panel layout, there may be “fold” lines in the etched panel
  - May be necessary to use leader boards when processing very thin unfilled materials



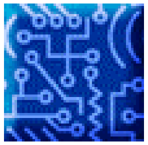
Processing Challenges

- Conveyor systems must be well-maintained
  - Misplaced rollers or guide fingers can be disastrous
  - Can use thin “dummy” panels to check conveyors
  - Rolled-annealed copper has more surface tension than reverse treat copper foil, so may adhere more as it goes through pinch rollers
- Autolaminator maintenance is critical
  - Balance tension of the top and bottom rolls
  - Once the equipment is set up correctly for thin materials, standard product will also run trouble-free



Processing Challenges

- For post-etch punch and AOI optical systems may need to adjust contrast between the copper and the dielectric. Handling also key.
- Scaling may vary for different stackups
  - No fiberglass reinforcement to constrain movement
  - Ultra-thin materials tend to move with adjacent materials
  - Once determined, scaling is generally stable



Processing Challenges

- Train technicians to handle thin materials as they would film
- At electrical test, may need to make adjustments for extra capacitance and reduced dielectric withstanding voltage of loaded materials

UL Qualification and IPC Standards

- UL qualification:
  - 3M C-Ply (complete)
  - DuPont HK4 (complete)
  - Oak-Mitsui FaradFlex (in process)
- IPC board performance standard for embedded passives virtually complete
  - We hope to incorporate it into IPC 6012

Summary

- OEMs are showing greater interest in thin and very thin laminates for performance, size EMI improvements
- Process challenges can be met with:
  - Good equipment that is well maintained
  - Technicians that are well trained
  - Minor process adjustments
- The capability to process very thin materials makes standard thickness material processing easier and more robust

Unicircuit Thin Laminate Experience

2/8/2004

Materials Utilized:

- 3M C-Ply
- Gould Upilex
- Nelco N4000-6
- Polyclad 371

Manufacturing Issues & Lessons Learned:

- Artwork modifications
- Material stabilization
- Transportation approach for .001 & .002 cores
- .002 cores with 2oz Cu
- Hipot testing
- Lamination
- Thermal stress testing
- IST testing

OEM Product Deployment:

- Raytheon
- Lucent
- Agilent
- MIT
- Motorola SPS
- Rockwell Collins

Summary:

- End item performance data is very closely held by OEM's and is considered to be confidential and proprietary.
- Products are being deployed in a number of different market sectors.
- Robust manufacturing guidelines have been established.
- In process and final yield data supports that the product is mature, and is production worthy.

CM Challenges Related to Thin and Ultra Thin Core Laminates =< 1 Mil

February 2nd , 2004

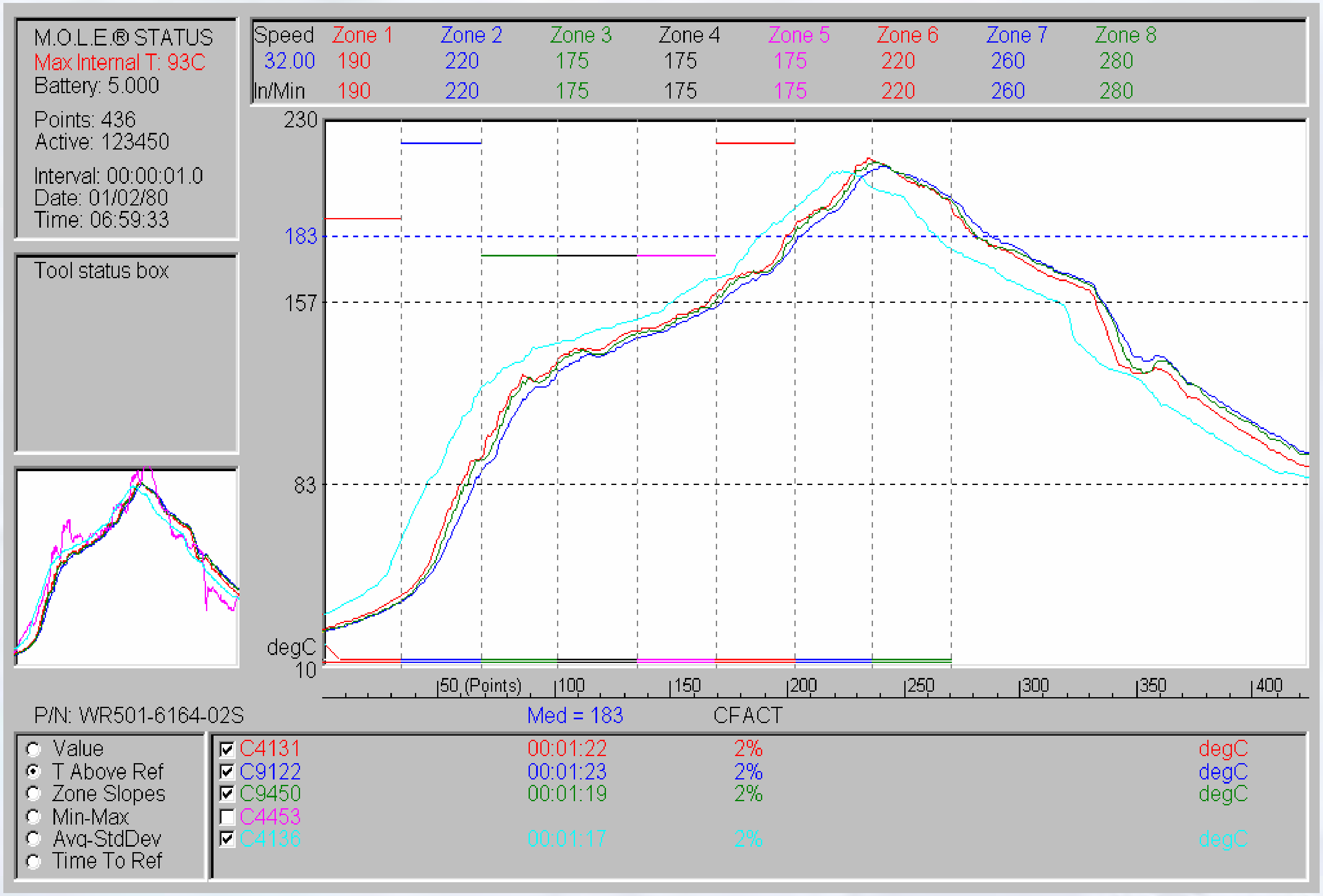
Benchmark
Electronics

Considerations for Processing 1 Mil Boards

- Incoming Inspection
- Cross-sectional Analysis
- Handling
- Storage
- Fixturing
- Thermal Profiling
- Testing
- Final Packaging
- Integration

Benchmark
Electronics

Typical Profile for Processing this Size/ Type Assembly



M.O.L.E.® STATUS
Max Internal T: 93C
Battery: 5.000

Points: 436
Active: 123450

Interval: 00:00:01.0
Date: 01/02/80
Time: 06:59:33

Tool status box

Speed	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7	Zone 8
32.00	190	220	175	175	175	220	260	280
In/Min	190	220	175	175	175	220	260	280

P/N: WR501-6164-02S

Med = 183

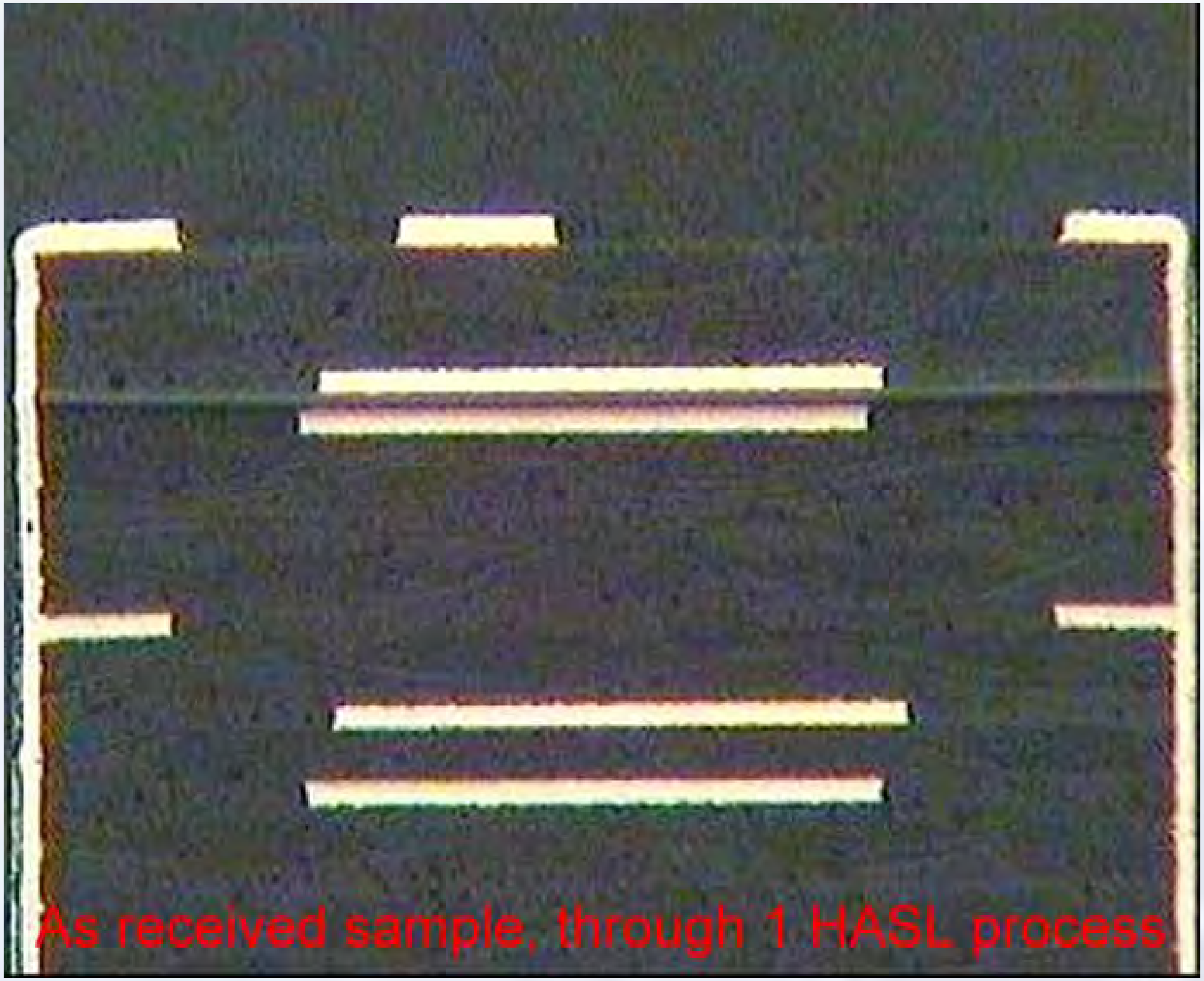
CFACT

○ Value
● T Above Ref
○ Zone Slopes
○ Min-Max
○ Avg-StdDev
○ Time To Ref

☑ C4131	00:01:22	2%	degC
☑ C9122	00:01:23	2%	degC
☑ C9450	00:01:19	2%	degC
☐ C4453			
☑ C4136	00:01:17	2%	degC

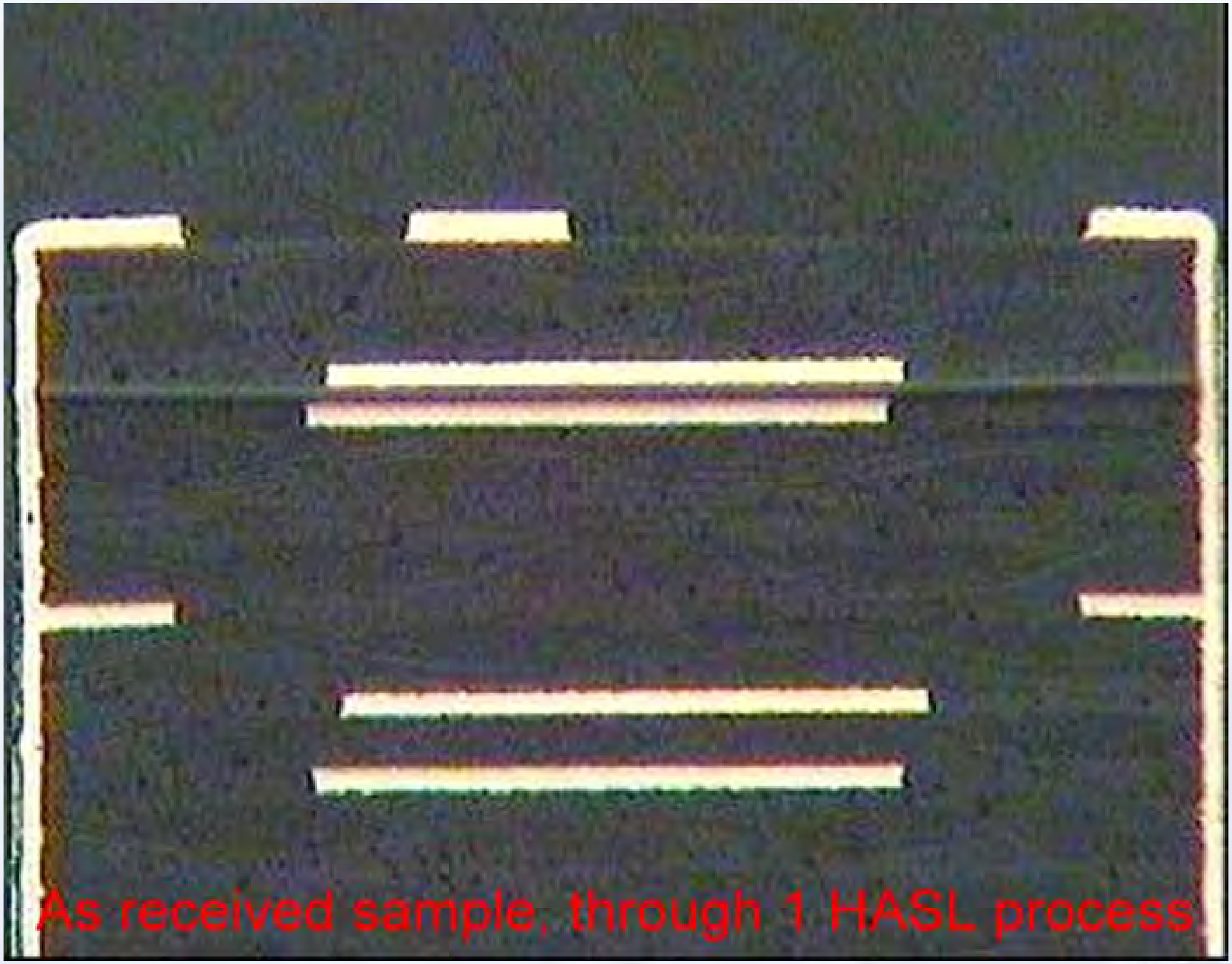
Benchmark
Electronics

As received Sample, note condition of 1 mil Core



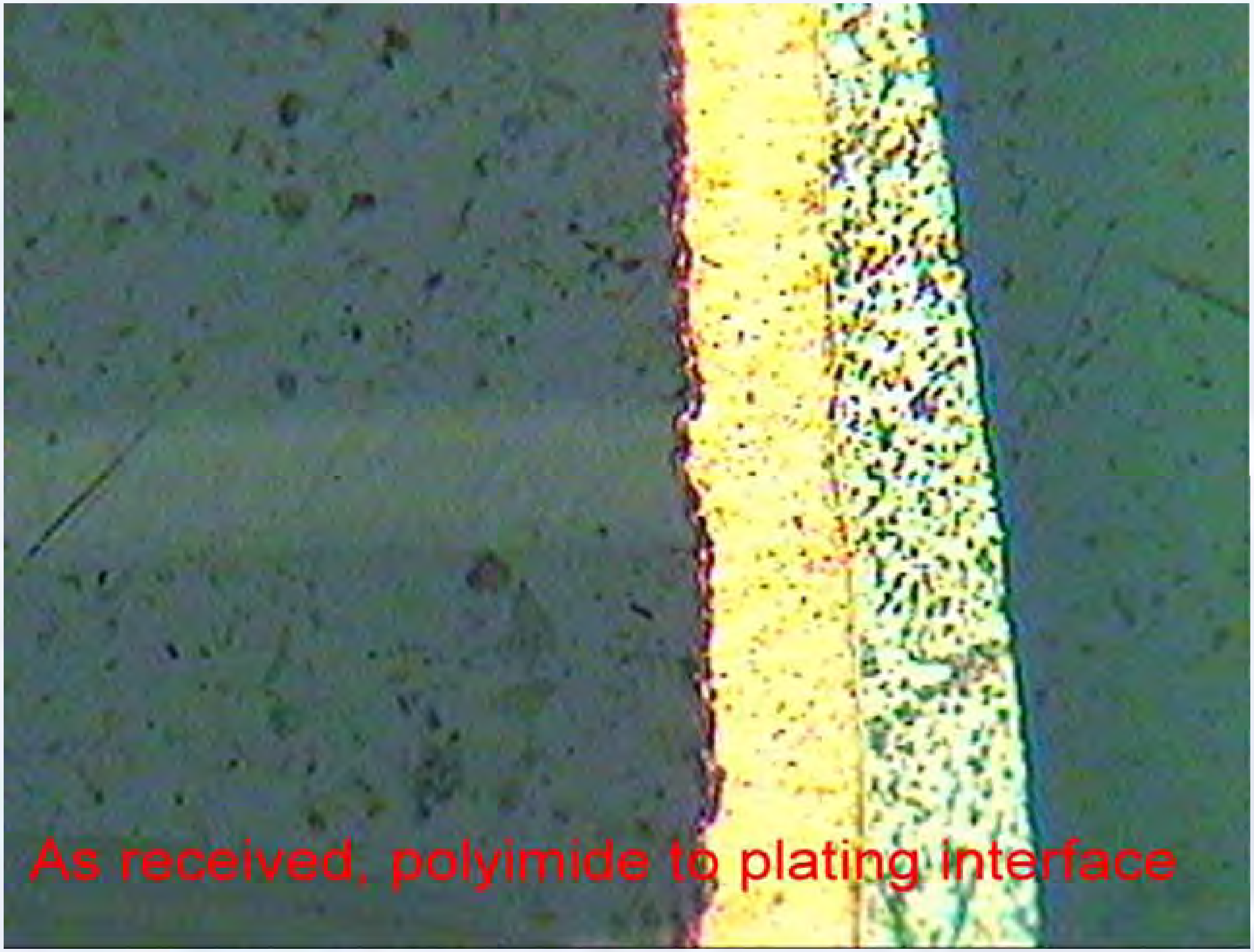
Benchmark Electronics

As received sample through 1 HASL process



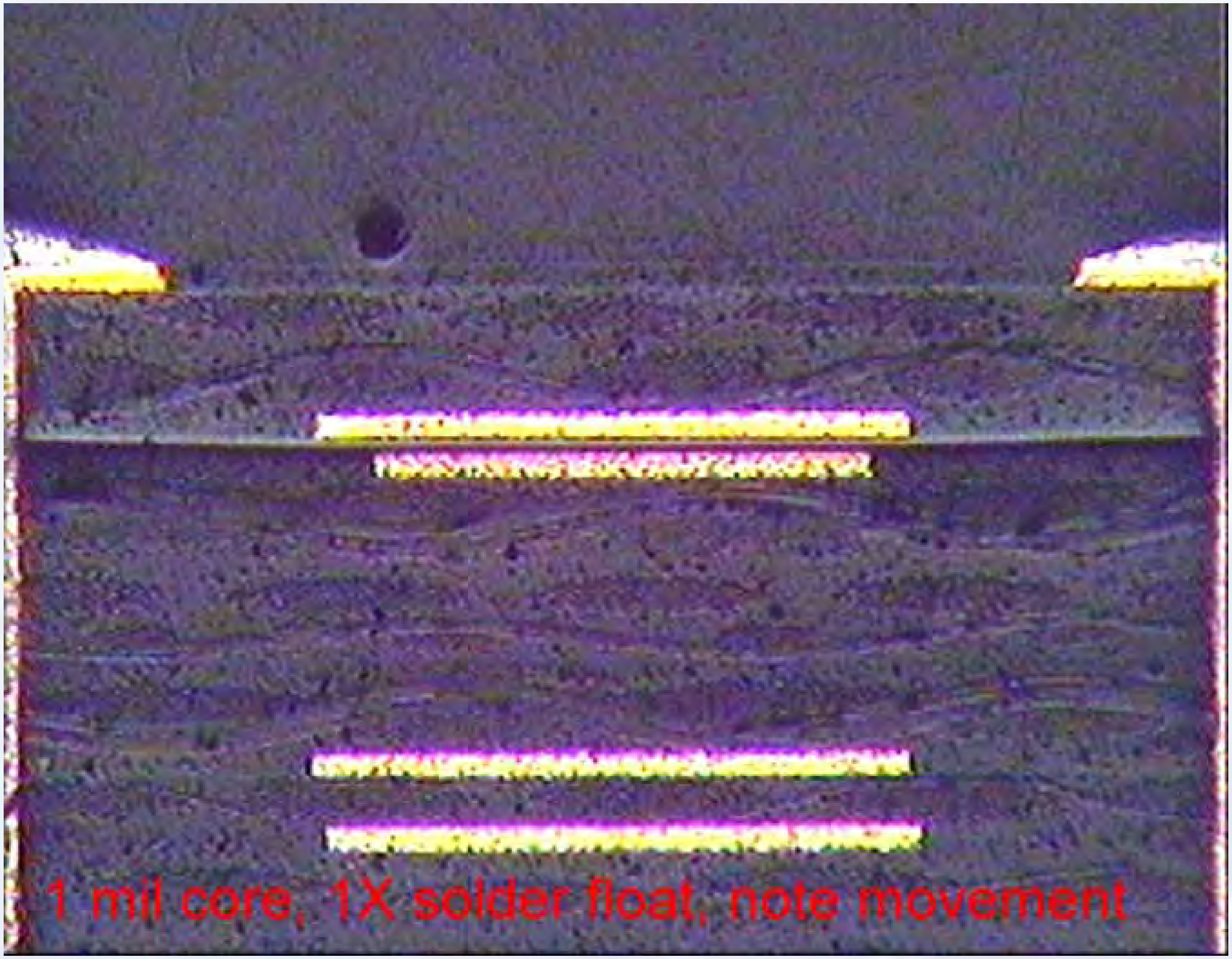
Benchmark Electronics

As received sample, polyimide to copper interface



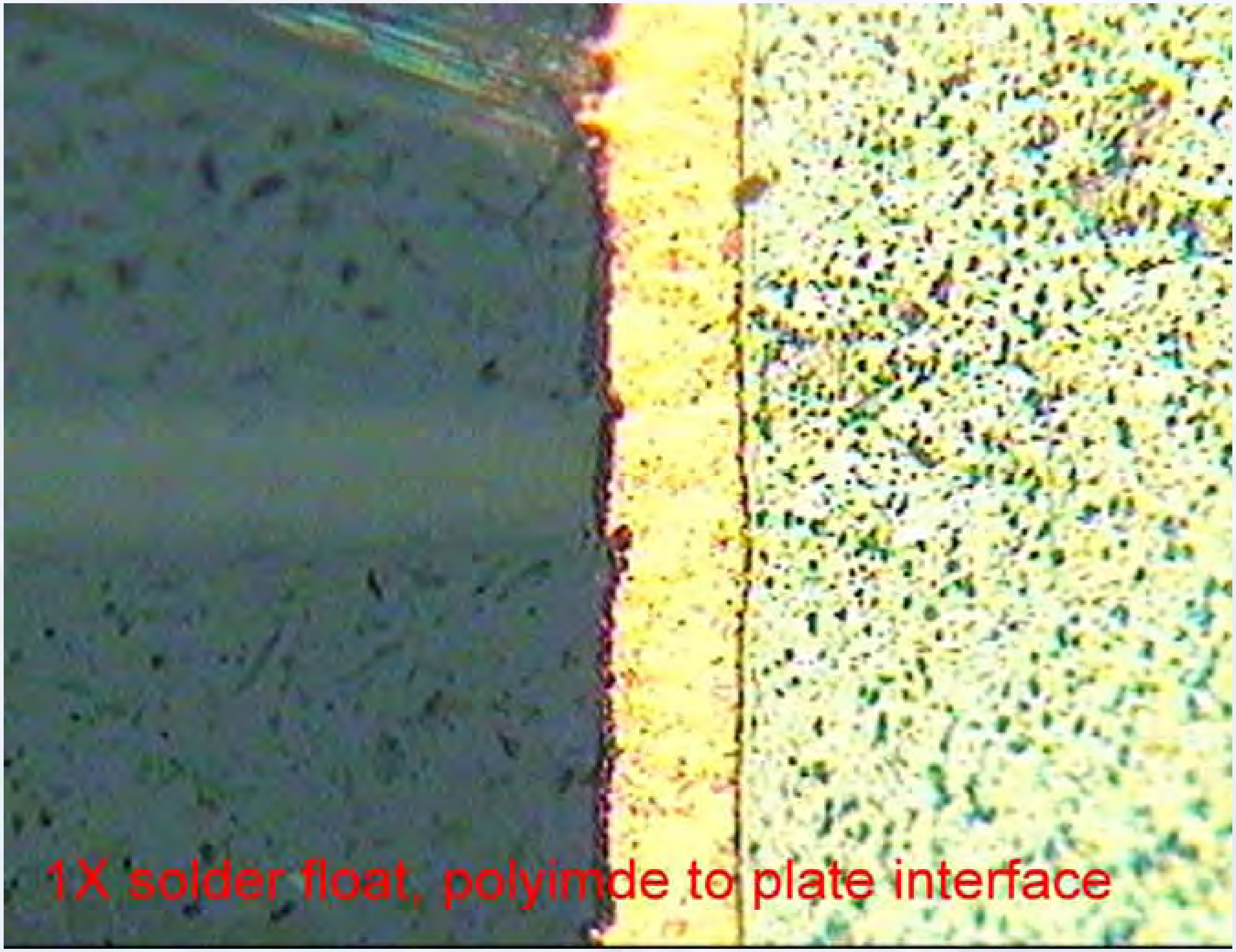
Benchmark
Electronics

1 X solder float sample, note 1 core movement

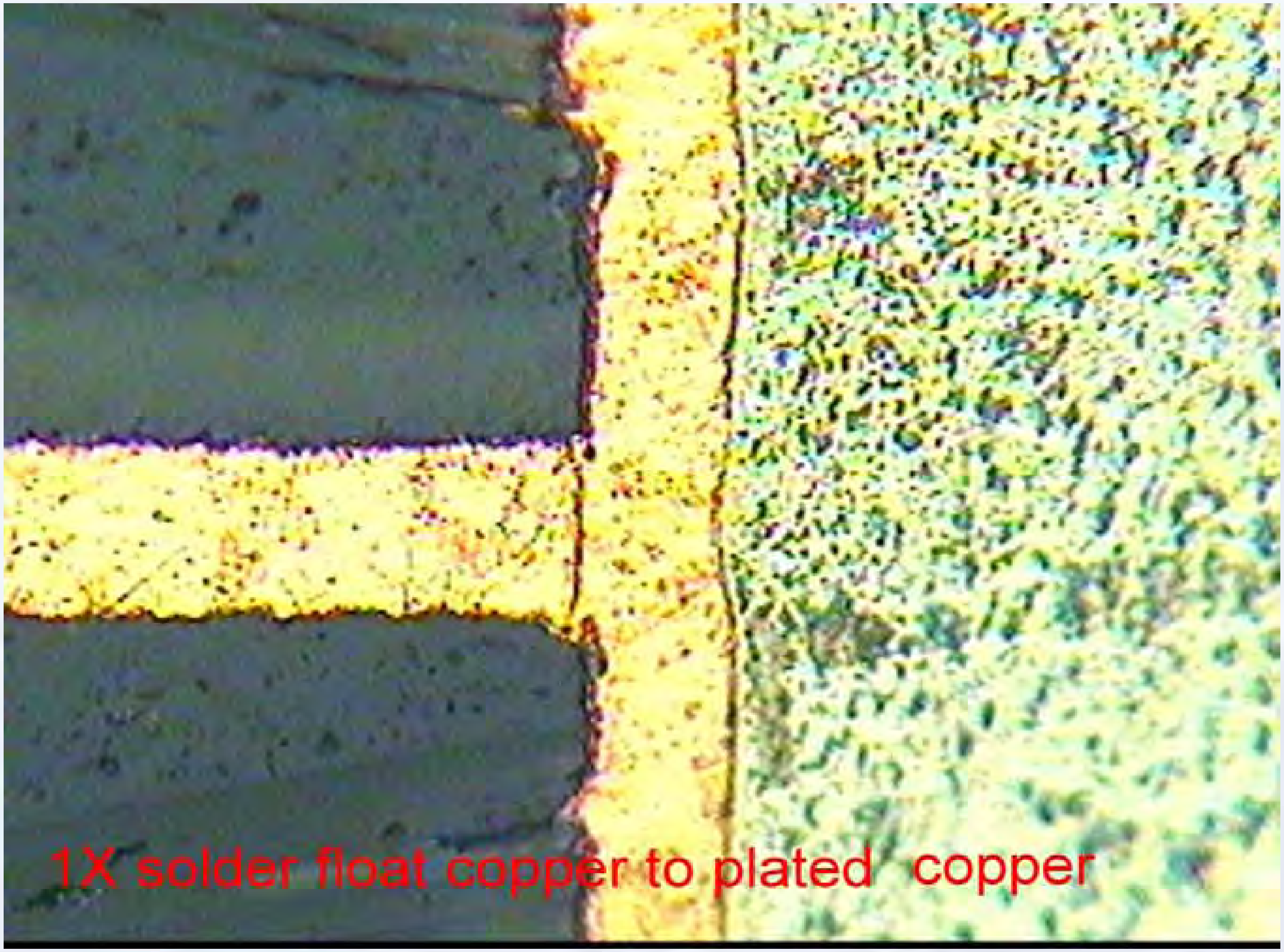


Benchmark
Electronics

1X solder float, polyimide to copper plate

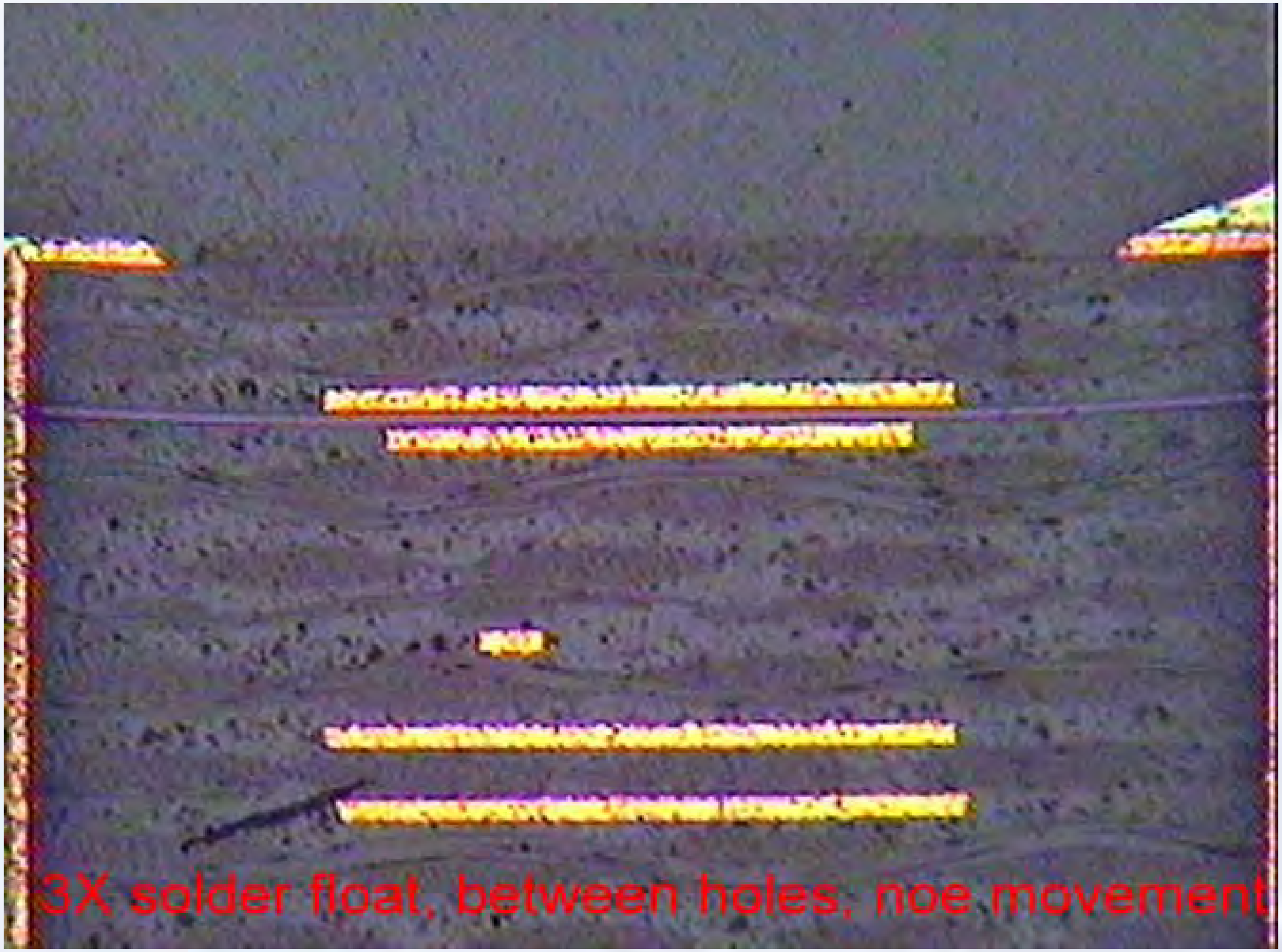


1X solder float, copper to copper interface

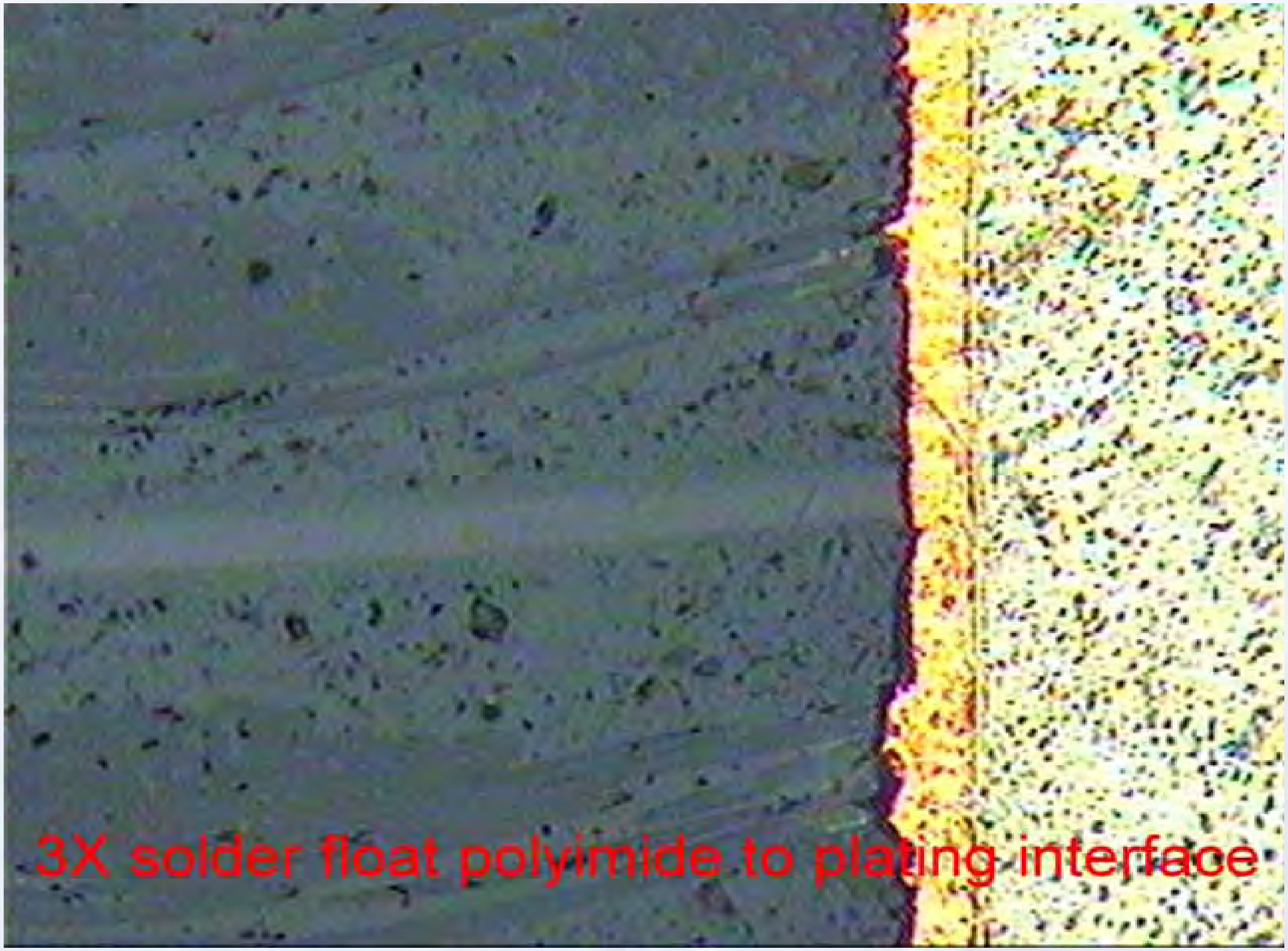


Benchmark Electronics

3 X solder float, note the position of polyimide

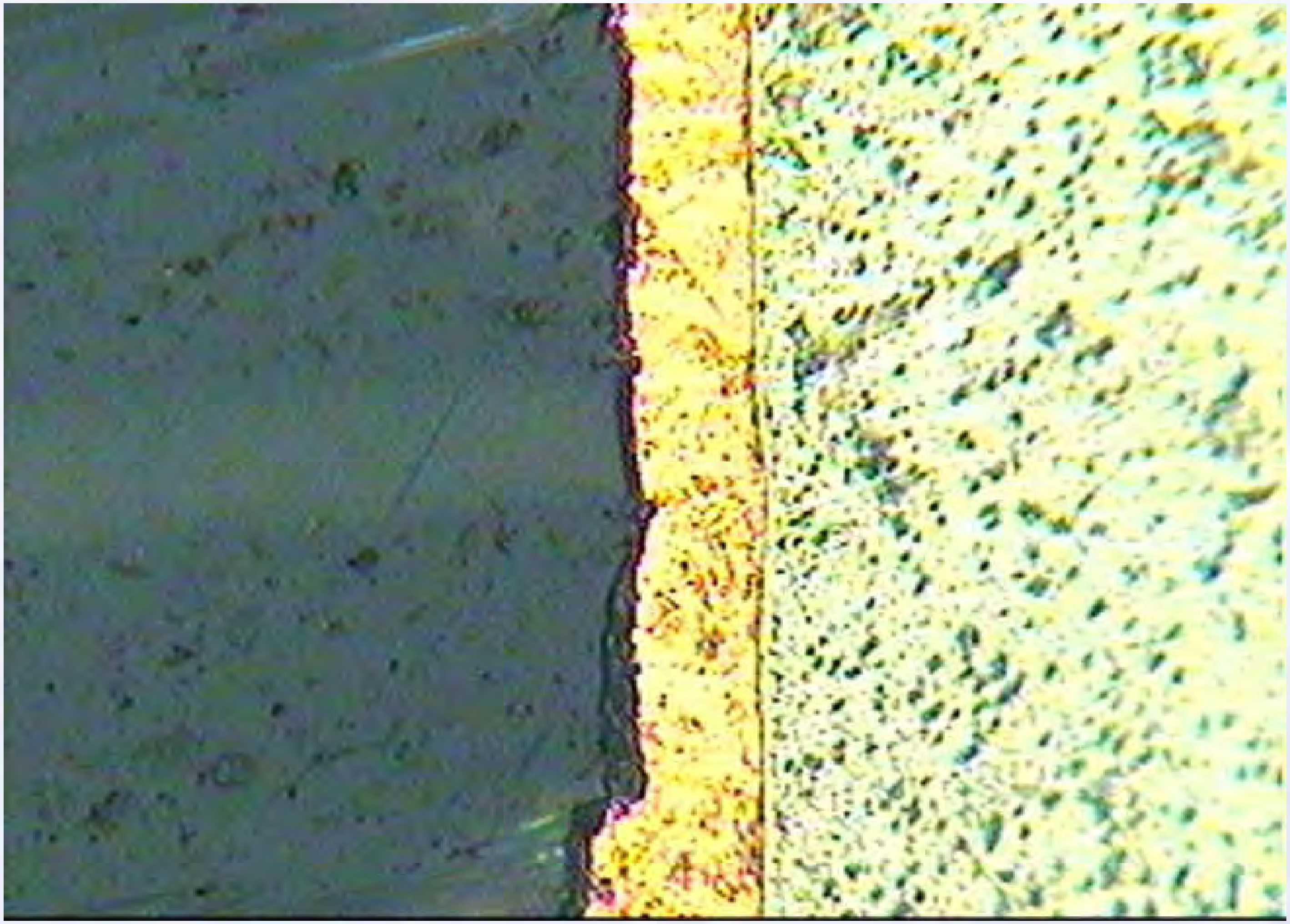


3 X solder float polyimide to plating interface



Benchmark
Electronics

Closer view of Polyimide to copper interface

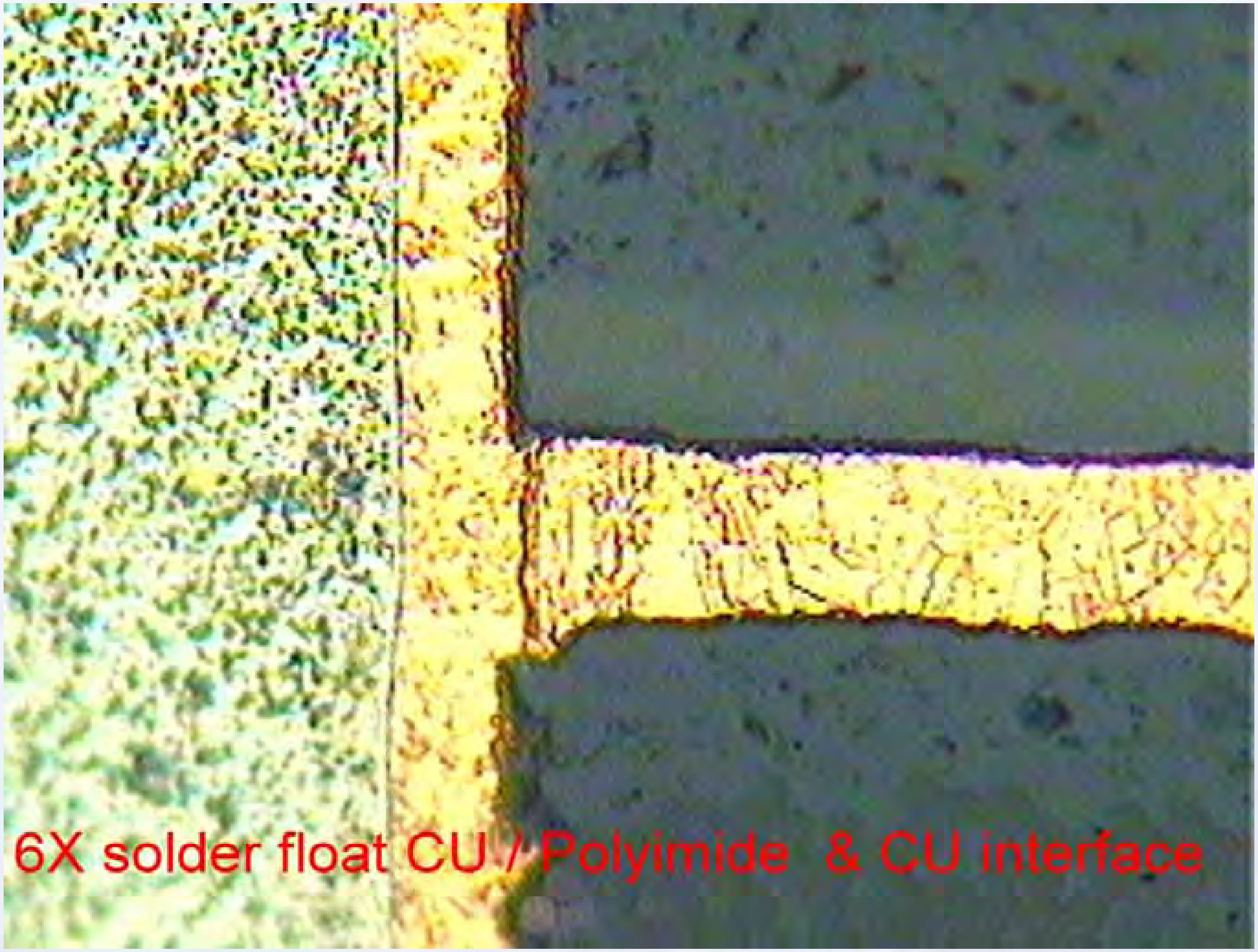


Benchmark Electronics

6 X Solder Float, Polyimide To Plated Copper

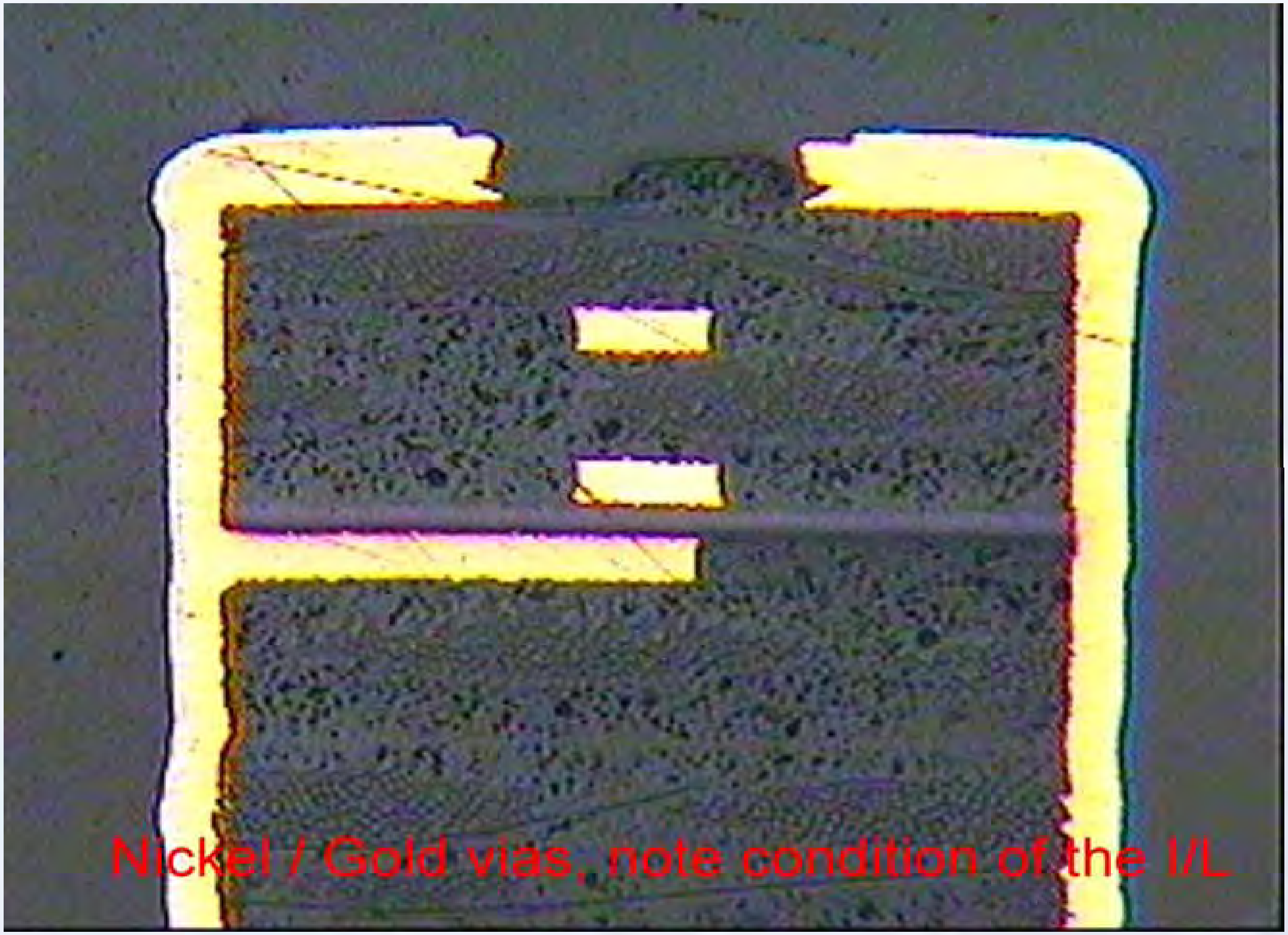
Benchmark Electronics

6 X Solder Float, note 1 mil Core interface region



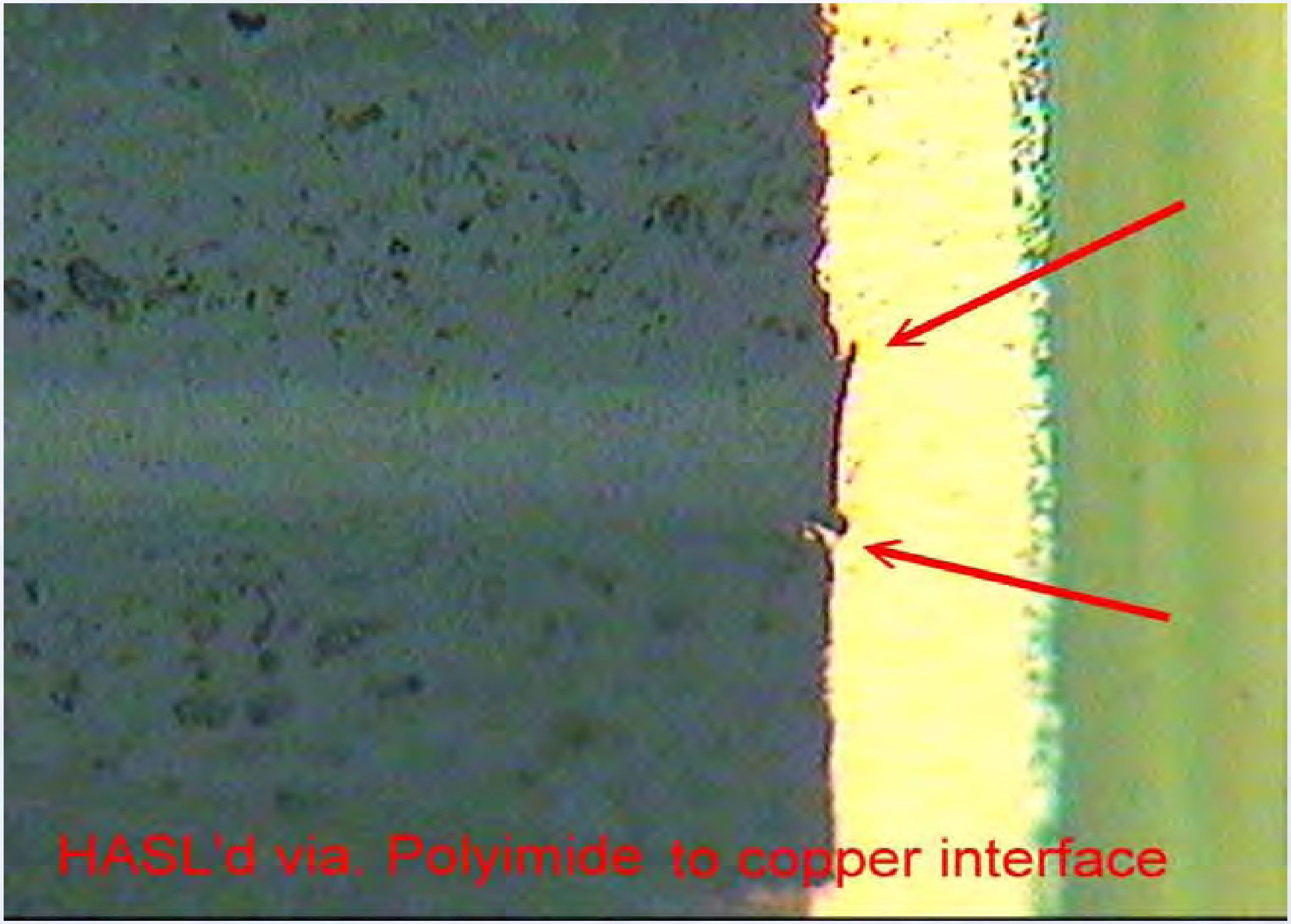
Benchmark Electronics

Nickel / Gold Via


Nickel / Gold vias, note condition of the I/L

Benchmark
Electronics

Polyimide to copper plating



Benchmark
Electronics

What do we know and where do we go?

- 1 mil Material has been in use for many years
- Application to PCBs recent event
- 250 plus units processed at BEI without failure related to 1 mil
- IST testing from Multiple suppliers indicate acceptable reliability
- Long term reliability studies for assembled product not complete
- HALT / HASS type testing recommended for assembled units

Thin Laminates and Power Plane Noise

John Grebenkemper, Ph.D.
Hewlett-Packard Company
February 2, 2004

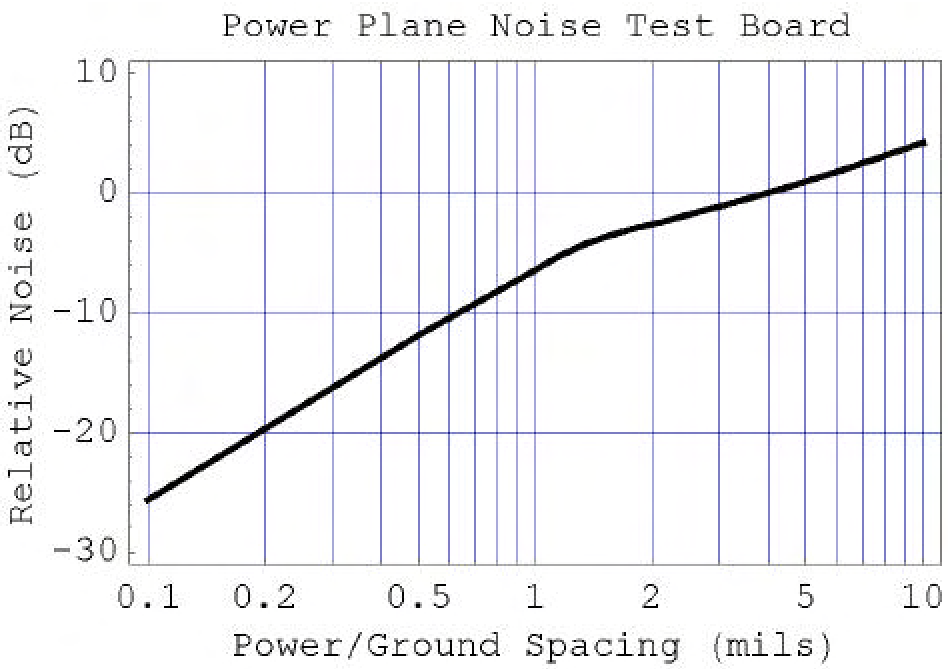
Laminate Thickness & Noise

- Reduced Laminate Thickness Decreases Noise
  - Increased capacitance between planes
  - Decreased distribution inductance
  - Reduced distribution impedance
- Reduced Laminate Thickness Increases High Frequency Loss
  - Increases electric field between power and ground planes
  - Increases high-frequency current in conductors
  - High-frequency loss increases due to I^2R
  - Increased loss damps noise faster

Calculation of Power Plane Noise

- Simulated board physical design parameters
  - Board size : 3 by 6 inches
  - Separation between power and ground planes: 4 mils
  - Assumed dielectric loss tangent: 0.01
  - Assumed relative permittivity of dielectric: 4
  - Copper power and ground planes
    - Conductivity of copper: 58×10^6 Siemens/meter
  - Noise source is 2 ns pulse with a 200 ps risetime
  - RMS Noise averaged across entire board

Spacing Between Power And Ground Planes



- Decreasing the spacing between the power and ground planes can substantially reduce the noise
- Slope ~10 dB/decade above 1.5 mil spacing
- Slope ~20 dB/decade below 1.5 mil spacing
- A 0.3 mil spacing has 16 dB less noise than a 4 mil spacing

Laminate Thickness Test Board

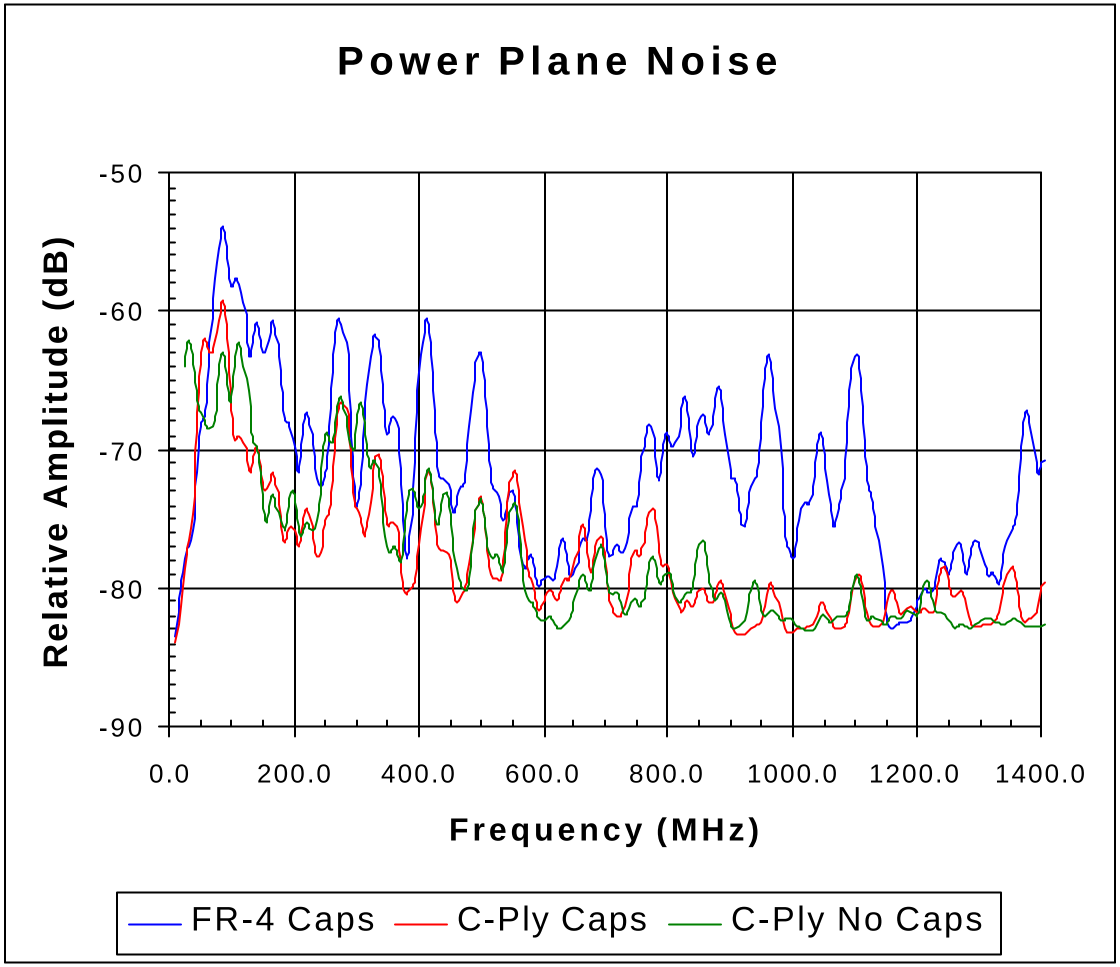
- Processor daughtercard
  - MIPS R14K processor @ 550 MHz
  - 9 Secondary cache SRAM's @ 275 MHz
- Laminate thickness between power & ground modified
  - Standard FR-4 type material, 3 mil thickness
  - 3M C-Ply material, 0.3 mil thickness, $\varepsilon_r=16$
- Measurements made on 1.5 volt I/O power distribution

High-Frequency Bypass Capacitors

- Bypass capacitors used in test vehicle
- Capacitors distributed around the board
- Mounting sites for 0603 capacitors designed to minimize ESL

Quantity	Value	Package
9	2.2 μF	8-pin IDC
15	0.1 μF	0603
15	1000 pF	0603
15	100 pF	0603

Noise Reduction Using C-Ply 8µm Dielectric



- Blue: 3 mil FR-4
- Red: 0.3 mil C-Ply
- Green: 0.3 mil C-Ply with no HF bypass capacitors
- High frequency noise is substantially reduced
  - Insufficient low frequency capacitance when no HF bypass capacitors used

Total Noise Power

- Integrate noise power over frequency
- Compute the relative change in noise power
- Bypass capacitors do not provide much benefit with C-Ply material
- 13 dB reduction in noise with no HF bypass capacitors between FR-4 and C-Ply Laminates

FR-4 With No HF Bypass Capacitors	+6.8 dB
FR-4 With HF Bypass Capacitors	0.0 dB
C-Ply With No HF Bypass Capacitors	-6.5 dB
C-Ply With HF Bypass Capacitors	-7.1 dB

Conclusions

- Decrease the laminate thickness to reduce the noise on printed circuit board power planes
- May be able to eliminate some of the HF bypass capacitors

hp®

invent

Frequency Dependent Capacitance and Inductance of Thin and Very Thin Laminates

Istvan Novak

Signal Integrity Senior Staff Engineer

Volume Server Products

Sun microsystems

Outline

Laminates measured

Test board construction

Extracted absolute capacitance:

Extracted relative capacitance

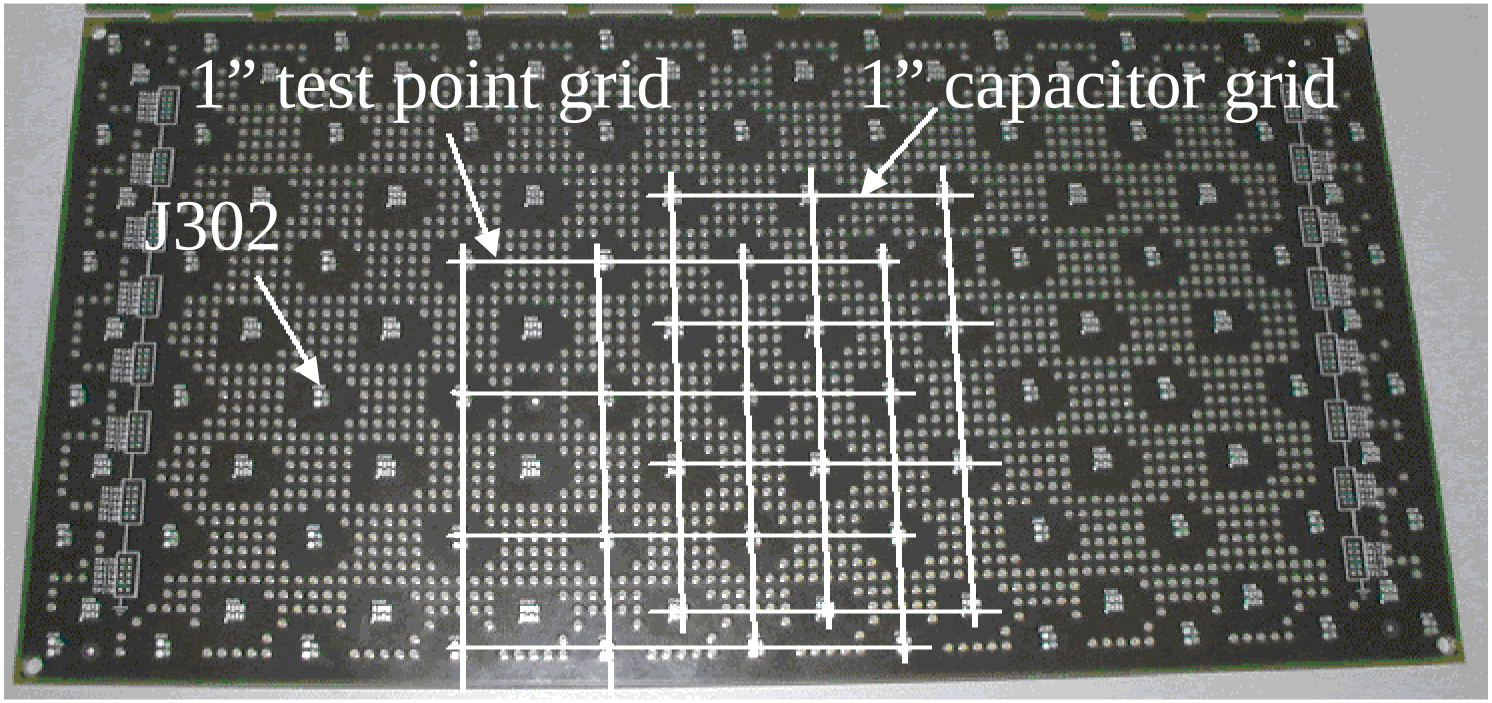
Extracted inductance

Conclusions

Thin Laminates in Test Boards

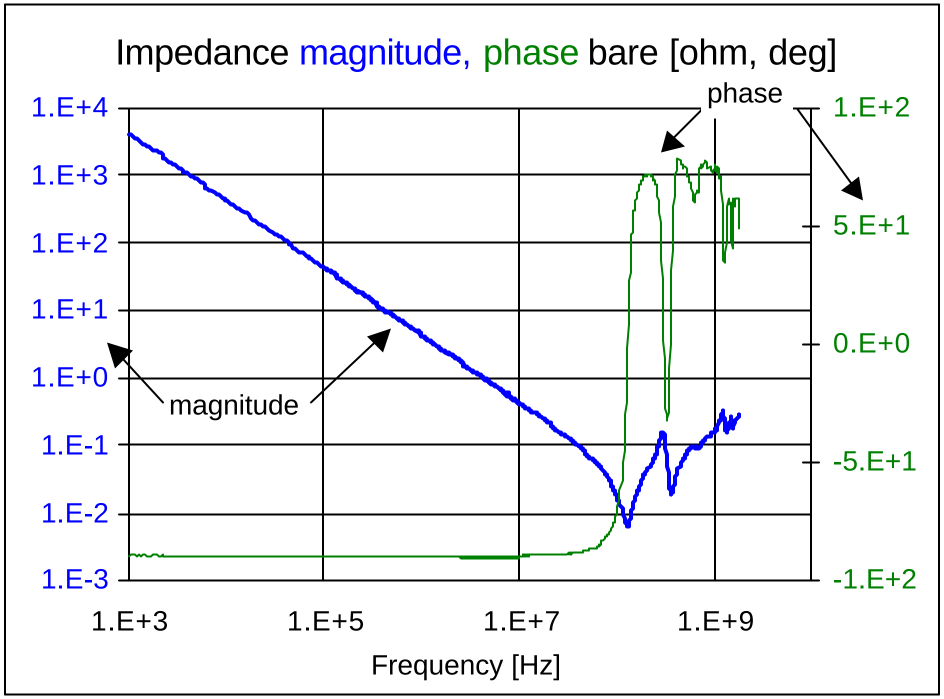
- DuPont's Interra^{TM} HK04: three 25um laminates with one and two-ounce RA and ED Cu; two 50um laminates with one and two-ounce RA Cu, one HKXX14 laminate with one-ounce Cu
- Oak-Mitsui FaradFlex^{TM} unreinforced epoxi: 24um, 16um and 12um laminates with one-ounce RA Cu
- Matsushita glass-reinforced epoxi laminates: ZBC2000^{TM} and ZBC1000^{TM} with one-ounce Cu
- 3M C-Ply^{TM} 24um, 12um, 8um unreinforced filled epoxi, one-ounce Cu

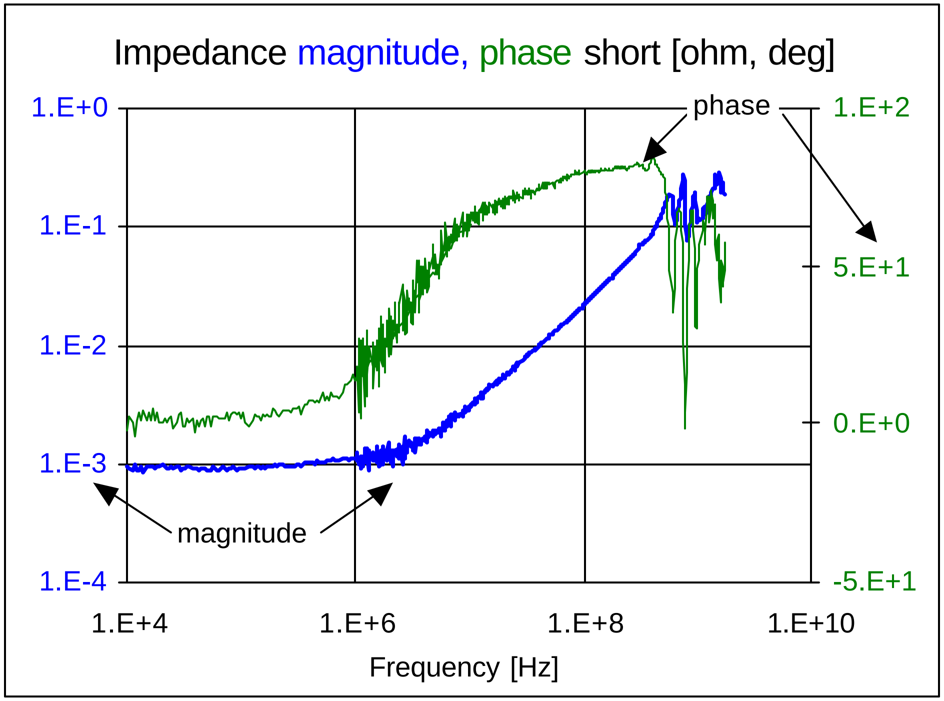
Test Board Top View



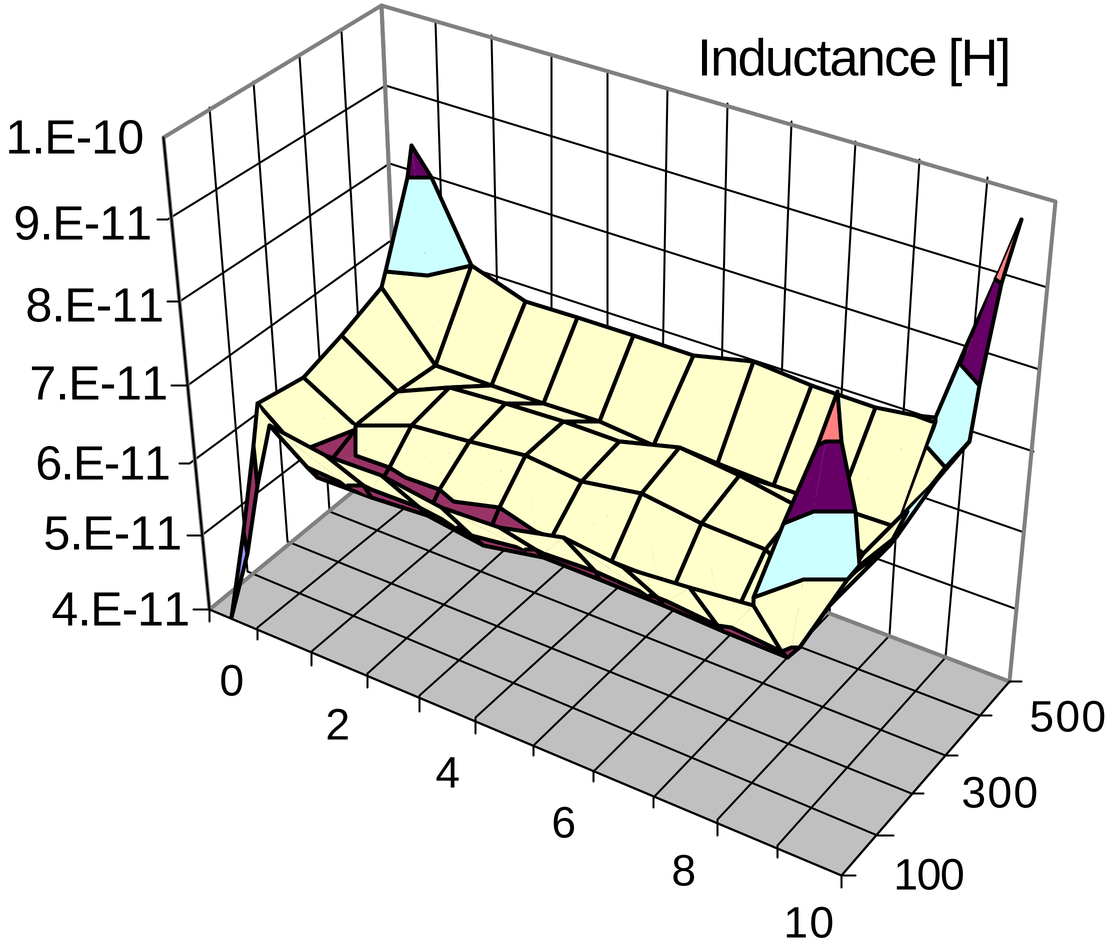
Open/Shorted Board Impedance

HK042536R

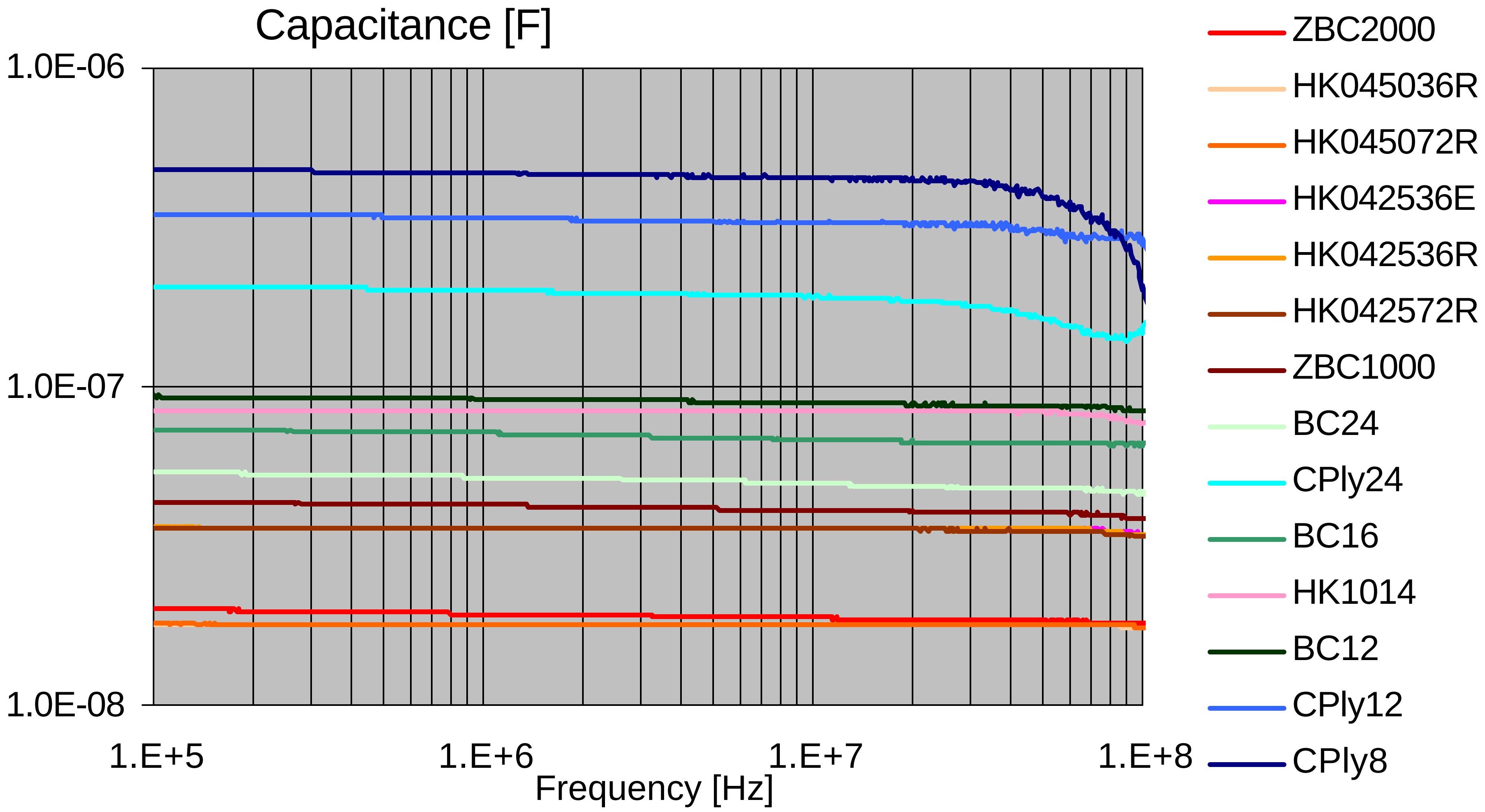




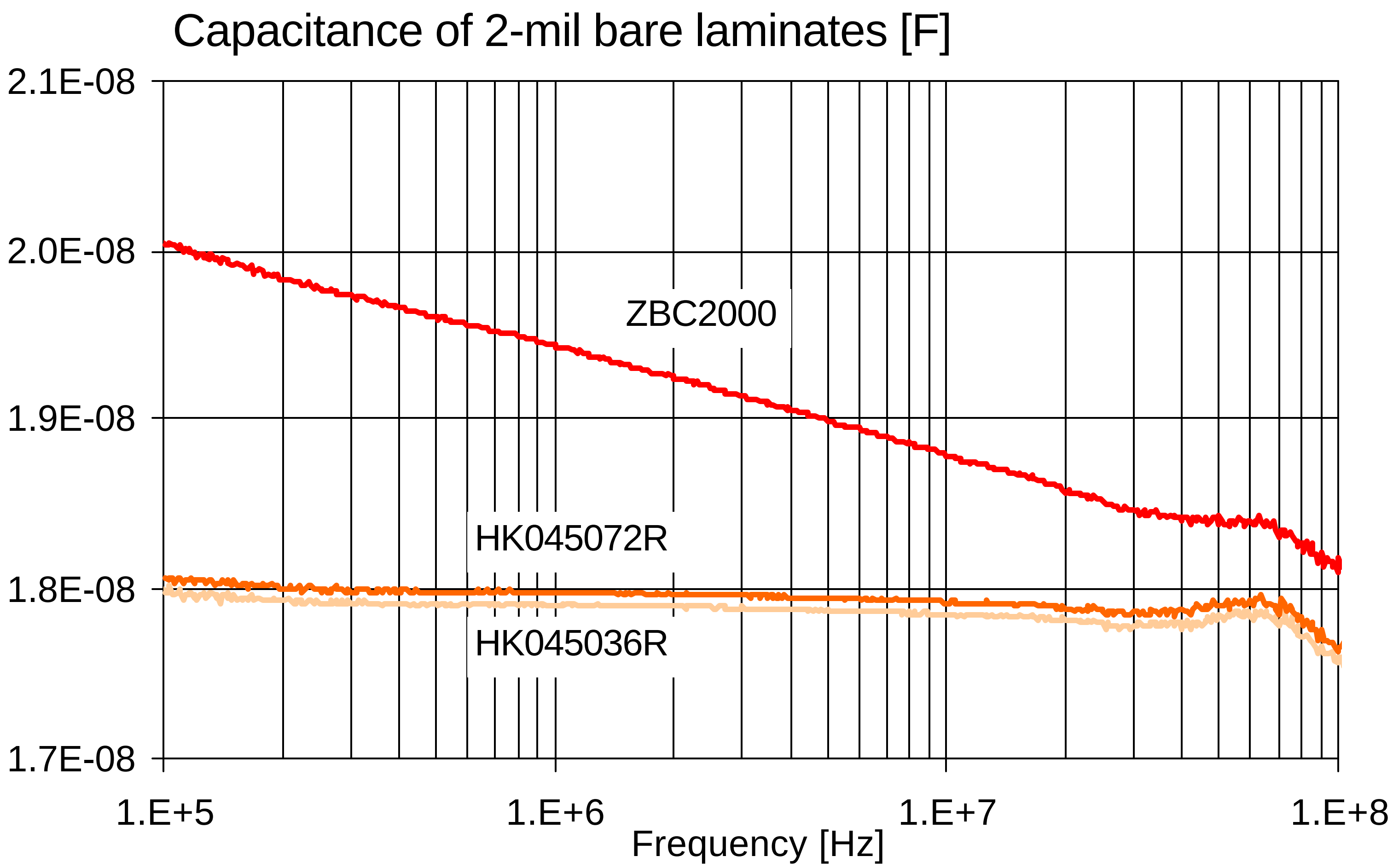
Shorted Board Inductance



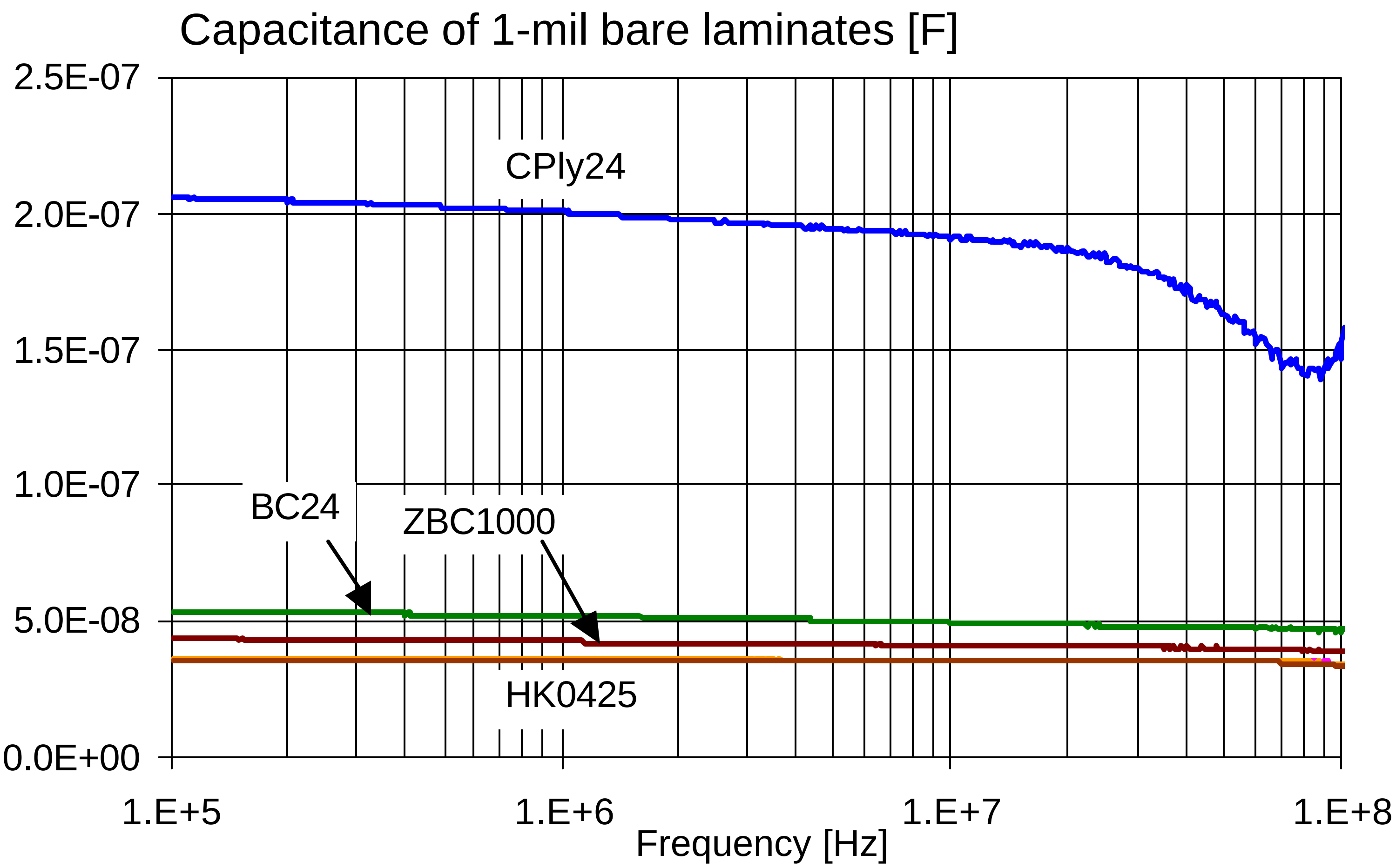
Capacitance of Open Boards



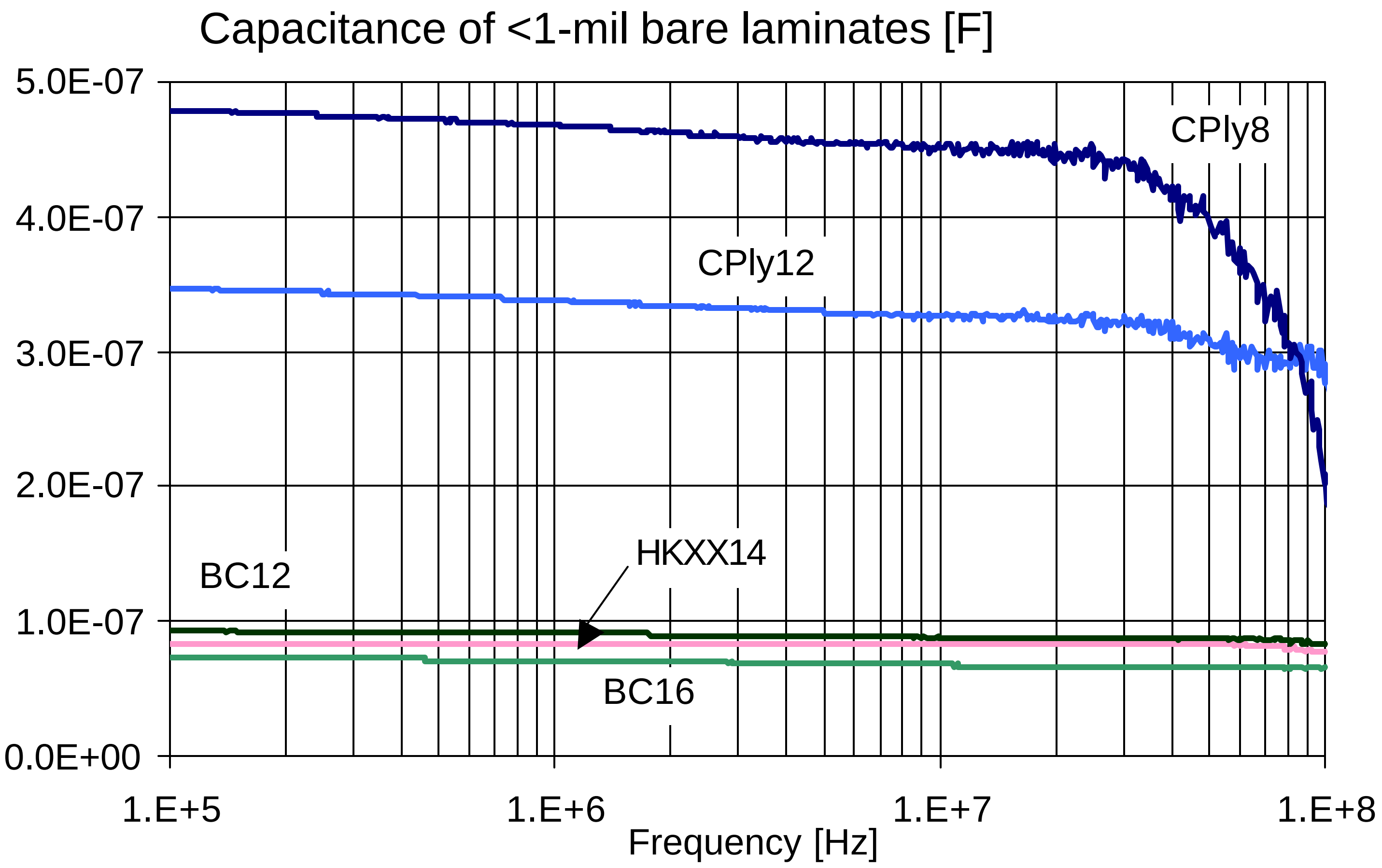
Capacitance of 2-mil Boards



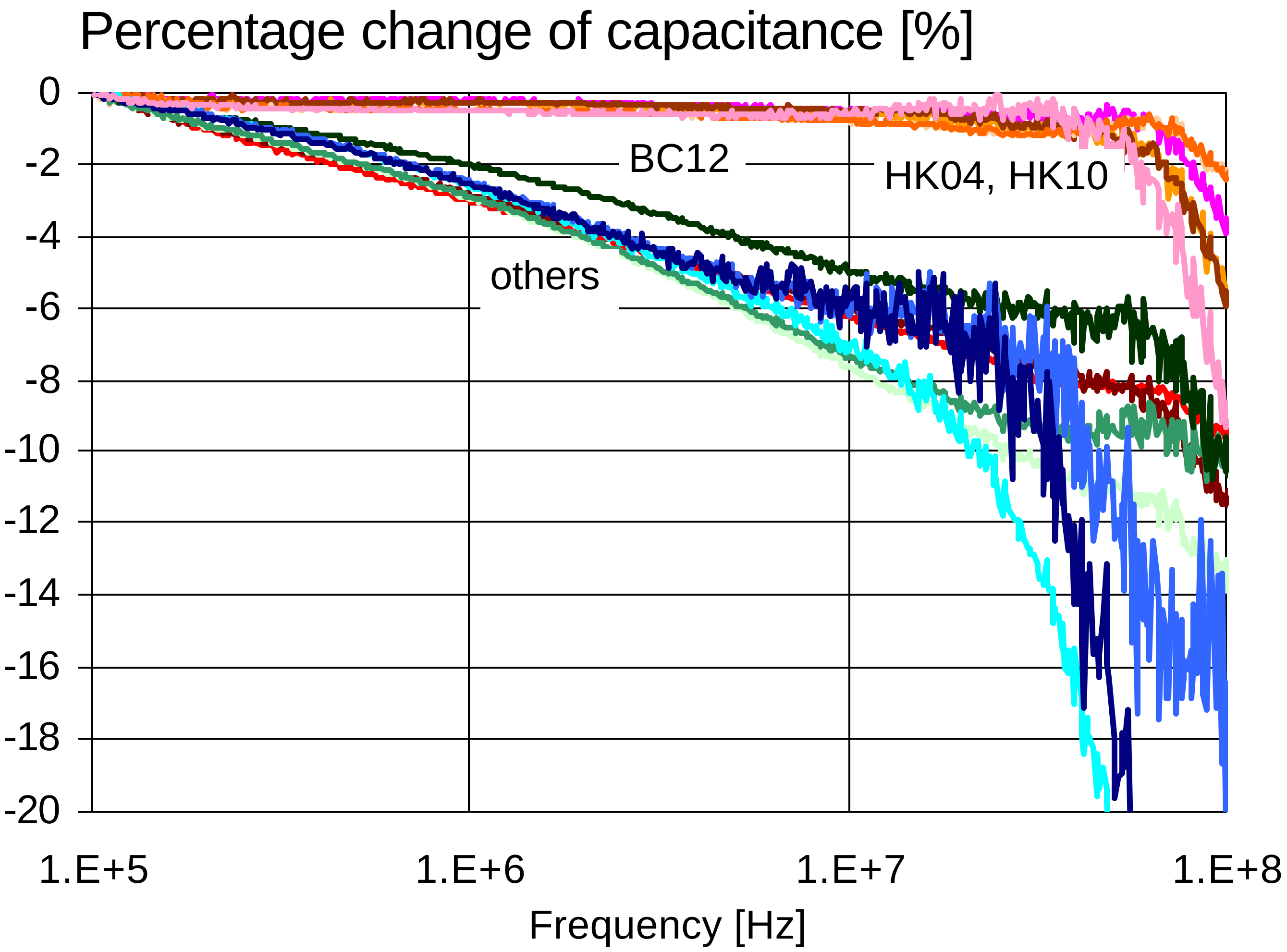
Capacitance of 1-mil Boards



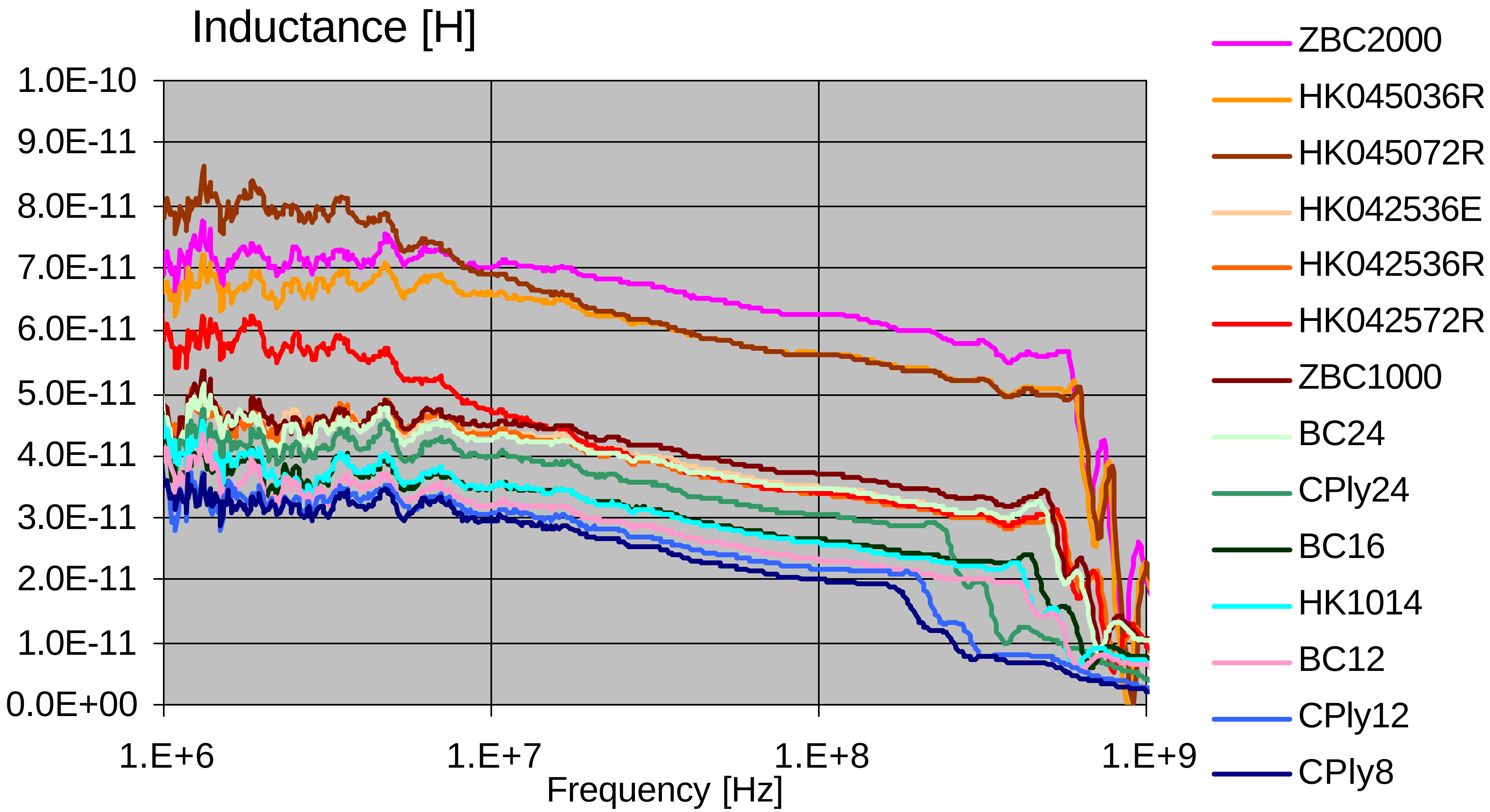
Capacitance of <1-mil Boards



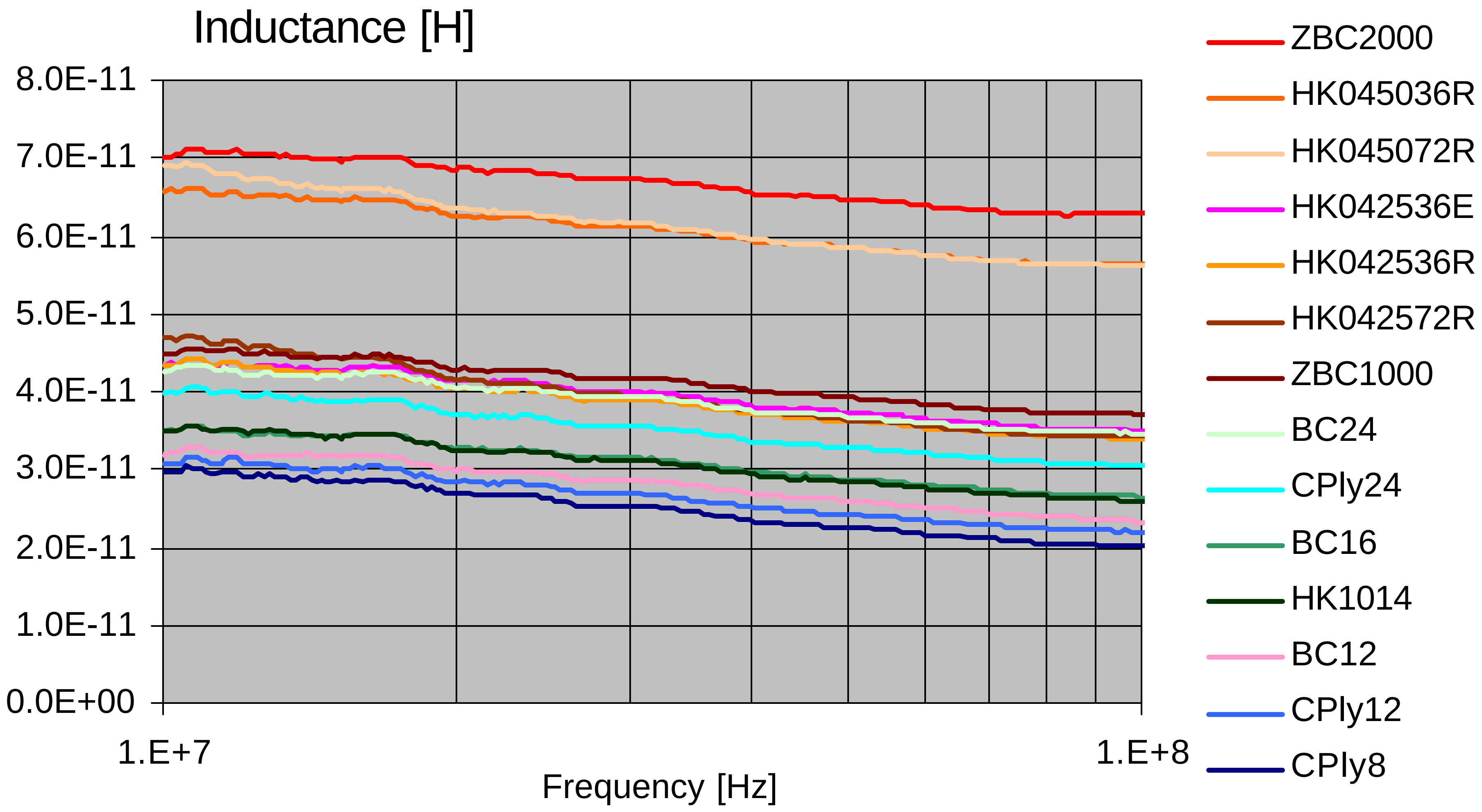
Relative Change of Capacitance



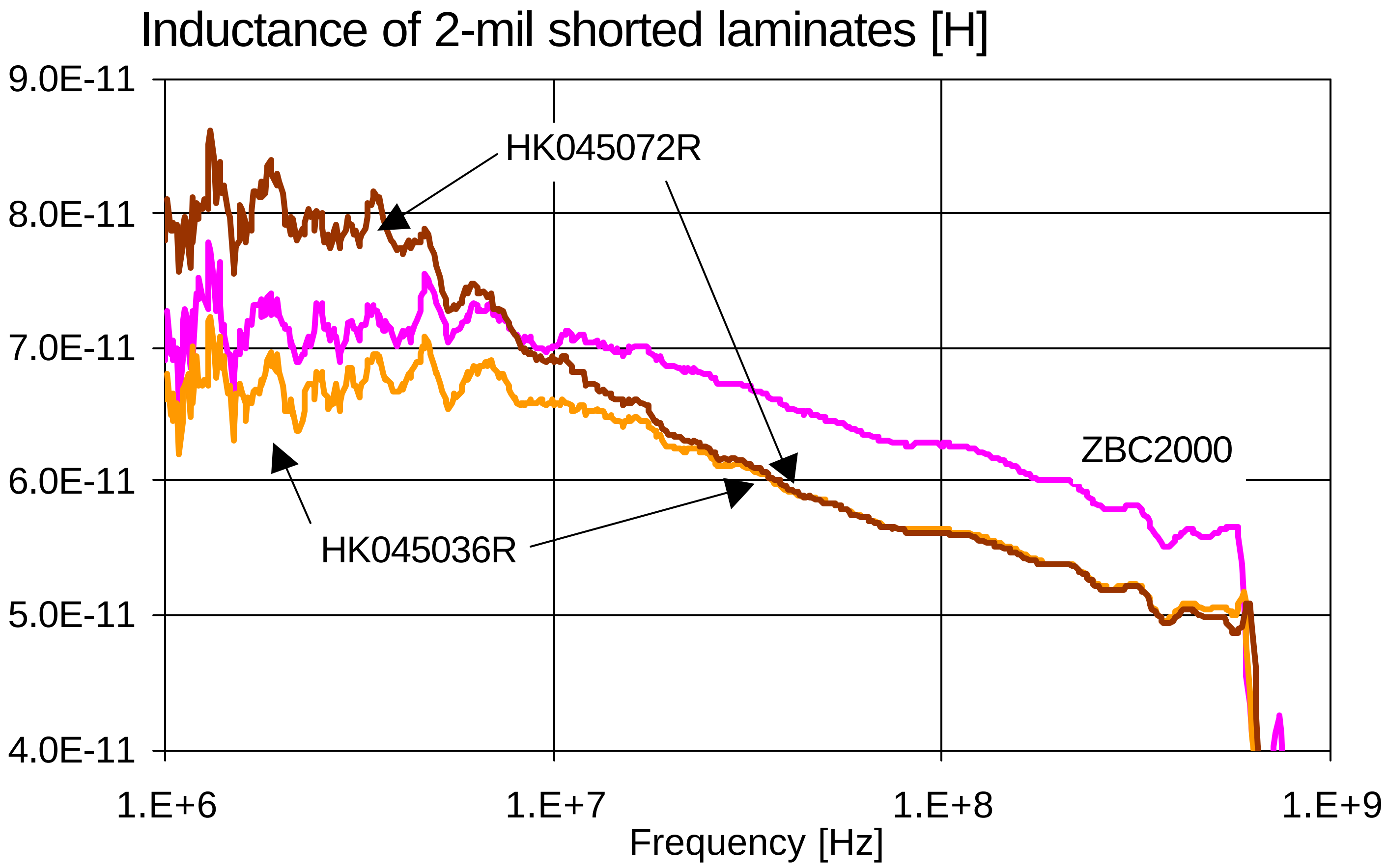
Inductance of Shorted Boards (1)



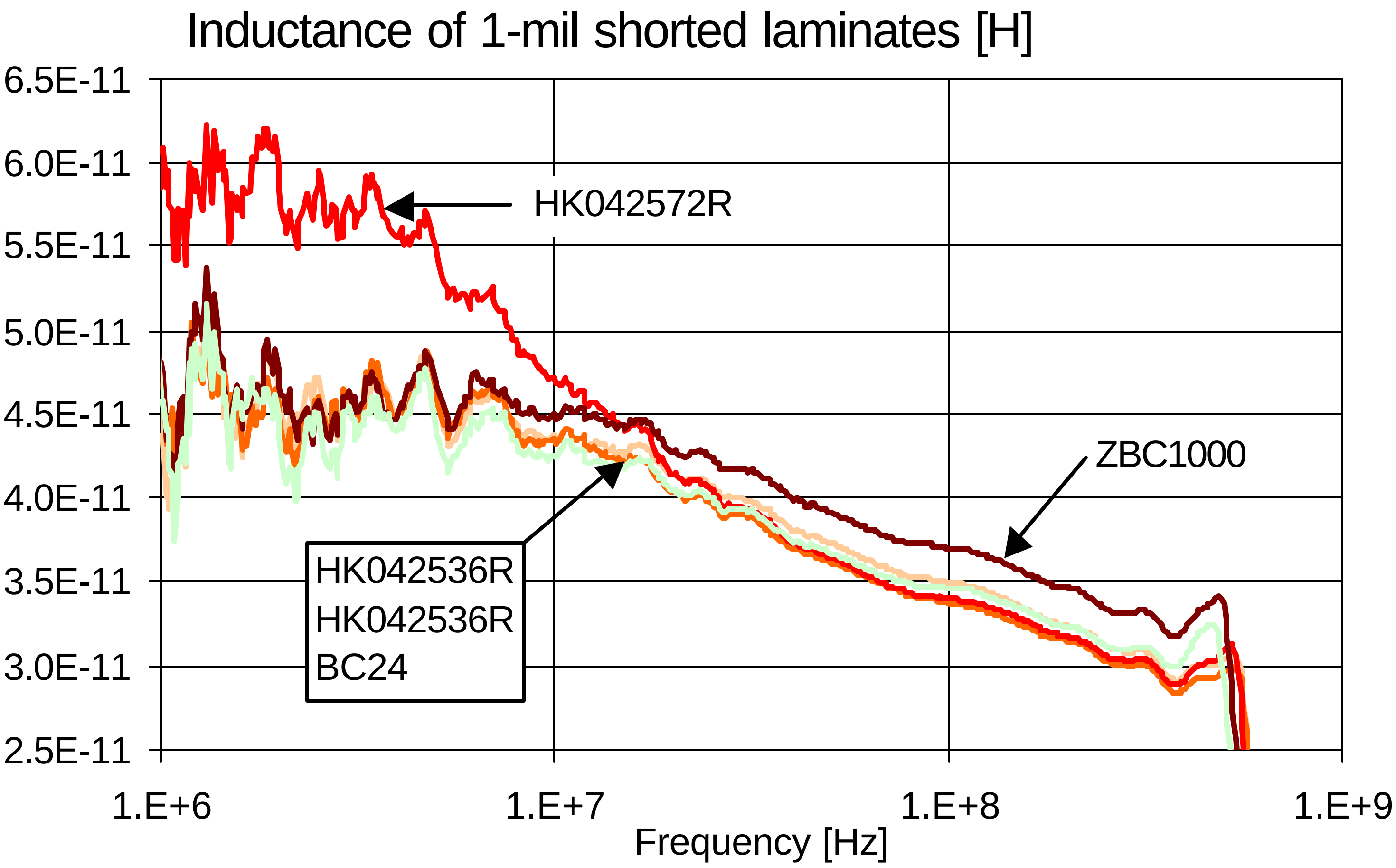
Inductance of Shorted Boards (2)



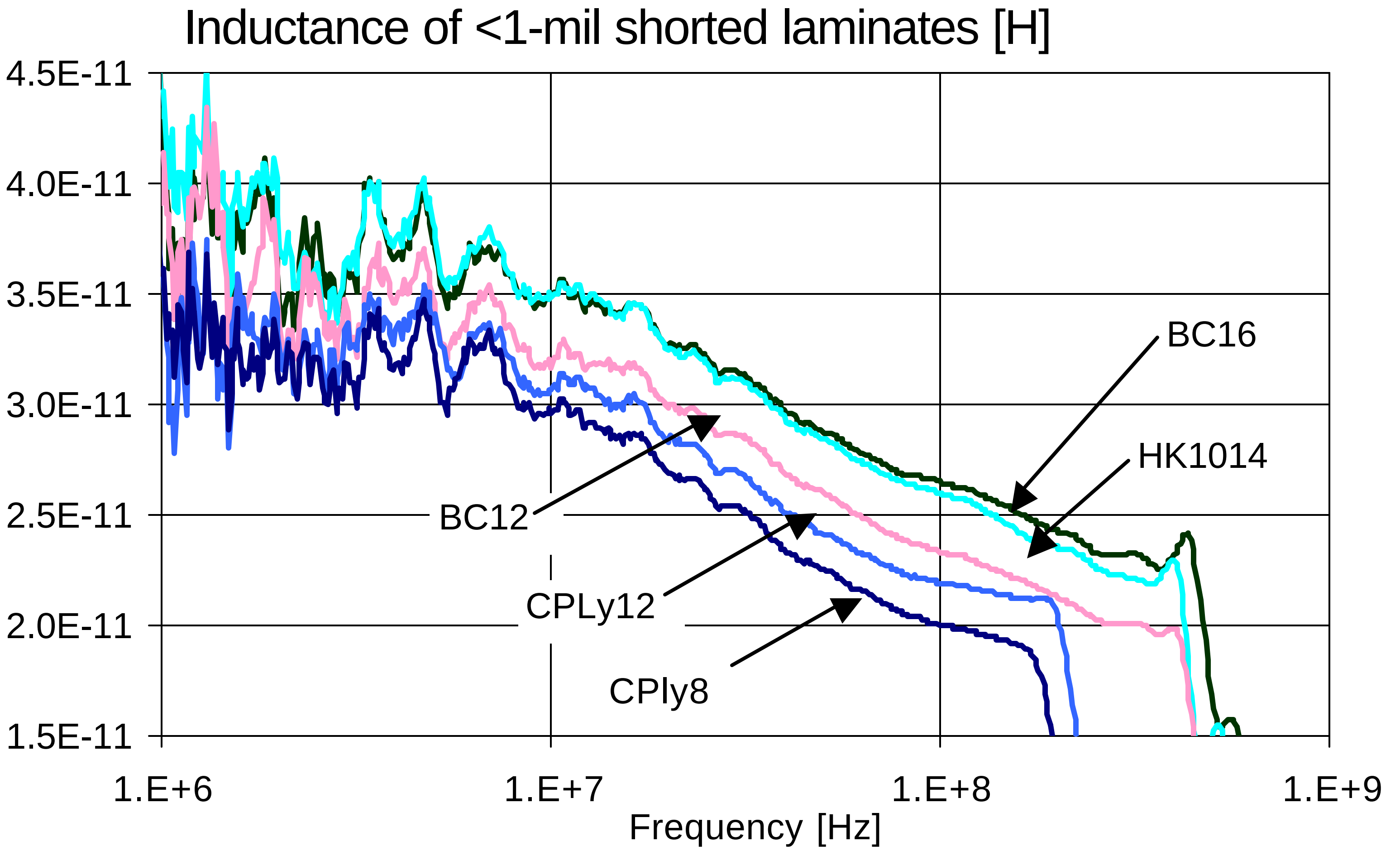
Inductance of Shorted 2-mil Boards



Inductance of Shorted 1-mil Boards



Inductance of Shorted <1-mil Boards



Conclusions

Capacitance of bare boards drops with frequency

  - -3%/decade for resin laminates
  - <1%/decade for polyimide

Inductance of shorted boards

  - varies with copper/laminate thickness
  - drops with frequency