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DC Bias Effect in Ceramic Capacitors

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The density of multi-layer ceramic capacitors (MLCC) has increased tremendously over the years. While fifteen years ago a state of the art X5R 10V 0402 (EIA) size capacitor might have had a maximum capacitance of 0.1 uF, today the same size capacitor may be available with 10 uF capacitance. This huge increase in density unfortunately comes with a very ugly downside: the capacitance is now very sensitive to DC and AC bias across the part.

MLCCs are manufactured with different types of ceramics. With a given case size, dielectric thickness and plate count, the capacitance is proportional to the dielectric constant of the ceramic: the higher the dielectric constant, the more capacitance we get from the same structure. For low loss, high-performance RF and microwave applications Class 1 materials are used [1]. These provide very good and stable electrical characteristics, practically zero bias and temperature dependence, but their relative dielectric constant is below 100 and hence capacitance density is low. In a 0402-size package we may get 1000 pF with 50V rating. If we need more capacitance in a small package, we have to select Class 2 (or Class 3) ceramics [2], which are ferroelectric materials with a dielectric constant in the 200 to 14000 range.

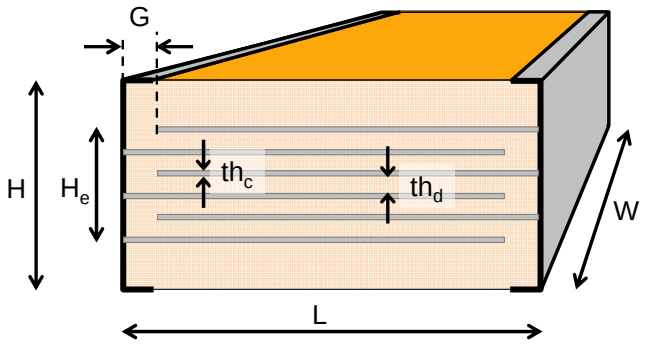

***Figure 1**: Approximate internal geometry of MLCC.*

A typical two-terminal MLCC internal geometry is shown in *Figure 1*. The two vertical metal terminals connect every other horizontal plate, creating a number of parallel-connected parallel-plate capacitor segments. The stack of capacitor plates fills the *H* total

capacitor body height with an effective height of H_e. The non-connected capacitor plates should not come out to the sidewall of the capacitor body, they are pulled back to create a small *G* gap. If for now we ignore these gaps and consider $H=H_e$ and $G=0$, each pair of adjacent capacitor plates creates a C_u unit capacitance:

$$C_u = \varepsilon_0 \varepsilon_r \frac{LW}{th_d}$$

where ε_0 is the dielectric constant of vacuum, or 8.85 pF/m, and ε_r is the relative dielectric constant of the ceramic material. In the capacitor body altogether we have *N* plate pairs, where *N* (if we ignore the end effects) can be approximated with

$$\mathrm{N} = \frac{\mathrm{H}}{\mathrm{th_d} + \mathrm{th_c}}$$

The total capacitance from the *N* pairs of capacitor plates gives us the following formula:

$$C = \varepsilon_0 \varepsilon_r \frac{LWH}{th_d(th_d + th_c)}$$

In the above expression the *LWH* product is the volume of the capacitor body. For regular ceramic capacitors the *H* height typically does not exceed the *W* width, and for a given case size this creates the LW^2 upper limit for the volume. To increase capacitance, either the ε_r relative dielectric constant has to increase, or the th_d and/or th_c thickness values have to decrease. In case the conductor thickness is much less than the dielectric thickness, the capacitance grows with the inverse square of the dielectric thickness. This gives a convenient scaling possibility to improve the volumetric density of ceramic capacitors: if we use thinner dielectric layers, in the given case size we can produce more and more capacitance.

However, as we make each dielectric layer thinner, the *E* field strength from the same *V* voltage applied across the part grows proportionally:

$$E = \frac{V}{th_d}$$

Also, if we increase the ε_r dielectric constant, the *D Electric Displacement Field* will grow proportionally:

$$D = \varepsilon_0 \varepsilon_r E$$

If we plot the relationship between *E* and *D* in high dielectric constant ferroelectric materials (see *Figure 2*), *D* will not follow it proportionally and eventually the curve flattens out, which is called saturation.

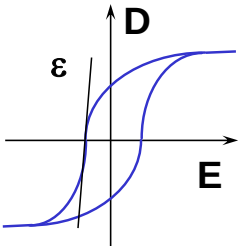

Figure 2: *Relationship between the E and D fields in ferroelectric materials.*

Over the many years as we, the users, kept asking for more capacitance in the same package, this scaling helped the industry to give us what we asked for. But we get not only more capacitance, we also get more bias sensitivity. Today the detailed data sheets from major MLCC vendors give us the typical bias sensitivity we can expect from MLCC parts, but unfortunately this kind of data is not a guaranteed specification. In case we want to collect our own data, the techniques and instrumentation is available in professional form [4]. When we look at the data sheet values or at our own measured data [5], we can see in some applications we can easily loose up to 80% of the capacitance just to DC bias effects.

We can also use simple home-made equipment to measure complex reflections and complex impedance and from that we can back-calculate capacitance. *Figure 3* shows the DC bias effect measured with a home-made vector-network analyzer on a 100 uF MLCC.

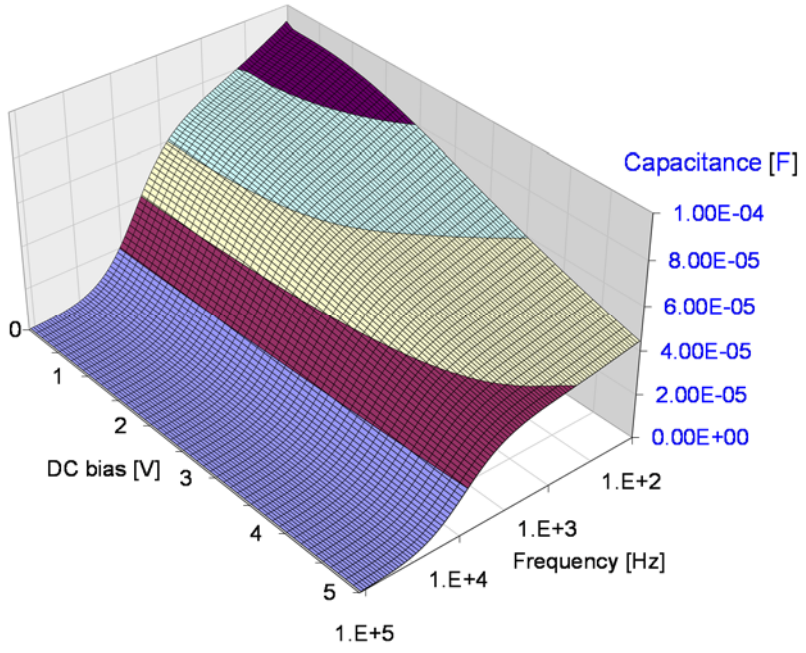

Figure 3: *Capacitance as a function of frequency and DC bias. Measured on a 100 uF 4V Class 2 MLCC part.*

The 3D surface is put together from multiple individual frequency sweeps, each with a different DC bias value across the capacitor. The DC bias voltage is shown on the left axis; the right axis shows frequency. Note that the capacitance depends not only on the bias voltage, but also on frequency. None of these dependencies are present in Class 1 ceramic capacitors. *Figure 4* shows the bias-dependence surface for a 0.1 uF COG MLCC.

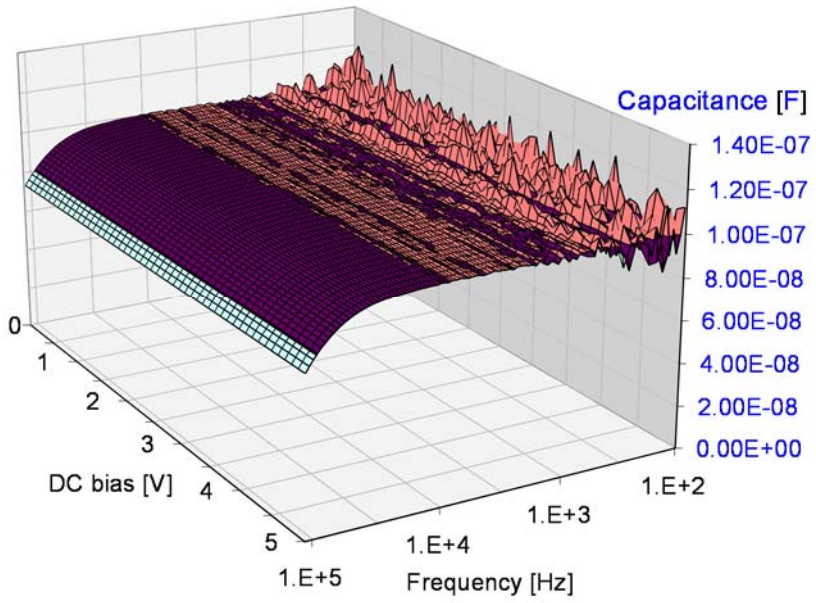

Figure 4: *Capacitance as a function of frequency and DC bias. Measured on a 0. 1 uF Class 1 MLCC part.*

The 3D surface of *Figure 4* is flat in both directions until we start approaching the series resonance frequency of the part. There is an increasing noise on the measured surface at very low frequencies. At 100 Hz the impedance magnitude of a 0.1 uF capacitor is more than 10 kOhm. The noise illustrates the limitation of the simple home-made instrumentation when we try to measure kilo-ohm impedance values in two-port shunt-through connection.

So be careful when you use a 6.3V rated Class 2 ceramic capacitor in a 5V application: a big percentage of the capacitance may be gone. The good news is that this bias dependence is hardly present in tantalum and aluminum capacitors, film capacitors and printed-circuit laminates.

References

[1] http://en.wikipedia.org/wiki/Ceramic_capacitor#Class_1_ceramic_capacitors
[2] http://en.wikipedia.org/wiki/Ceramic_capacitor#Class_2_ceramic_capacitors
[3] http://en.wikipedia.org/wiki/Permittivity
[4] "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," DesignCon 2010, February 1-4, 2010, Santa Clara, CA.

Available at http://www.electrical-integrity.com/Paper_download_files/DC10_12-TH3_Novak-Mori-Resso.pdf

[5] "DC and AC Bias Dependence of Capacitors Including Temperature Dependence," DesignCon East 2011, September 27, 2011, Boston, MA. Available at http://www.electrical-integrity.com/Paper_download_files/DCE11_200.pdf