Vias structural details and its effect on System performance

Roger Dame, Principal Engineer, Oracle Corporation
Gustavo Blando, Principal Engineer, Oracle Corporation
Istvan Novak, Senior Principal Engineer, Oracle Corporation
Jason Miller, Principal Engineer, Oracle Corporation
Kevin Hinckley, Principal Signal Integrity Engineer, Oracle Corporation

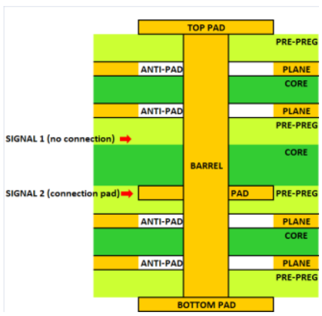
Agenda

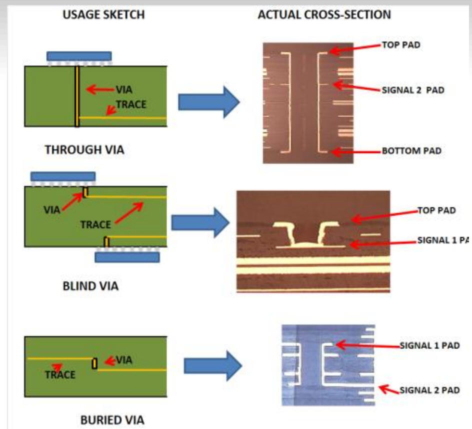
- Anatomy of a via
- Via performance
- Frequency and Time domains
- Fast Edge Rate TDR techniques
- 50X scaled measurements
- Conclusion

2

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

Anatomy of a via



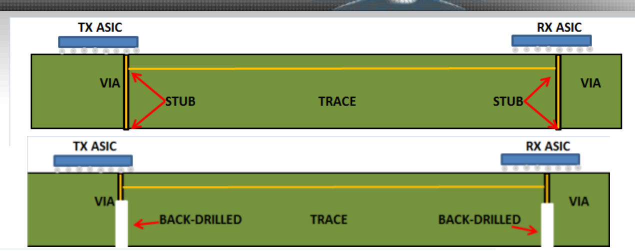


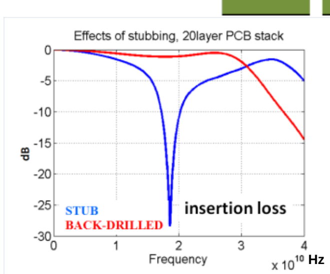
UBM Electronics

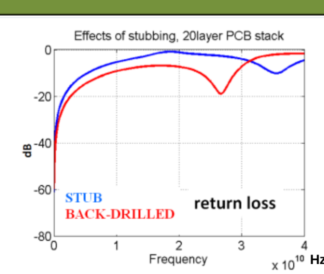
DESIGNCON 2012
WHERE CHIPHEADS CONNECT

VIA PERFORMANCE

Affects of stubbing on transition vias.



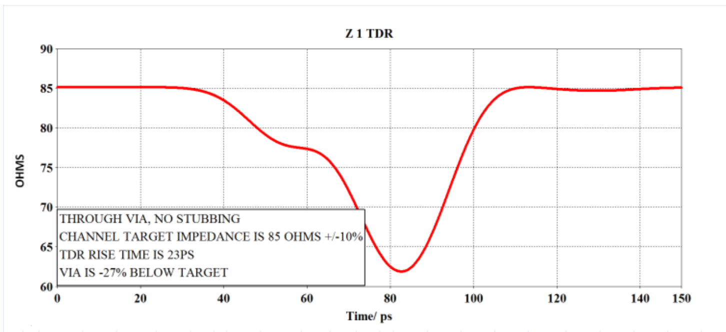




UBM Electronics

VIA PERFORMANCE

Impedance mis-match on through vias



UBM Electronics 5

VIA PERFORMANCE

We can summarize via performance within two major categories:

<u>**Gross Discontinuities**</u>**: via stubbing, special pads and other structures causing major resonances.**

<u>**Impedance Discontinuities**</u>**: pads, stack symmetry, and the number of planes subtly affect impedance.**

The primary objective is to make vias seamless and inert in the channel… like the trace it connects.

UBM Electronics 6

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

Frequency versus Time Domains

Exploring Via sub-structures

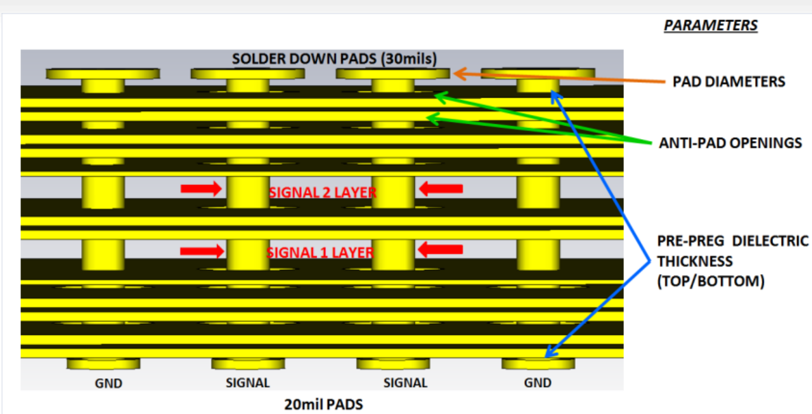
Can we use frequency--time or both domains to reveal via sub-structures and their affects so as to help us optimize via performance?

We will explore these domains using a 3D solver.

UBM Electronics 7

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

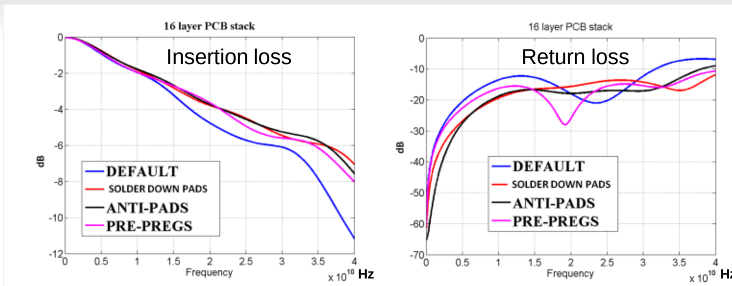
Frequency domain: 16 layer stack



UBM Electronics 8

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

Insertion and return loss versus parameter changes:



VIA sub-structural parameters

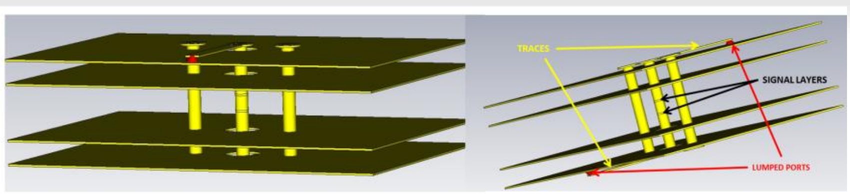
structures	default		adjusted to	
ANTI-PADS	28	mils	40	mils
SOLDER DOWN PADS	30	mils	20	mils
PRE-PREGS (TOP/BOTTOM)	3.5	mils	12.5	mils

Insertion loss trends are expected,
but no clear relations to the sub-structures can be observed.

UBM Electronics

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

Frequency domain: simple 8 layer stack:



Let's test more structural changes
one parameter at a time.

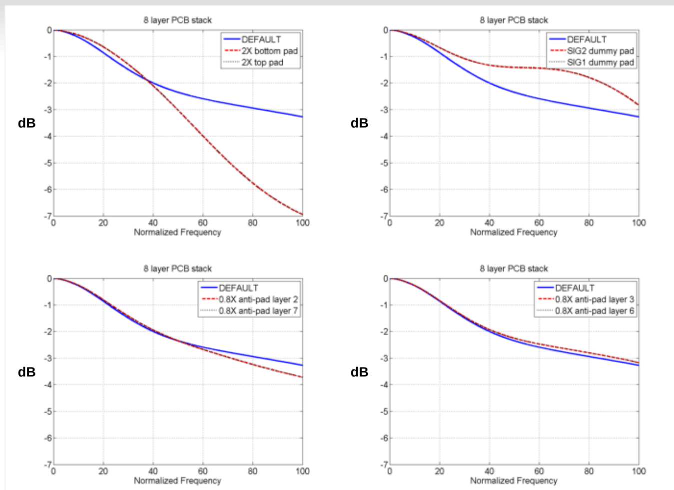
VIA sub-structural parameters

structures	scale from default	
top pad	2	X default
anti-pad GND4	0.8	X default
anti-pad GND3	0.8	X default
signal 1 dummy1 pad	4	X barrel diam
signal 2 dummy2 pad	4	X barrel diam
anti-pad GND2	0.8	X default
anti-pad GND1	0.8	X default
bottom pad	2	X default

UBM Electronics

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

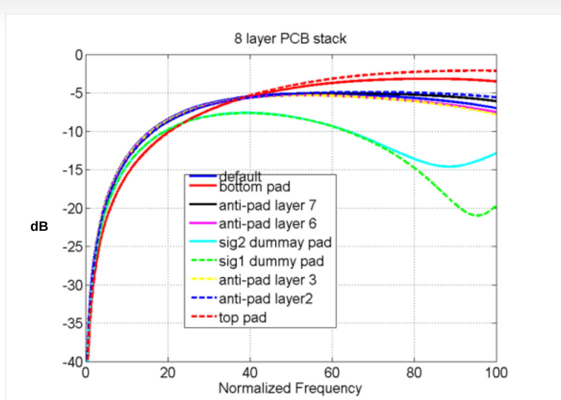
Insertion loss versus parameter changes:



UBM Electronics 11

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

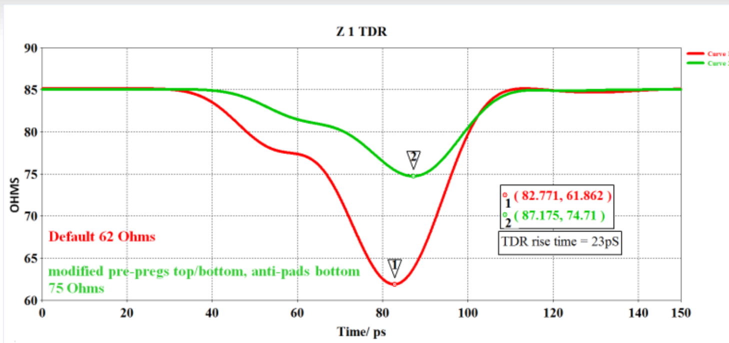
Return loss versus parameter changes:



UBM Electronics 12

DesignCon 2012
WHERE CHIPHEADS CONNECT

Time domain: 16 layer stack



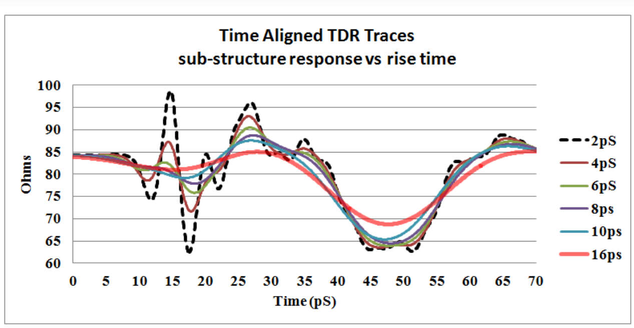
Impedance target is 85 ohms, contrasting the default structure against two parameter changes with a Trise of 23ps.

What do we see using faster rise times?

UBM
Electronics 13

DesignCon 2012
WHERE CHIPHEADS CONNECT

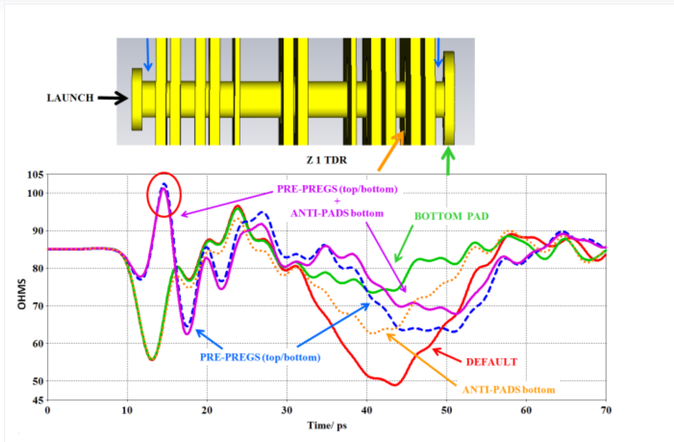
Time domain: 16 layer stack, TDR response vs Trise



Fast Edge Rate TDR (FER) exposes detail. But can we use this?

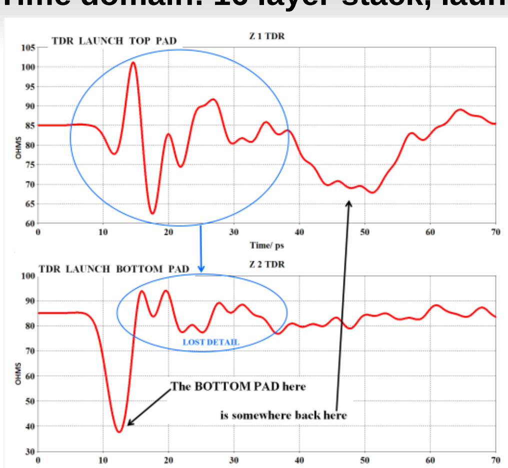
UBM
Electronics 14

Time domain: 16 layer stack, 3 parameter changes



UBM Electronics 15

Time domain: 16 layer stack, launch vs big discontinuities

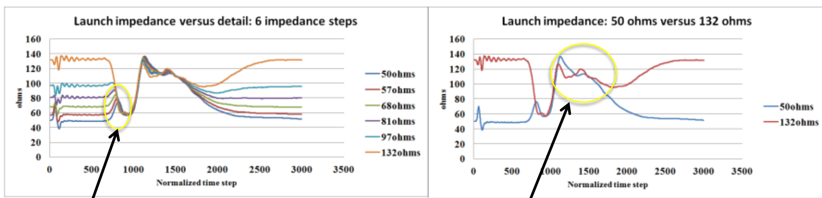


Launch the TDR at both ends, detail can get lost.

UBM Electronics 16

DesignCon 2012
WHERE CHIPHEADS CONNECT

Time domain: 8 layer stack, launch impedance also impacts detail



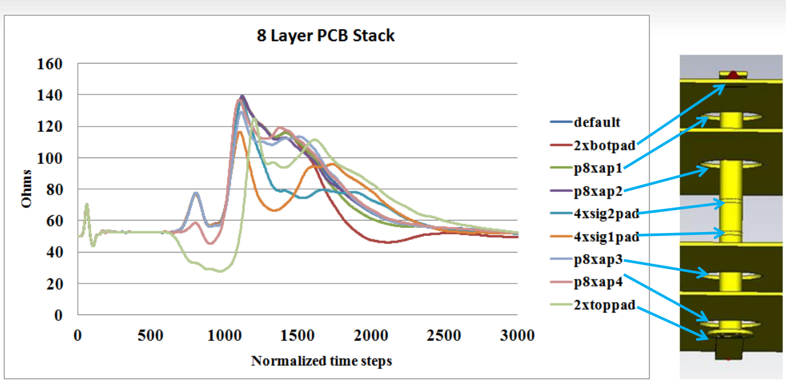
Lost detail with high launch impedance

New detail with high launch impedance

UBM Electronics

DesignCon 2012
WHERE CHIPHEADS CONNECT

Time domain: 8 layer stack, stepping through 8 parameter changes

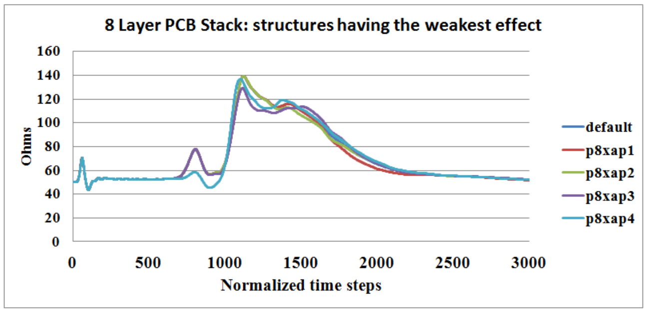


A bit messy, let's sort the sub-structures. Our target impedance is 50 ohms.

UBM Electronics

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

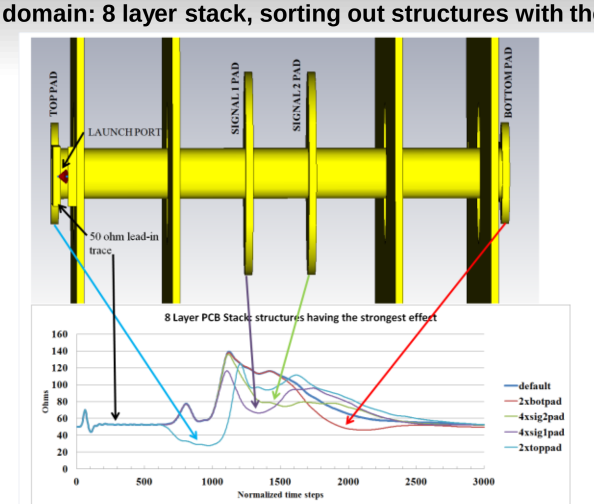
Time domain: 8 layer stack, sorting out structures with the least impact



UBM Electronics 19

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

Time domain: 8 layer stack, sorting out structures with the most impact



UBM Electronics 20

FER TDR Optimization

We need to consider physical measurements using standard TDR equipment. But how are we going to physically generate a 2ps edge rate?

The answer lies in the power of scaling…..

FER TDR Optimization: 50X 3D and Physical models

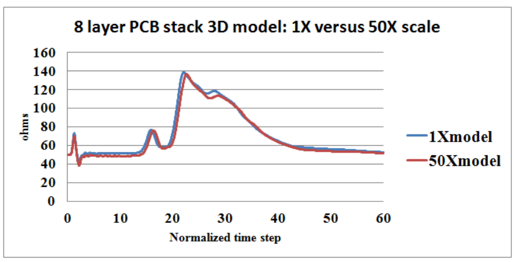
We will use the simple 8 layer stack for these exercises.

FER TDR Optimization:

1X 50X dimensional details
3D model correlation

STACK DETAILS		1X	50X model	
metal layers	material	thickness	thickness	
1	top	1.44	72	mils
	pre-preg	3	150	mils
2	ref	1.44	72	mils
	core	17	850	mils
3	ref	1.44	72	mils
	pre-preg	13.8	690	mils
4	signal 1	1.44	72	mils
	core	10.96	548	mils
5	signal 2	1.44	72	mils
	pre-preg	13.8	690	mils
6	ref	1.44	72	mils
	core	17	850	mils
7	ref	1.44	72	mils
	pre-preg	3	150	mils
8	bot	1.44	72	mils
	total	90.08	4504	mils

STRUCTURE DETAILS	1X	50X model	
via barrel diameter	10	500	mils
top/bottom pads	20	1000	mils
anti-pads	28	1400	mils
trace width	11.5	575	mils
trace thickness	1.44	72	mils
trace length	78.2	3911	mils
plane width	300	15000	mils
plane length	200	10000	mils



Compare FER TDR traces for the 1X vs the 50X 3D scaled model.

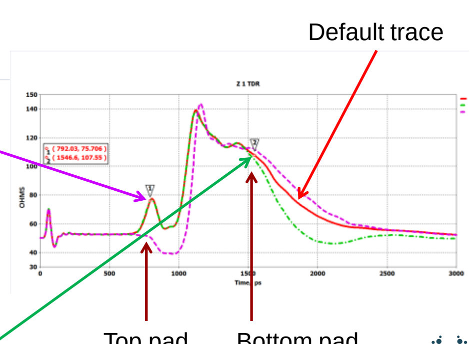
1X: Trise=600fs
50X: Trise=30ps

UBM Electronics

FER TDR Optimization: (50X) Calibrating the TDR trace

ϵ=1 (air), Tpd~85ps/inch

		50X model		accumulated delay from launch	measured	
starting time				0	792.03	pS
metal layers	material	thickness				
1	top	72	mils	12.24		pS
	pre-preg	150	mils	37.74		pS
2	ref	72	mils	49.98		pS
	core	850	mils	194.48		pS
3	ref	72	mils	206.72		pS
	pre-preg	690	mils	324.02		pS
4	signal 1	72	mils	336.26		pS
	core	548	mils	429.42		pS
5	signal 2	72	mils	441.66		pS
	pre-preg	690	mils	558.96		pS
6	ref	72	mils	571.2		pS
	core	850	mils	715.7		pS
7	ref	72	mils	727.94		pS
	pre-preg	150	mils	753.44	1546.6	pS
8	bot	72	mils	765.68	12.24	pS estimated
	total	4504	mils	765.68	766.81	pS

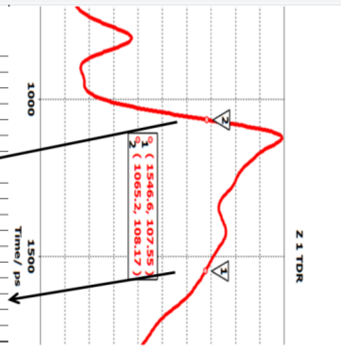


UBM Electronics

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

FER TDR Optimization: (50X) locating the large impedance discontinuity

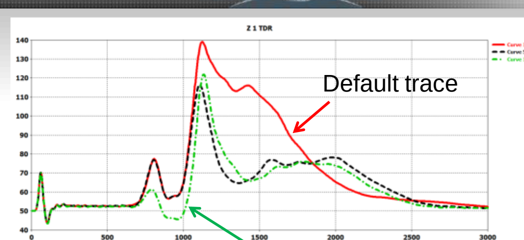
		50X model		accumulated delay from launch	measured	
starting time				0	792.03	pS
metal layers	material	thickness				
1	top	72	mils	12.24		pS
	pre-preg	150	mils	37.74		pS
2	ref	72	mils	49.98		pS
	core	850	mils	194.48		pS
3	ref	72	mils	206.72	1065 - 792	
	pre-preg	690	mils	324.02	273	pS
4	signal 1	72	mils	336.26		pS
	core	548	mils	429.42		pS
5	signal 2	72	mils	441.66		pS
	pre-preg	690	mils	558.96		pS
6	ref	72	mils	571.2		pS
	core	850	mils	715.7		pS
7	ref	72	mils	727.94		pS
	pre-preg	150	mils	753.44	1546.6	pS
8	bot	72	mils	765.68	12.24	pS
	total	4504	mils	765.68	766.81	pS



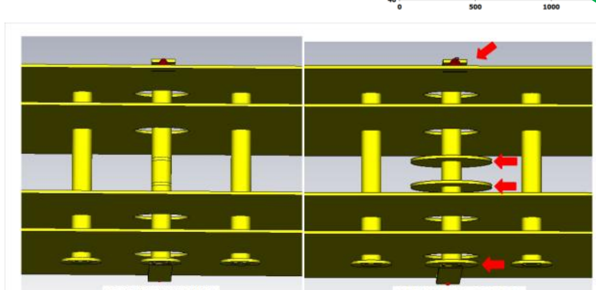
UBM Electronics

DESIGNCON 2012
WHERE CHIPHEADS CONNECT

FER TDR Optimization: (50X) best solution



Default trace



Increased top/bottom pads
Added dummy signal pads

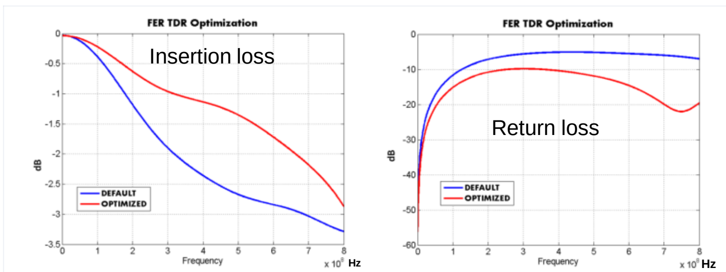
UBM Electronics

DESIGNCON 2012

WHERE CHIPHEADS CONNECT

FER TDR Optimization: (50X) back to the Frequency domain

How well did we do?



~1.2dB improvement @ 400MHz ~5.3db improvement @ 400MHz

UBM Electronics 27

DESIGNCON 2012

WHERE CHIPHEADS CONNECT

50X Physical Model Correlation: considerations

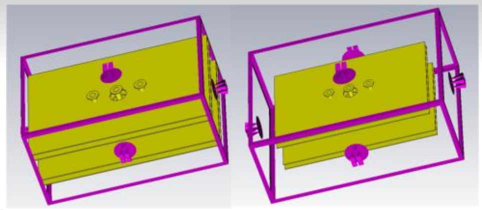
- **Absorbing boundary issue**
- **Flexibililty**
- **Simple construction**

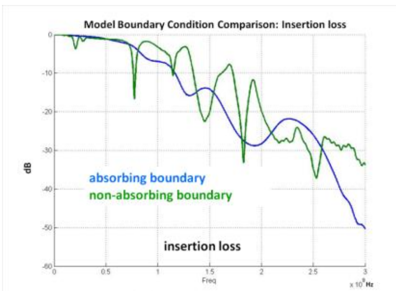
UBM Electronics 28

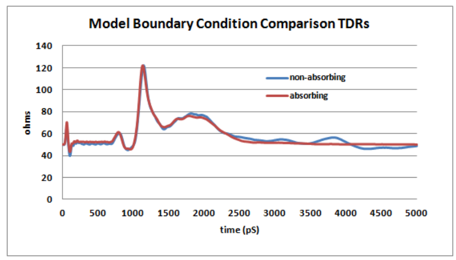
DESIGNCON 2012
WHERE CHIPHEADS CONNECT

50X Physical Model Correlation:

Absorbing boundaries: frequency vs time domains



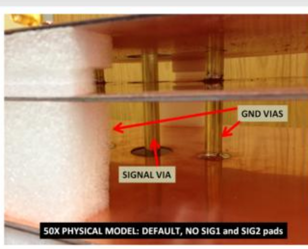


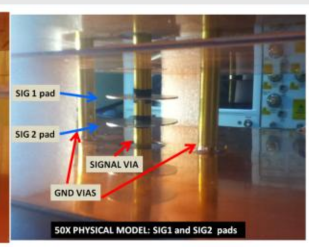


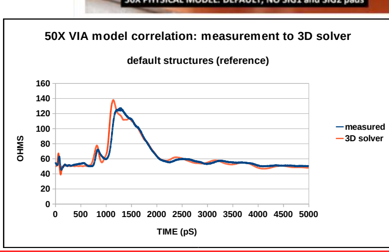
UBM Electronics 29

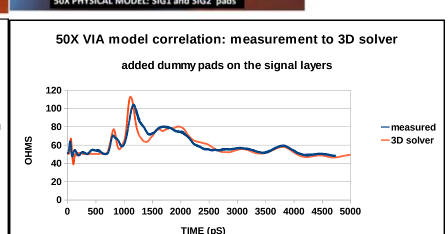
DESIGNCON 2012
WHERE CHIPHEADS CONNECT

50X Physical Model Correlation: 3D vs physical, default and 1 parameter change









UBM Electronics 30

Conclusions:

- **Frequency domain does not provide sub-structure detail.**
- **Time domain using Fast Edge Rate TDR in simulation can reveal significant detail of a via's sub-structure.**
- **A simple process using this technique was demonstrated.**
- **The technique has been demonstrated against a 50X physical model.**