DesignCon 2016

Target Impedance and Rogue Waves

Panel discussion

Eric Bogatin, Teledyne LeCroy, moderator
Istvan Novak, Oracle
Steve Sandler, PicoTest
Larry Smith, Qualcomm
Brad Brim, Cadence
the empty chair, in memoriam Steve Weir

Abstract

The target impedance concept has been used by the industry for a number of years. It is the basis of a simple and robust design process, but it assumes a smooth flat impedance profile. Looking out from the silicon, the impedance profile is never flat, which results in higher noise. Excitation patterns that can create the worst-case or almost-worst-case time-domain response of a power distribution network has gained a lot of interest in recent years. The peak value of the step response, the response to a repetitive excitation at a resonance peak as well as the absolute worst-case time-domain response are potentially producing results much worse than target impedance alone would imply. The panel will discuss how these are related, how the target impedance concept can be applied under such circumstances as well as providing tips for recognizing and avoiding rogue waves. Rogue wave measurements will also be shown.

Target Impedance and Rogue Waves

Istvan Novak, Oracle

Steve Sandler, PicoTest

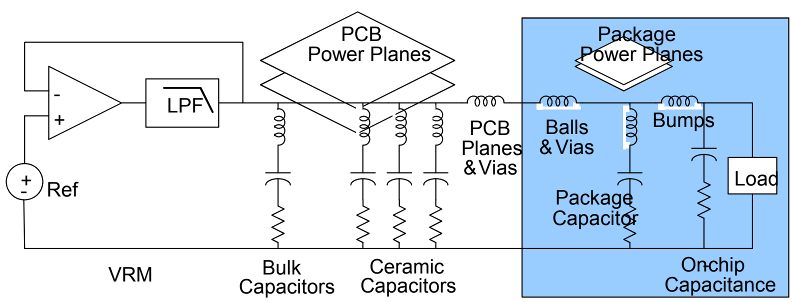
Larry Smith, Qualcomm

Brad Brim, Cadence

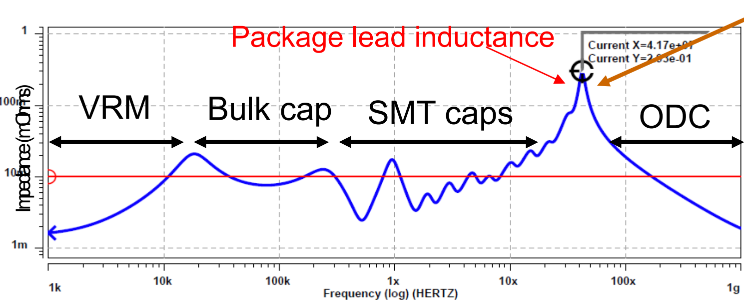
Eric Bogatin, Teledyne LeCroy, moderator

the empty chair, Steve Weir

An Important Lesson I learned from Steve Weir



What we see looking into the PDN from the Chip's perspective



The "Bandini Mountain"

- Steve Weir

Panel discussion: Target Impedance and Rogue Waves

How to Design with Target Impedance?

Istvan Novak, Oracle

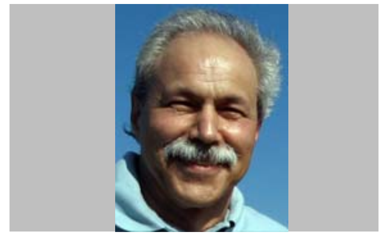
Panel discussion: Target Impedance and Rogue Waves

How to Design with Target Impedance?

Istvan Novak, Oracle

SPEAKERS

Istvan Novak
Senior Principal Engineer, Oracle
istvan.novak@oracle.com



Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

The Basics

- The Target Impedance concept relates supply noise to PDN (self) impedance
- Originally developed for single, point-of-load PDN
- Assumes:
  - Flat impedance profile in the entire frequency band of possible excitations
  - Linear and Time Invariant PDN
- Challenges:
  - One or both assumptions are usually not valid
- Questions:
  - Can we still use the Target Impedance concept?
  - If yes, how?

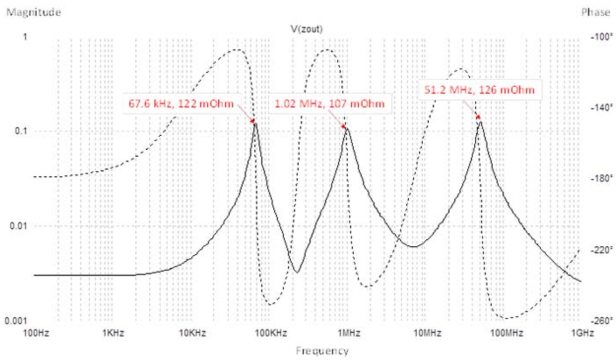
$$Z_{target} = \frac{\Delta V}{\Delta I}$$

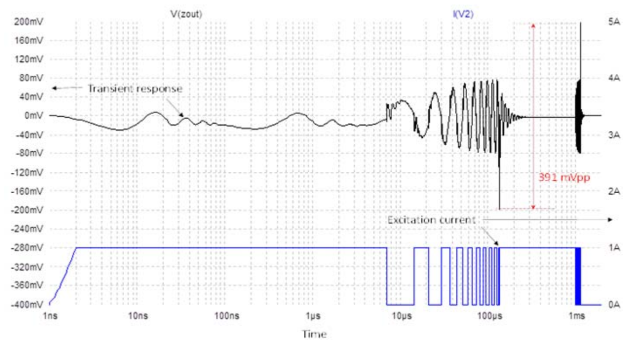
$$BW = \frac{1}{\pi\, t_{tr}}$$

For details, see [1]

Worst-Case PDN Noise Calculation

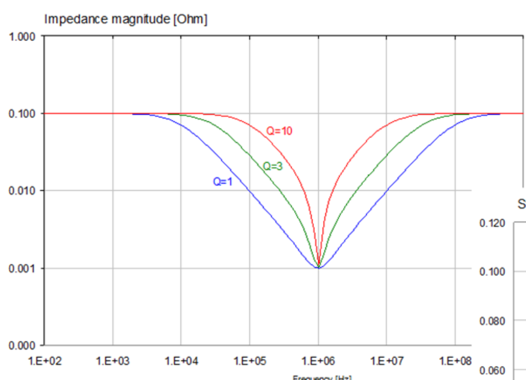
- Rogue wave vs. worst-case noise
- For Linear and Time Invariant self-impedance PDN, the worst-case noise can be calculated by the Reverse Pulse Technique



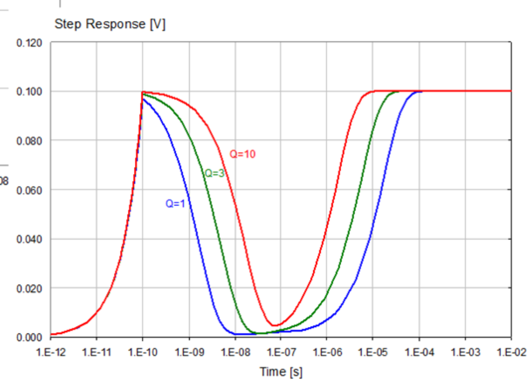


For details, see [2] and [3]

It is All About Impedance Flatness



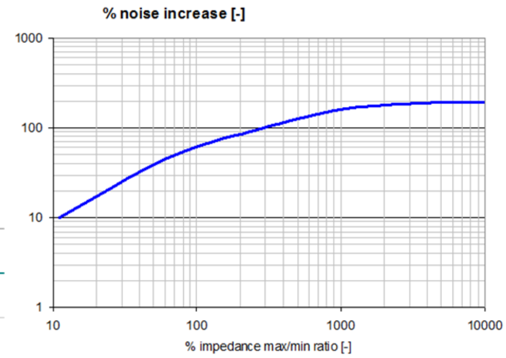
- All cases produce 290mVpp/A worst-case noise
- Conclusion: Q of dip does not matter

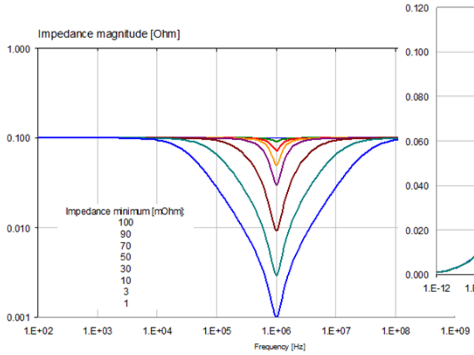


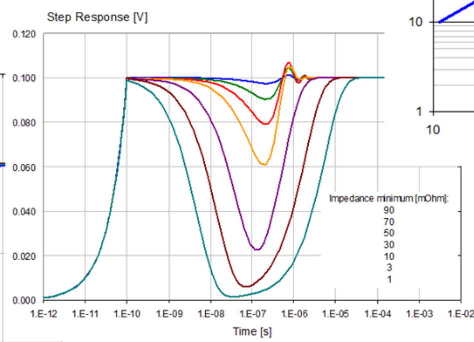
For details, see [4]

It is All About Impedance Flatness

- The cases produce different worst-case noise
- Conclusion: depth of dip matters
- Noise can be up to 3x higher

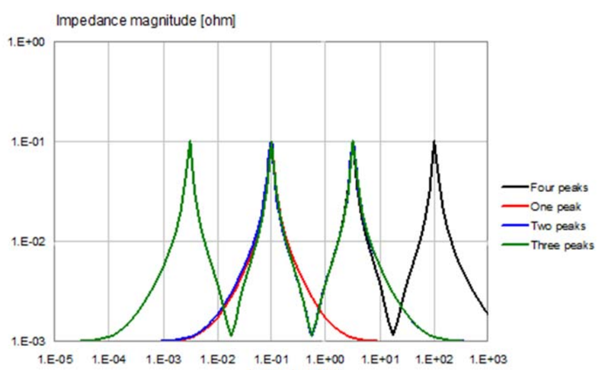




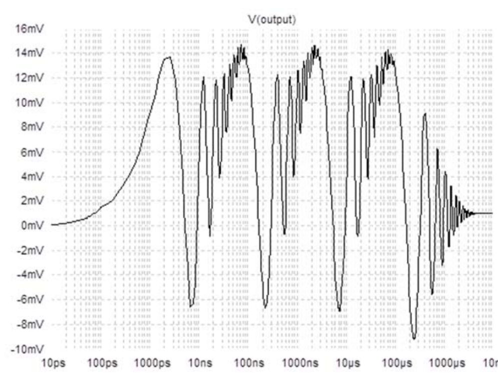


It is All About Impedance Flatness

- The cases produce different worst-case noise
- 120, 234, 346, 453 mVpp for 1, 2, 3 and 4 peaks, all with 100mOhm peak value
- Conclusion: number of peaks matters



Step Response with four impedance peaks



Is Target Impedance Useless ?

- NO, the target impedance is a very useful design tool
- How to do a systematic design based on target impedance and non-flat impedance?
  - Calculate your target impedance based on flat impedance and LTI assumptions
  - If you know your PDN design approach, select a corresponding correction factor
  - If you do not know your PDN design approach, a default correction factor of 3 is a safe starting point
  - Recalculate the target impedance based on the correction factor
  - Do the PDN design with the new (lower) target impedance
  - Check/validate the correction factor

Do You Need to Worry about Rogue Waves?

Not if you do the PDN design properly:

- You can estimate the worst-case noise for LTI PDNs with the Reverse Pulse Technique
- The primary concern should be impedance flatness (peaks and dips)
- The secondary concern should be LTI

MORE INFORMATION

References:

[1] Larry D. Smith, Raymond E. Anderson, Douglas W. Forehand, Thomas J. Pelc, and Tanmoy Roy, ‘‘Power distribution system design methodology and capacitor selection for modern CMOS technology’’, IEEE Transactions on Advanced Packaging, vol. 22, no. 3, pp. 284-291, Aug.1999.

[2] Drabkin, et al, “Aperiodic Resonant Excitation of Microprocessor power Distribution Systems and the Reverse Pulse Technique,” Proceedings of EPEP 2002, p. 175.

[3] Steve Sandler, “Target Impedance Limitations and Rogue Wave Assessments on PDN Performance,” paper 11-FR2 at DesignCon 2015, January 27 – 30, 2015, Santa Clara, CA.

[4] Systematic Estimation of Worst-Case PDN Noise: Target Impedance and Rogue Waves, QuietPower column, November 2015. Available at http://www.electrical-integrity.com/Quietpower_files/Quietpower-34.pdf

[5] How to Design a PDN for Worst Case?, QuietPower column, December 2015. Available at http://www.electrical-integrity.com/Quietpower_files/Quietpower-35.pdf

ORACLE

Thank you!

QUESTIONS?

UBM

Target Impedance and Rogue Waves

Steve Sandler, Picotest

DesignCon 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

UBM

Target Impedance and Rogue Waves

Steve Sandler, Picotest

DesignCon 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

INTRODUCTION

$$Z_{target} = \frac{\Delta V}{\Delta I}$$

Tolerable voltage noise

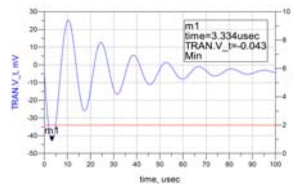
Expected current noise

$$\Delta V_{target} = Z_{target} \cdot \Delta I$$

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

Step

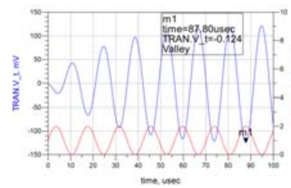
$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot e^{\frac{-\pi}{4Q}} = 39mVpk$$



$$\Delta I = 2Amps$$
$$\Delta V = 39mVpk$$

Resonant Sine

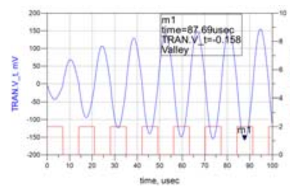
$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot \frac{Q}{2} = 123mVpk$$



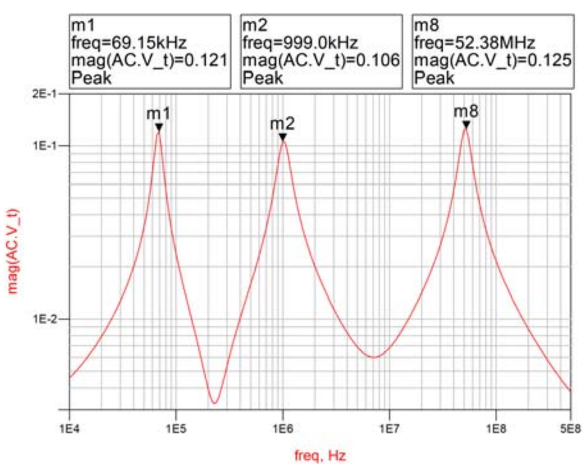
$$\Delta I = 2Amps$$
$$\Delta V = 123mVpk$$

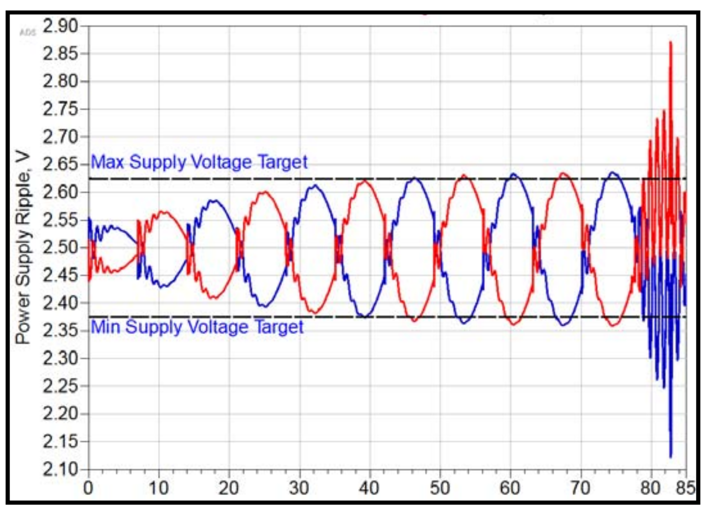
Resonant Square

$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot \frac{2Q}{\pi} = 157mVpk$$



$$\Delta I = 2Amps$$
$$\Delta V = 157mVpk$$





$$\Delta V_{target} \approx \Delta I \cdot \frac{4}{\pi} \sum_{0}^{n} Z_i$$

CHAPTER 1: MANAGING NOISE

Table 1. Example V_{CC} Core Voltage Power Supply Operating Conditions [(1)]

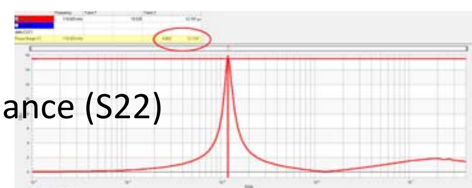
Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply (C1, C2, and 12 speed grades)	—	0.87	0.90	0.93	V
	Core voltage and periphery circuitry power supplier (C2L, C3, C4, I2L, 13, 13L, and 14 speed grades)	—	0.82	0.85	0.88	V

$$Z_{target} = \frac{\Delta V}{\Delta I} = \frac{30mV}{50\% \cdot Imax}$$

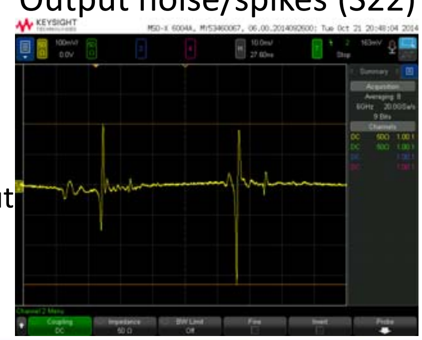
CHAPTER 2: MULTIPLE NOISE PATHS

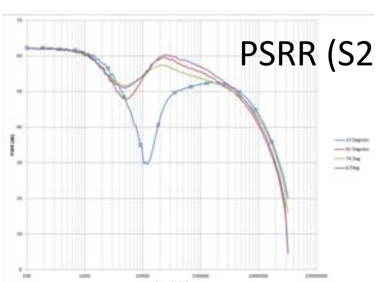
Reverse (S12)

Output Impedance (S22)



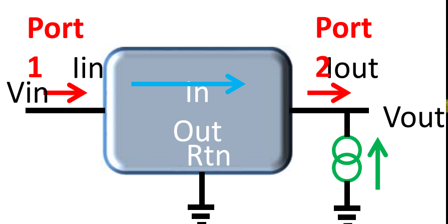
Output noise/spikes (S22)



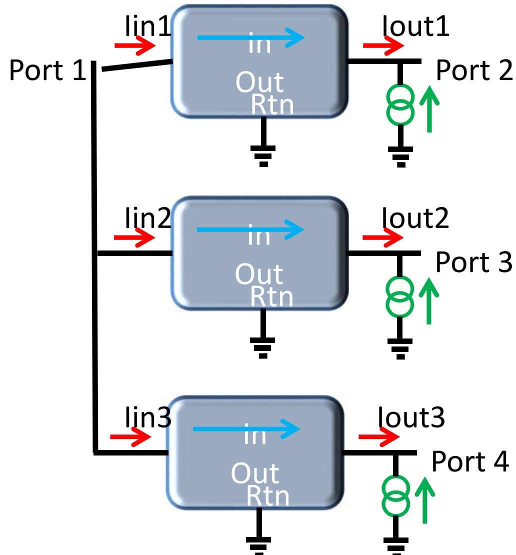


PSRR (S21)

Input impedance (S11)

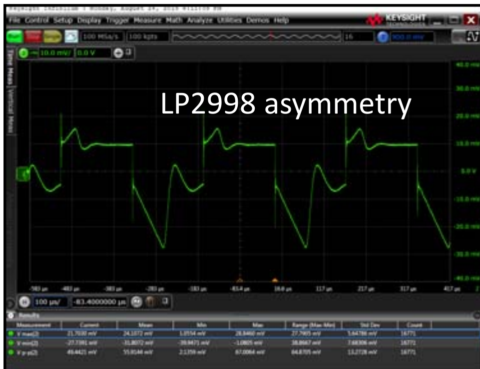


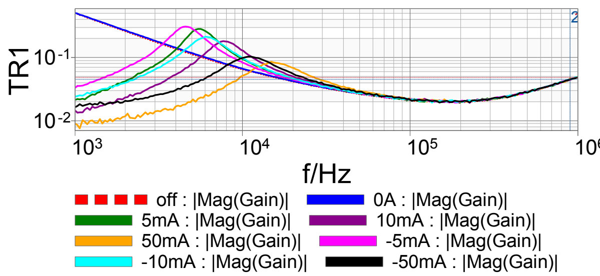
OBVIOUS PATHS THROUGH MULTIPLE VRM'S

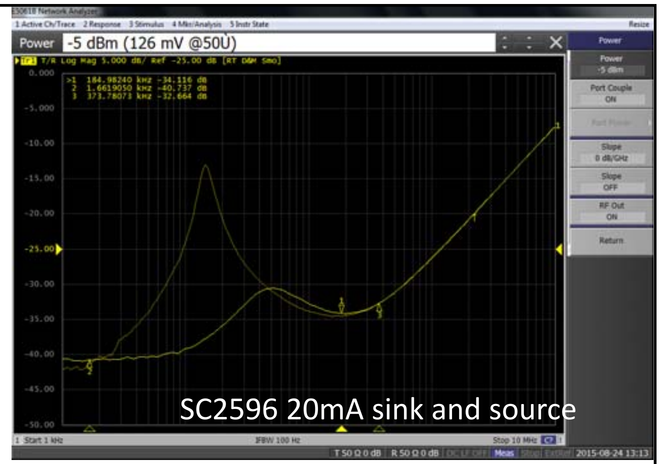


S11	S21	S31	S41
S12	S22	S32	S42
S13	S23	S33	S43
S14	S24	S34	S44

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16







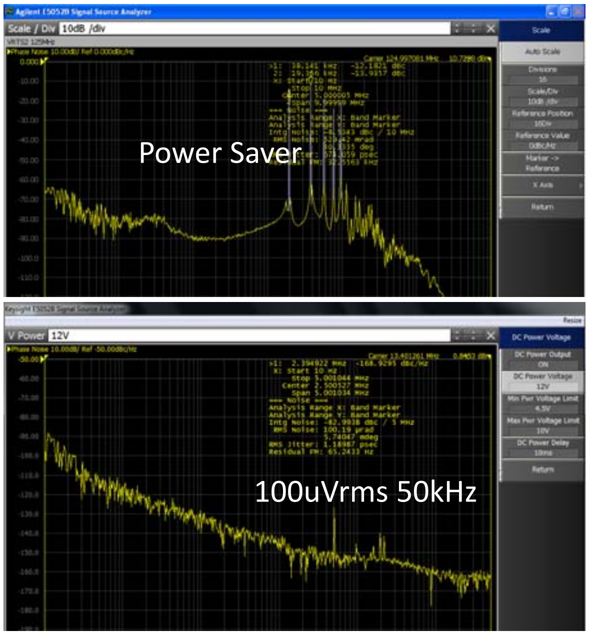
And as these DDR termination regulator measurements
show, performance isn't always symmetrical or small signal

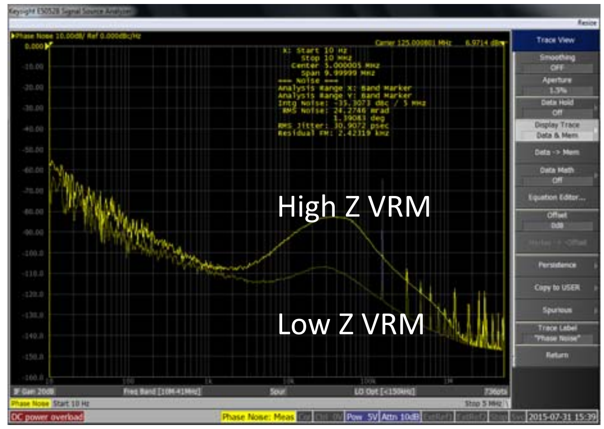
$$\Delta V \approx \Delta I_f \cdot \frac{4}{\pi} \sum_{f=0}^{\infty} Z_f + \sum_{n=0}^{\infty} V_n$$

n is inclusive of **all the noise terms** that we have spoken about (and some we may have mi

- Internal ripple and noise
- Frequency modulation noise
- Duty cycle modulation noise
- Large signal transients
- Intentional and unintentional Glitches (lightning, engine c
- Fault recoveries (soft-start is generally not functional)
- Turn-on overshoot
- Initial, temperature and age (and in some cases radiation)

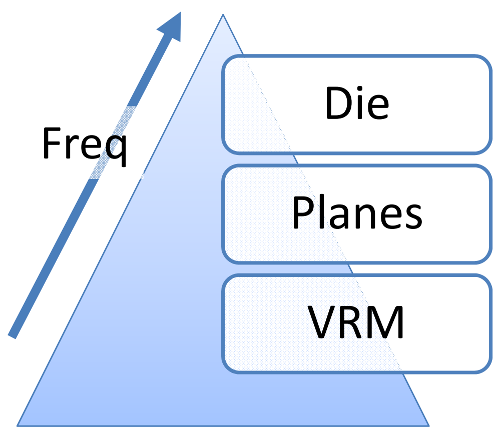
$$\Delta I_f \cdot \frac{4}{\pi} \sum_{f=0}^{\infty} Z_f \approx \Delta V - \sum_{n=0}^{\infty} V_n$$





CHAPTER 3 – BUDGETING FOR ∆V

CHAPTER 4 – LOW FREQUENCIES SCARE ME

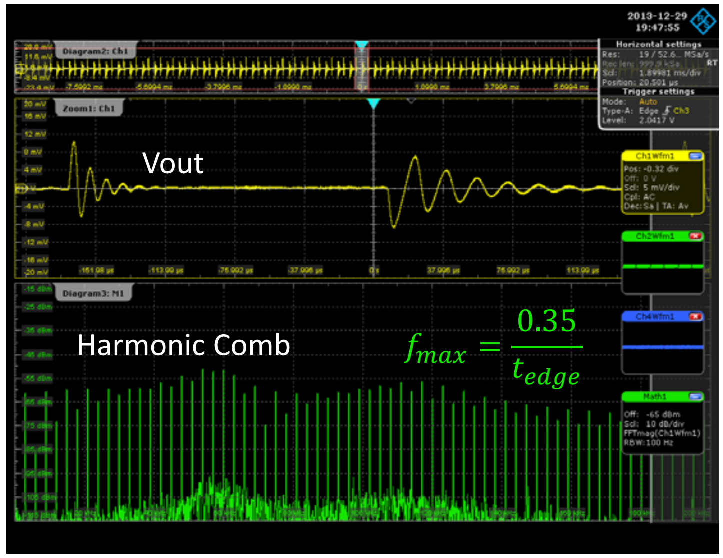


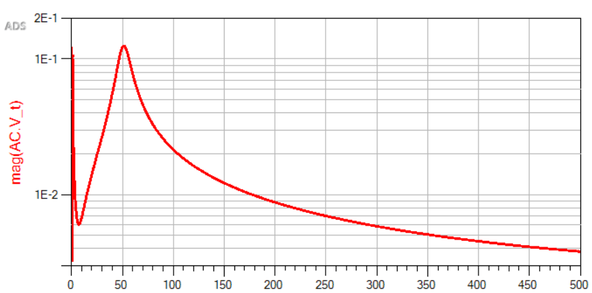
DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

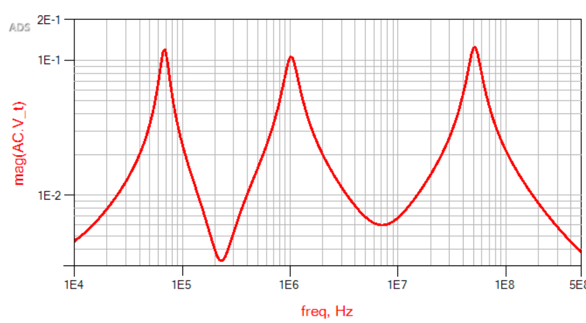
Ringing produces a noise comb with harmonics at all sum and difference frequencies

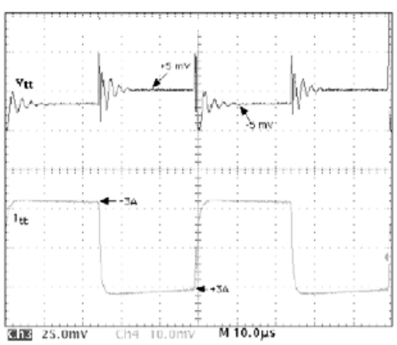
The LOWER the repetition rate the closer the spurs!

Note the large signal effect









Note that

- In this DDR regulator there appear to be multiple frequencies at the edges – hard to see with linear scales. Should be windowed
- Only large signal performance is shown
- Only natural response is shown

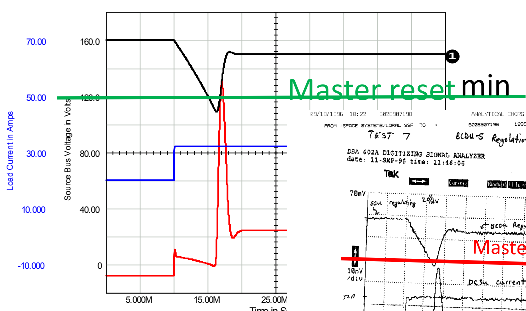
DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

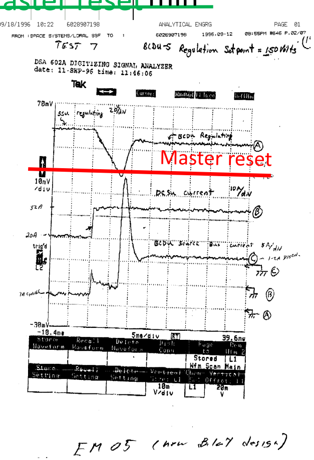
CHAPTER 4 – MISSING THE TARGET

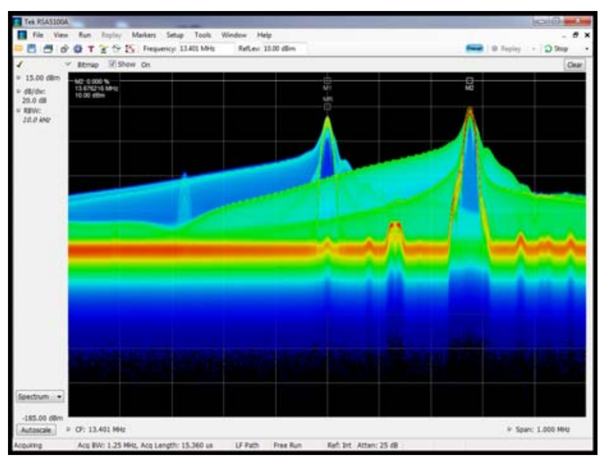
Means someone loses a lot of money!

http://vocabspace.wikispaces.com/file/view/money_in_trash.jpg/108783189/money_in_trash.jpg

CHAPTER 4 – EXAMPLES OF NOISE



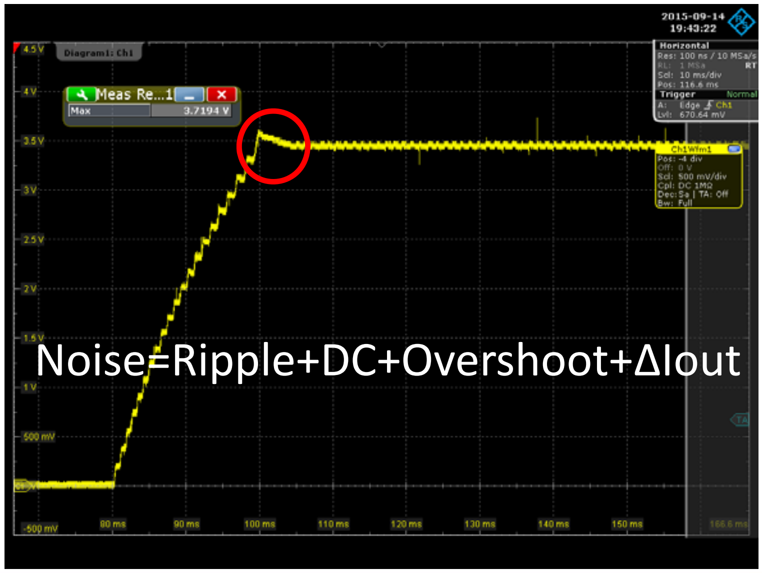




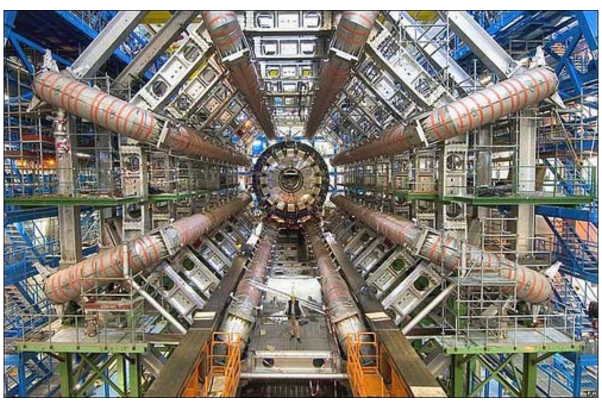
ISS during Eclipse
Main power rail fa
below master rese
The station……eve
minutes!

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

TURN ON OVERSHOOT CONTRIBUTES TO NOISE

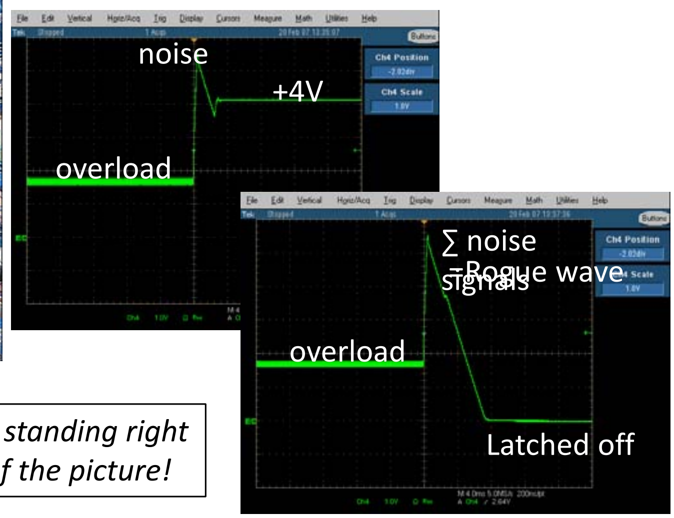


THE PERFECT NOISE STORM



https://c1.staticflickr.com/3/2326/2046228644_05507000b3_z.jpg?zz=1

Trivia –The designer of this coil system was standing right in front of this guy and was CROPPED out of the picture!



DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD
JANUARY 19-21, 2016
#DC16

CHAPTER 5 – SIMPLE ROGUE WAVES

DDR3 Termination regulator evaluation board

PICOTEST VRTS3 Demonstration board - modified

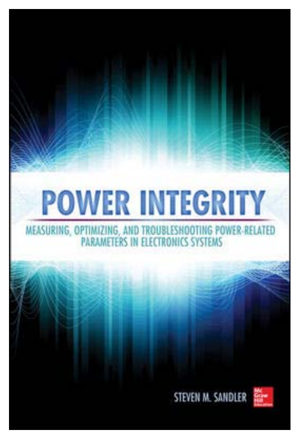
Thanks for Attending!

Keysight CERTIFIED EXPERT EDA SOFTWARE
Steven M. Sandler
Managing Director
www.picotest.com
(480) 375-0075

Steve Sandler has been involved with power system engineering for more than 37 years. Steve is the founder of of PICOTEST.com, a company specializing in accessories for high performance power system and distributed system testing.

He frequently lectures and leads workshops internationally on the topics of power, PDN and distributed systems. He is also the other of Power Integrity – from McGraw-Hill

He was also the recipient of the ACE 2015 Jim Williams Contributor of the Year ACE Award for his outstanding and continuing contributions to the engineering industry and knowledge sharing.



Contact me through our LinkedIn group – Power Integrity for Distributed Systems – or email me at Steve@Picotest.com

UBM

Target Impedance and Rogue Waves

Larry Smith (Qualcomm)

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

UBM

Target Impedance and Rogue Waves

Larry Smith (Qualcomm)

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

SPEAKERS

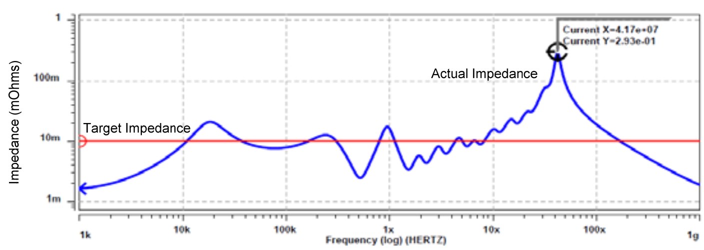
Larry Smith
Principal Power Integrity Engineer, Qualcomm
Larrys@qti.qualcomm.com

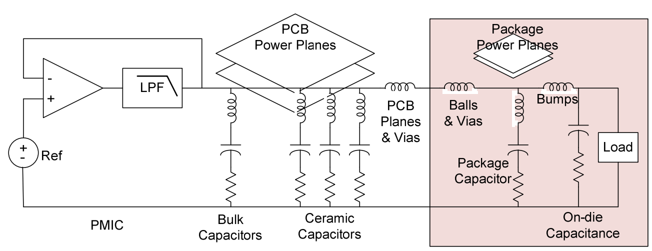
Larry D. Smith is a Principal Power Integrity Engineer at Qualcomm. Prior to joining Qualcomm in 2011, he worked at Altera from 2005 to 2011 and Sun Microsystems from 1996 to 2005 where he did development work in the field of signal and power integrity. Before this, he worked at IBM in the areas of reliability, characterization, failure analysis, power supply and analog circuit design, packaging and signal integrity. Mr. Smith received the BSEE degree from Rose-Hulman Institute of Technology and the MS degree in material science from the University of Vermont. He has more than a dozen patents and has authored numerous journal and conference papers.

Target Impedance is not a law or even a specification

$$Z_{target} = \frac{Vdd \times tolerance}{I_{max} - I_{min}} = \frac{1.2\,V \times 0.05}{7A - 2A} = 10\ mOhm$$

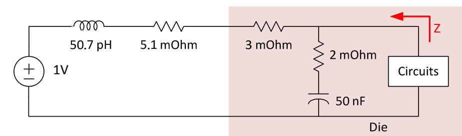
- Z_{target} is a reference line
  - drawn across frequency
  - gives you a basis for evaluating PDNs
- A PDN that significantly exceeds Z_{target}
  - Is in danger of performance problems
- A PDN significantly below the Z_{target}
  - Probably costs more than necessary
- Z_{target} is a function of frequency if
  - Tolerance = f (frequency)
  - Transient = f (frequency)

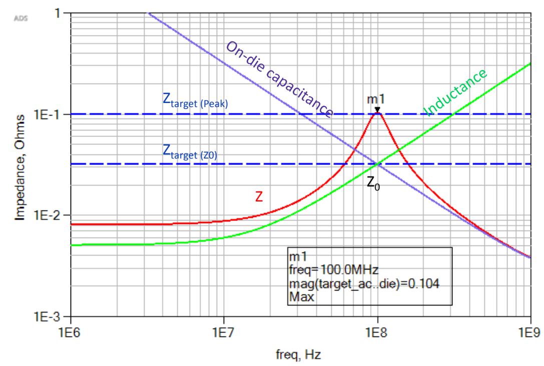




What is expected from a PDN that meets target impedance?

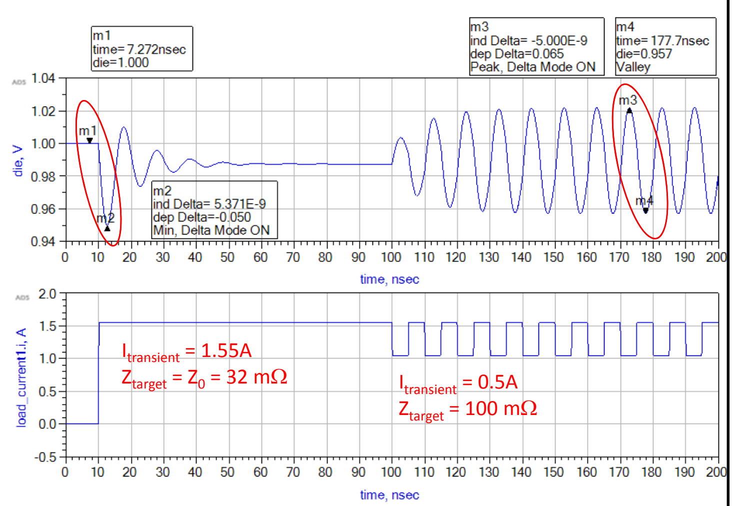
- Frequency Domain System Properties
  - Resonant Frequency $f_0 = 1/2\pi\left(\sqrt{LC}\right) = 100MHz$
  - Characteristic impedance $Z_0 = \sqrt{L/C} = 32m\Omega$
  - Q-factor $q\text{-}factor = Z_0 / R = \sqrt{L/C} / R = 3.15m\Omega$
  - Impedance Peak $Z_{peak} \approx Z_0 \cdot q\text{-}factor = \frac{L/C}{R} = 100m\Omega$
- Time Domain Step Response
  - Desire $Z_0 < Z_{target}$ $Z_{target(Z0)} = \frac{1V \times 5\%}{1.55A} = 32\ m\Omega$
  - Expect 5% droop with 1.55A step current $1V \times 5\% = 50mV$
- Time Domain Resonance Response
  - Desire $Z_{peak} < Z_{target}$ $Z_{target(Peak)} = \frac{1V \times 5\%}{0.5A} = 100\ m\Omega$
  - Expect ± 3.2% p-p with 0.5A resonance current $1V \times 5\% \times \frac{4}{\pi} = 63.7mV\ \ p\text{-}p$





Time domain simulation for Target Impedance

- Step response – 1st 100 ns
  - 1.55 Amps current step
  - Droop is exactly 50 mV (5% of 1V)
  - Z_0 and Z_{target} were identical
    - 32 mΩ
- Resonance response – 100 to 200 ns
  - 0.5 Amps current steps at resonant frequency
  - P-P voltage builds up to 65 mV
  - Maximum droop is 43 mV (4.3% of 1V)
  - Z_{peak} and Z_{target} were identical
- Expectations for Target Impedance
  - Characteristic Impedance Z_0 meets Z_{target}
    - PDN will support step current of $I_{transient}$
      - 1.55 Amps for this PDN
  - Peak Impedance meets Z_{target}
    - PDN will support resonant current of $I_{transient}$
      - 0.5 Amps for this PDN

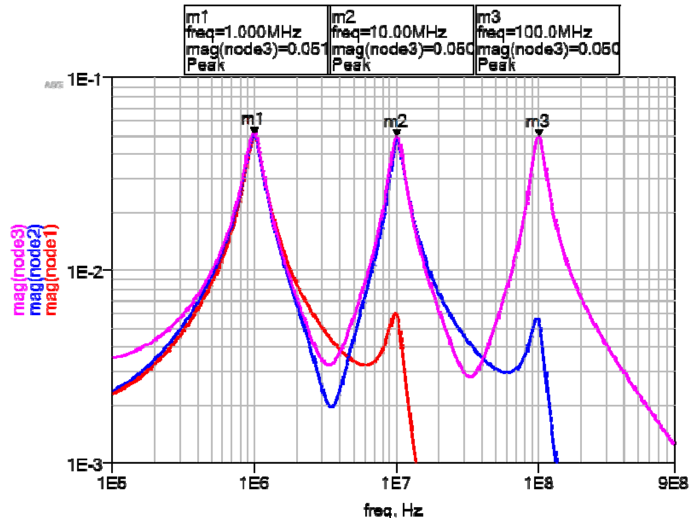


… for a single dominant impedance peak

What if there is more than one resonant peak?

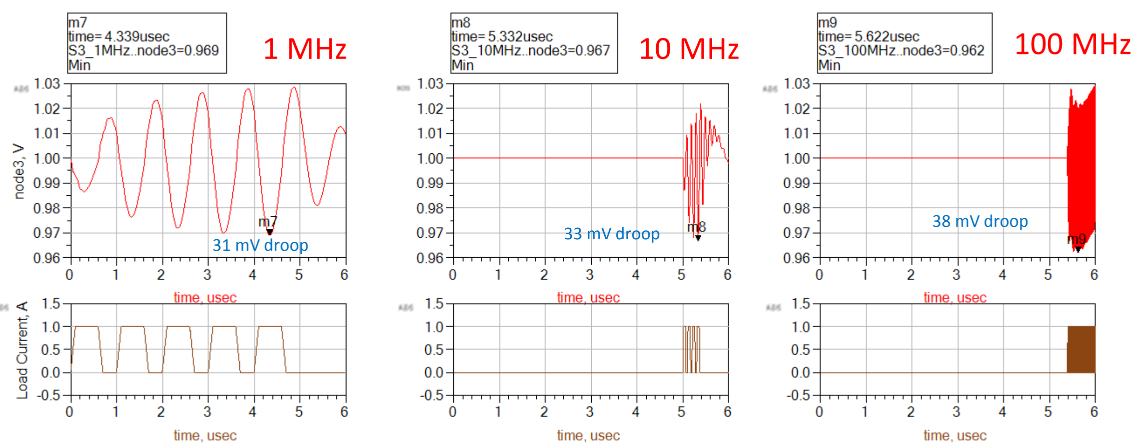
- A good PDN design only has 1 dominant impedance peak
  - This is economically necessary
  - Use good PDN design to flatten out all other peaks
- Rogue waves are possible with 3 peaks
  - superimpose energy from one resonant peak upon another
- 3 peaks at Z_{target} = 50 mΩ
  - 1 MHz
  - 10 MHz
  - 100 MHz
- Q-factor = 4

$$Z_{target} = \frac{Vdd \times tolerance}{I_{max} - I_{min}} = \frac{1.0\,V \times 0.05}{1A} = 50\ mOhm$$



Each resonant peak alone is well behaved

- Stimulate each resonant frequency, one at a time
- Current range is 0 to 1 Amp
- PDN has memory
- Energy from previous events ring out in time

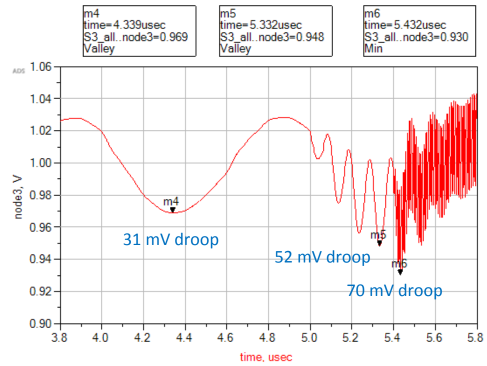


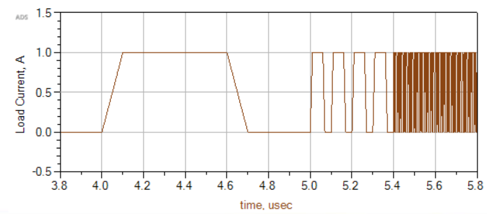
DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD
JANUARY 19-21, 2016
#DC16

Superposition of resonant waveforms

$$Z_{target} = \frac{Vdd \times tolerance}{I_{max} - I_{min}} = \frac{1.0\,V \times 0.05}{1A} = 50\ mOhm$$

- Start energy in next resonant peak before the first resonance dies out
  - 31 mV droop from 1 MHz resonance, 3.1% (m4)
- Stimulation of 2 resonant peaks
  - 52 mV droop, 5.2% (m5)
- Stimulation of 3 resonant peaks 7% droop
  - 70 mV droop, 7% (m6)
  - technically violates 5% voltage tolerance assumed in Z_target calculation
- Extremely low probability event
  - Difficult to fully stimulate 1st resonant frequency
  - Must fully stimulate 2nd resonant frequency at just the right phase
  - Then fully stimulate 3rd resonant frequency at just the right phase





Management of rogue waves

- Strive for flat PDN impedance profiles
  - Multiple high q-factor resonant peaks enable rogue waves
  - Economics almost requires that we have one high impedance peak
    - Between on-die capacitance and package inductance
    - Steve Weir referred to this as Bandini Mountain
  - Don't allow any others
- Even if we have 3 high q-factor resonant peaks, it is very difficult to stimulate them
  - Very low probability event
- A fully stimulated 3 peak PDN with q-factor 4
  - Only produced 7% droop
    - When target impedance was based on 5% tolerance
- Rogue waves are interesting but are not very harmful

Thank you!

QUESTIONS?

DesignCon 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

UBM

Target Impedance and Rogue Waves

What's Your Target?

Brad Brim (Cadence)

DesignCon 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

UBM

Target Impedance and Rogue Waves

What's Your Target?

Brad Brim (Cadence)

Speaker

Brad Brim

Product Engineering Architect, Cadence Design Systems

bradb@cadence.com

Brad has been in the EDA industry for more than 25 years. His graduate studies and initial commercial contributions were in the area of electromagnetic simulation and passive component modeling for circuit simulation. Some of the products he has worked on include: Momentum, ADS, HFSS, PowerSI and OptimizePI. His roles have included software development, applications engineering and product marketing. Prior to joining Cadence as product engineer architect he held various roles with HP/Agilent (now Keysight), Ansoft (now Ansys) and Sigrity (now Cadence).

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

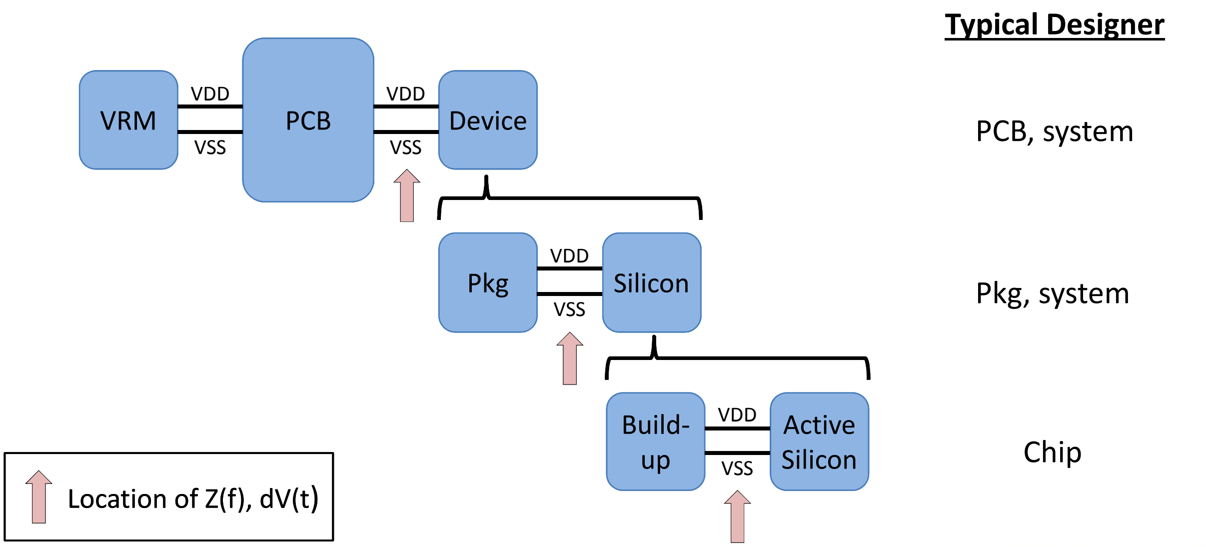
Content

- Target impedance and rogue waves – Overview
- PDN Partitioning and Model Resolution
- Where does additional PDN noise come from?
  - the VRM, the Device
  - multiple devices
  - multiple rails
- What's your target?
  - bottoms-up target impedance enablement

Target Impedance and Rogue Waves - Overview

- Istvan, Steve and Larry thoroughly discussed PDN Rouge Waves
  - desire flat impedance with minimum number of resonances
  - when resonances present, Z_{peak} and number of resonance are dominant effects
  - dI time profile also matters
- Slightly different worst case noise levels were cited
- Need to include external noise in the dV budget.
  - DC, VRM, power-up/down, EMI
- This discussion focuses on two points
  1. additional noise sources
  2. where is your Z_{target} and how to make it more complete and accurate

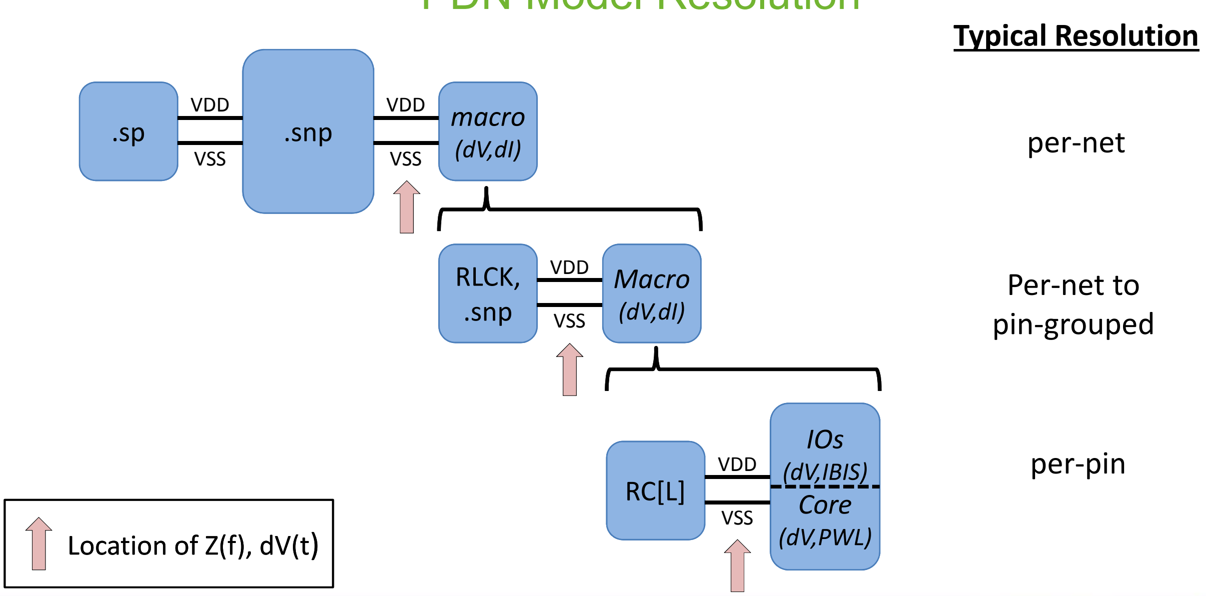
PDN Design Partitioning



JANUARY 19-21, 2016

#DC16

PDN Model Resolution



JANUARY 19-21, 2016

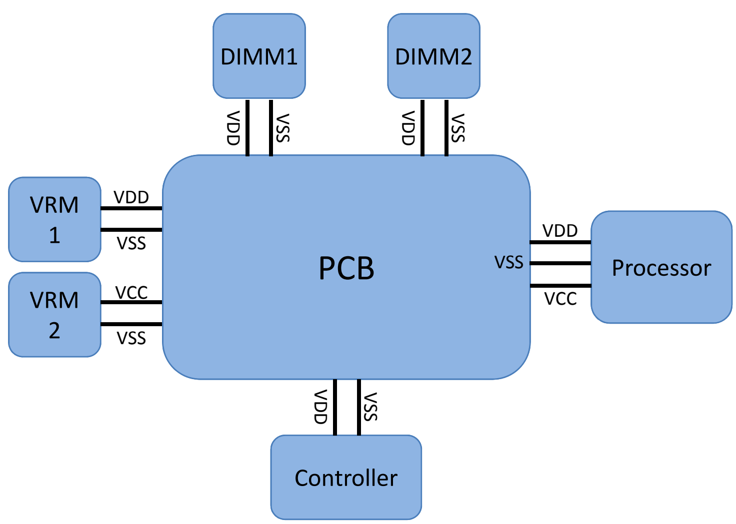
#DC16

VRM and Single Device Noise

- VRM noise
  - single or multiple switching power supplies connected to one rail
  - between rails, unconnected area fills are evil
- Single device
  - locally split planes connected in another domain
  - coupling between core and IO noise
  - coupling among IOs in the same or different banks
  - power-up/down of blocks within the device
  - stated-dependent, spatially-distributed on-die switching activity

PDN Complexities

- Many devices, rails, VRMs!
- Who's the designer and what can they affect?
- What models and reliable requirements are available?
- At what resolution must the PDN be modeled?
- Coupling levels?
- Are there external noise sources to augment dV?



Multiple Devices

- Most designs have multiple devices connected to each PDN rail
- Memory bus: VRMs, processor, controller, DRAMs/DIMMs
- Each device has unique dI(t), both amplitude and time profile
- Entire system should be considered, including mutual impedances Z_{nm}
  - $dV_n(f) = \sum_m \{Z_{nm}(f) * dI_m\}$
  - dV_{ext} is not included here but serves to reduce the dV budget
- An effective self impedance may be defined and applied for target impedance based design
  - $Z_n(f) = dV_n(f)/dI_n$
  - in other fields this is referred to as an "active impedance"

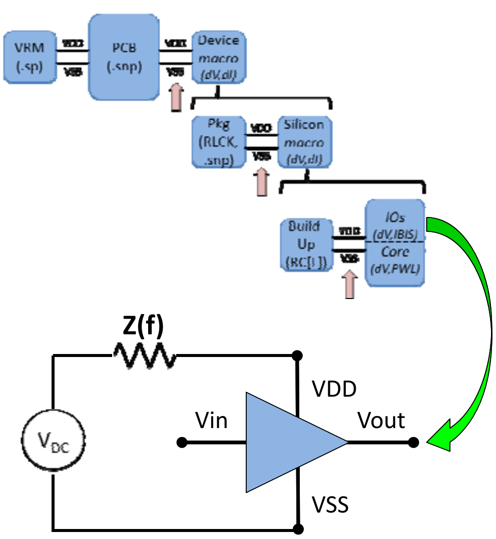
Multiple Rails

- Multiple PDN rails may be coupled
  - true whether or not shared current paths exist
- One PDN rail may serve as the coupling mechanism between two otherwise-uncoupled rails
- Similar *active impedance* concept may be applied to extend target impedance design approach
- The PDN extractions and circuit/system simulations are much more resource intensive with many more diverse dI and dV_{ext} sources
  - analysis tools are available to perform the extractions
  - simulation/optimization tools are available to characterize and tune the system
  - the difficulty continues to be access to reliable requirements and models

What's Your Target?

- Where is Z_{target} for you?
  - Z(f) or V(t) matter at the switching circuit inside the device of interest
  - ball pads available for PCB designers, top of solder bumps for package designers
- What can you affect?
  - PCB designer cannot affect Bandini Mountain but can affect DC, low frequency (bulk caps) and mid frequency (on-board decaps)
  - package design can partially affect Bandini Mountain by reducing loop inductance
- How can you deterministically affect Z(f)?
  - you may not have access to a model with the nodes of interest in the active silicon
  - many PDN designers will not know Z(f) for the L_{pkg}/C_{die} resonance
  - does your device vendor provide per-net/pin Z(f) guidance or do they provide a dV budget or dI(t) profiles per-net/pin?

Bottoms-up Target Impedance Enablement



- IC buffer/block designers should investigate sensitivity of operation w.r.t. Z(f) or dV(t)
  - Z(f) is probably easier and no less accurate
  - $dV_{ext}(t)$ could be added (IR drop, core noise, EMI)
  - accurate enough for reliable design guidelines
- Buffer/block level requirements may be applied with on-die and package models to establish packaged device Z(f)
- A measurement analogy/reversal to "load pull" could be applied for verification
  - could be emulated by simulation when Z(f) is not available from extraction or previous design

Summary

- Z_{target} is an approximate macromodel
  - however, transient simulation and design tuning of the full design is impractical
  - in the absence of specific Z(f) requirements, consider Z_{target} as a guideline
- Consider the complexities of the PDN (multiple rails and devices)
  - active impedance concept generalizes target [self] impedance design flow
- Reliable specification of Ztarget requirements for packaged devices is possible, though almost never available
  - must be enabled from a bottoms-up approach starting with simulation of circuit sensitivity w.r.t. PDN Z(f) or dV

Thank you!

QUESTIONS?

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16