Reflections on DesignCon 2011

Interview by Andy Shaughnessy

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Istvan Novak has been attending DesignCon regularly since the mid-1990s, and every year since 1998. He's watched it grow from the Hewlett-Packard Design Conference into one of the definitive design conferences in signal and power integrity.

We asked Istvan to give us his impressions of DesignCon 2011.

ANDY: What did you think of DesignCon 2011, and the PCB track in particular?

ISTVAN: I was very glad to see DesignCon grow again. Attendance was up, and for me there is a very simple way to check it: During the day, when a lot of visitors are diverted to the overflow parking (as was the case this year), it means good attendance. The conference recently went through a management change, and as always, this created some challenges and headaches. It was good to see, though, that the new conference management is eager to get feedback from the participants and seems ready to listen and make the necessary adjustments.

The papers in the PCB track were interesting, but I think it could benefit from a more direct Call for Papers specifically for the PCB Summit, even if its papers are dispersed among the other DesignCon papers. The summit might benefit from invited TecForums and panel discussions with a wide participation of the key industry players, fabricators, assembly houses and OEMs. It would be great, for instance, to hear from the various sources about discrete and active components embedded in rigid boards, or about the reliability and manufacturability experiences with new low-loss laminates.

ANDY: Tell us about some of the topics you covered in your own sessions.

ISTVAN: First of all, I was particularly proud of our team, because from 2010 three of our papers received Best Paper awards.

This year our team from the Oracle Burlington office had altogether four presentations. One paper explored the laminate losses and described our attempt to separate dielectric loss tangent and conductive losses from measured data with no a priori assumption about their frequency dependency. The paper showed how challenging it is to provide clean enough measurements to support the process. Our second paper gave some very interesting examples showing what unexpected artifacts may show up in our simulation results when we truncate the physical size of a real package so that it fits into a 3D field solver.

Our third paper summarized an almost year-long test series on the DC and AC bias sensitivity of MLCCs, showing a couple of surprises. It was shown that contrary to

popular beliefs, X7R parts are not necessarily better than X5R in this respect. Different relaxation times were also found after the bias was applied, which eradicated an additional 20-30% of the capacitance. Our panel discussion covered a similar topic: I was honored by having well-known industry experts from Ansys, Kemet and IBM share their views about the changing needs of capacitor characterization and modeling.

ANDY: What sorts of SI and PI challenges were attendees concerned with? Was this year's DesignCon truly "The Jitter and Noise Show" as some attendees labeled it?

ISTVAN: Yes, I agree with this characterization. Signal and power integrity are both concerned with noise, though at lower speeds the signal integrity problems can be more readily attributed to deterministic elements. As signaling speed increases and the interaction among more and more circuit elements becomes inevitable, everything blends together to what appears to be a blurred noise on the supply rails and on the signal edges. By now the concepts of jitter and power noise became widely accepted and acknowledged trouble makers for our signals, so it is understandable that we all look for solutions to these challenges.

ANDY: What were some of the more interesting sessions you attended?

ISTVAN: One of the pleasant headaches at DesignCon is to pick which paper to attend among the several parallel tracks, which all may be interesting to you. From the presentations I ended up following this year, I particularly liked Eric Bogatin and Mike Resso had a talk on Monday titled "A Really Simple Method to Characterize Differential Interconnects." Eric and Mike are great speakers and this was an excellent tutorial summarizing how de-embedding and automatic fixture removal can be performed.

I also liked the papers "Improved Multiline-based De-Embedding" by Jon Martens and "Multiport S-parameter Measurements" by Andrea Ferrero, since these will help us in our continued effort to refine our measurements and improve accuracy. There were two interesting papers about PCB losses. The paper "Total Loss: How to Qualify Circuit Boards" highlighted the conflicting interests of the various parties, such as laminate vendors, PCB fabricators and OEM end-users. The paper "Experiment-based Separation of Conductor and Dielectric Losses in PCB Striplines" gave an interesting empirical approach to separate out the effect of surface roughness and dielectric loss from the measured loss curves.

I also thought that the paper "Wavelet Denoising for TDR Dynamic Range Improvement" was an excellent work. And last but not least, Steve Weir's paper "PDN Application of Ferrite Beads" was a superbly written and well delivered paper on a topic that interests many of us.

ANDY: As always, we appreciate your analysis, Istvan.

ISTVAN: Thank you, Andy.