DesignCon 2004

TecForum TF9

Thin and Very Thin Laminates for Power Distribution Applications: What Is New in 2004?

Session organizer and chair:

Frank Alberto	SUN Microsystems, Inc.

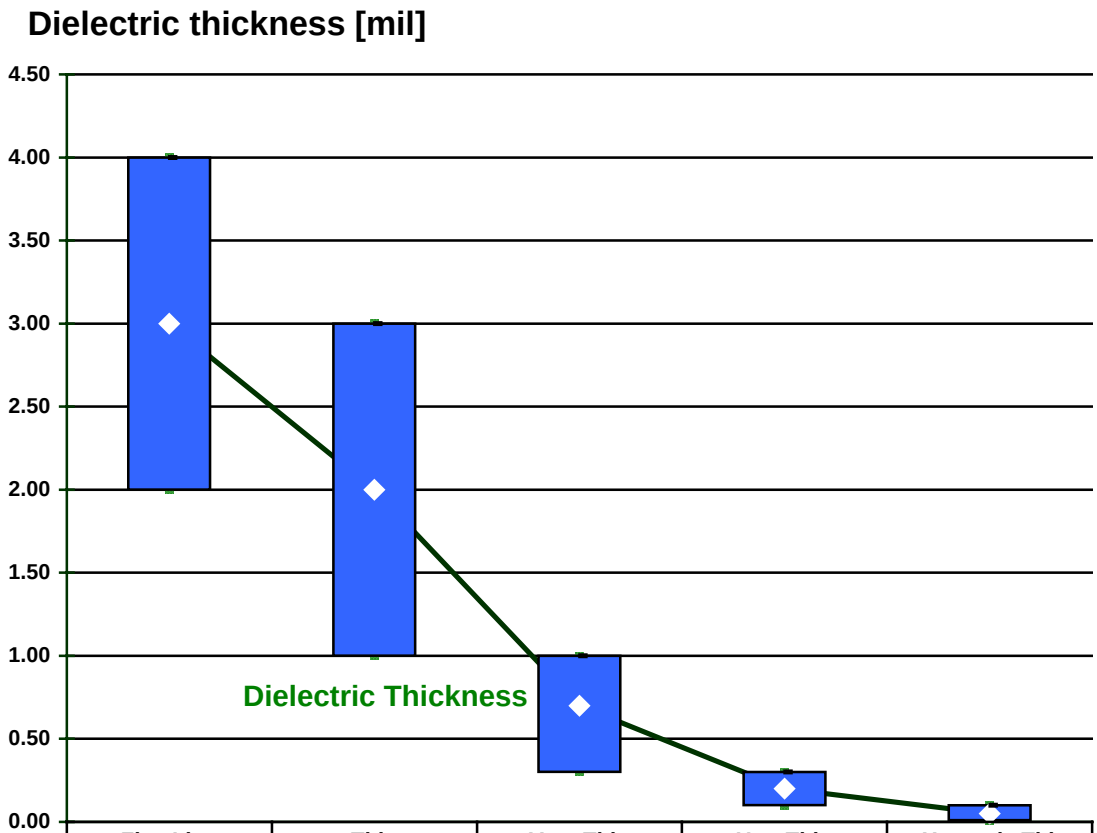
Presenters:

David McGregor	DuPont iTechnologies
Bill Balliette	3M Electronic Solution Division
John Andresakis	Oak-Mitsui Technologies, LLC
Cindy Gretzinger	Sanmina-SCI, Owego
Bob Greenlee	Merix Corporation
Lance P. Riley	Unicircuit, Inc.
Steve Patrick	Benchmark Electronics, Inc.
John Grebenkemper	NonStop Enterprise Division, Hewlett-Packard Company
Istvan Novak	SUN Microsystems, Inc.

Abstract

At DesignCon 2002, a TecForum titled "Thin PCB Laminates for Power Distribution: How Thin Is Thin Enough?" brought together five representative OEMs, three PCB fabricators, and three material suppliers to answer these questions: How thin is thin enough? When will these thin laminates be needed? Will the industry be ready? Since then there has been progress in the available laminates, in their agency approval status, and in the experience collected with them. This TecForum begins with an introduction reviewing the definition and classification of thin laminates, followed by the overall comparison of thin laminate availability in 2002 versus 2004.

Introduction



	Fine Line	Thin	Very Thin	Utra Thin	eXtremely Thin
Min	2.00	1.00	0.30	0.10	0.01
Nom	3.00	2.00	0.70	0.20	0.05
Max	4.00	3.00	1.00	0.30	0.10

Thin laminate nomenclature.

Part I. DuPont™ Interra™ Planar Capacitor Laminates

David R. McGregor, DuPont

Job Title and Current Responsibilities: Senior Development Associate. Team leader responsible for development of thin embedded planar capacitor laminate materials.
Educational Background: 1971 B.S. in Mechanical Engineering from North Carolina State University.
Work Experience: 1974 to present: Quality control, process engineering and product development in Dacron® polyester, Chromium Dioxide magnetic tape, solder mask, primary imaging photoresists and thin core laminates.

I. Introduction

Publications describing the use of thin core laminates as embedded planar capacitors or low impedance power distribution planes in printed wiring boards began emerging in the mid 1980's. The practical embodiment of these publications has been primarily a laminate with a 50 micron or thicker FR-4 dielectric. In the past several years the advantages of using laminates with thinner dielectric have been researched and presented. Using 25 micron cores initially is a good first step. The board processing is not too difficult and there are the electrical advantages of higher capacitance density and lower impedance. These attributes permit improved embedded capacitance, enabling active device function with reduced surface mount capacitors. Laminate with dielectric thickness less than 25 microns will have correspondingly higher capacitance density and reduced impedance performance.

Because of the manufacturing difficulty associated with creating a very thin glass reinforced dielectric, laminates thinner than 25 micron are generally non-reinforced, being either pure polymer or polymer containing a filler to raise the dielectric constant. Adding the filler increases the capacitance density but increases the current conducted at higher voltages, resulting in a lower HiPot voltage. For designs expected to run at relatively low voltage, these materials are quite suitable. For high voltage designs there will be a lower thickness limit, depending on the dielectric material chosen.

Unreinforced, thin dielectrics may also prove to have an advantage with respect to Conductive Anodic Filament growth (CAF). Conductive filaments have been observed growing along the glass fibers in the glass cloth in epoxy or other polymer systems. When plated through-holes are closely spaced, it is possible for copper filaments to grow along the glass fibers to create shorts. Unreinforced dielectrics have been CAF tested at 10 and 150 Volt bias without failure.

Efforts to bring thin core laminates to the marketplace have been accelerating. Several thin core laminates are now commercial and some are close to commercialization. In the case of DuPont, three commercial laminates are available.

II. Laminates

Three laminates are currently available as commercial products and will be discussed here. These three laminates offer both reduced inductance, reduced EMI, and increased capacitance density. Others are under development.

The first laminate is Interra™ HK 04. It is an all polyimide, unfilled dielectric that is 25 microns thick. It is based on the same all polyimide platform that has been sold to the flex industry in high reliability applications, e.g., satellites, under hood automotive, disk drives etc., for a number of years and millions of square feet have been made. Because it is unfilled, it has excellent voltage resistance and, unlike older flex laminate materials, its water absorption is much lower. The key properties are discussed below.

The second laminate is Interra™ HK 10. It is a barium titanate filled polyimide dielectric that is 25 microns thick. It has similar impedance performance to the HK 04 but has a higher dielectric constant. Even though it has a filler, it is capable of being imaged double-sided. The HK 10 key properties are discussed below.

The third laminate is Interra™ HK 11. It is also a barium titanate filled polyimide dielectric but its thickness is 14 microns. Because it is filled and thinner than HK 10, a sequential lamination process is used during board manufacture. Its key properties are also discussed below.

III. Key Properties

Interra™ HK 04

Physical Characteristics:

Dielectric Material:	Polyimide
Thickness:	25 microns
Copper Thickness:	9 - 108 microns
Copper Type:	ED or RA
Maximum Sheet Size:	24” x 51”
Standard Sheet Size:	18 - 18.5” x 24 - 24.5”

Physical Properties:

Peel Strength:	10 pli
CTE:	25 ppm/°C
Water Absorption:	0.8% (100% RH for 48 hours)
UL	
Flammability:	UL94 V-0
RTI, mech/elec:	200° C / 240° C
Dissimilar Materials w/FR-4:	Complete. This test not required for fabricator.
Debond/Delam:	This test required to be done by each fabricator.

Electrical Properties:

Dielectric Constant:	3.5
Capacitance Density:	0.8 nF/in^2 (measured at 1 MHz)
Dissipation Factor:	0.003 (measured at 1 MHz)
Breakdown Voltage:	6000 Volts/mil
HiPot Voltage:	>1500 Volts DC

Performance Characteristics:

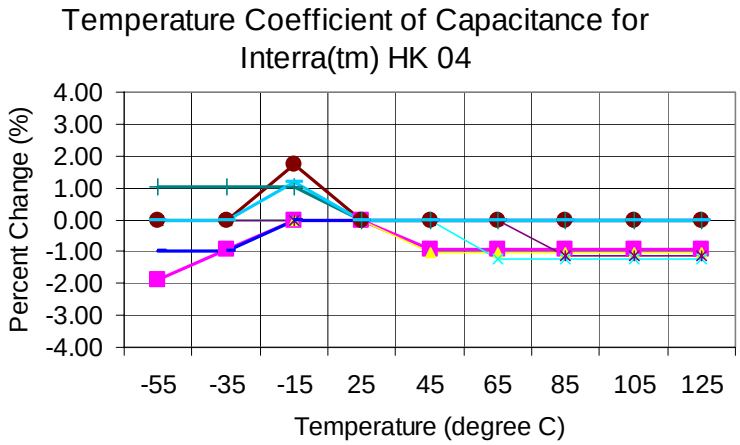


Figure 1. Temperature Coefficient of Capacitance for Interra™ HK 04 on nine samples.

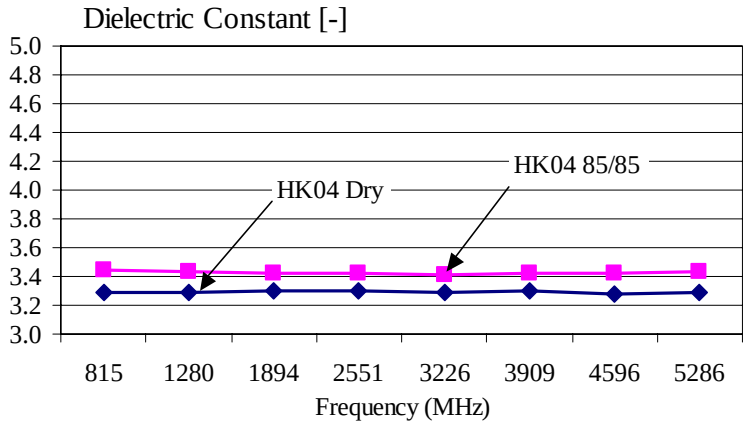


Figure 2. Moisture effect on Dielectric Constant. Top trace: dry; lower trace: 85/85.

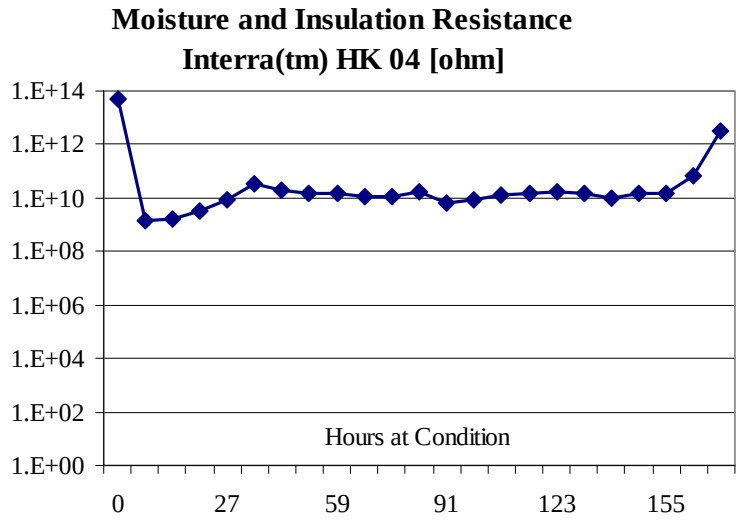


Figure 3. Moisture and Insulation Resistance for Interra™ HK 04

Reliability Test Results:

85/85 100VDC Bias, 1000 hrs.:	No change in resistance during test.
HAST 100VDC Bias, 96 hrs.:	No change in resistance during test.
Humidity Effect on Capacitance:	<10% increase from 0 - 90%RH
85/85 Capacitance Change:	No change during 1000 hours
Solder float peel strength:	No change after 288°C / 10 seconds
High Temperature Aging:	No change in peel strength after 150ºC/1000 hrs.
Thermal Cycling:	No change in peel strength -55 - 150ºC/1000 hrs.

Interra™ HK 10

Physical Characteristics:

Dielectric Material:	Polyimide with barium titanate filler
Thickness:	25 microns
Copper Thickness:	36 - 72 microns
Copper Type:	ED
Maximum Sheet Size:	19.5” x 51”
Standard Sheet Size:	18 - 18.5” x 24 - 24.5”

Physical Properties:

Peel Strength:	8 pli
CTE:	46 ppm/°C
Water Absorption:	0.7% (100% RH for 48 hours)
UL	
Flammability:	UL94 V-0
RTI:	130° C
Dissimilar Materials w/FR-4:	Pending.

Electrical Properties:

Dielectric Constant:	10
Capacitance Density:	2.2 nF/in^2 (measured at 1 MHz)
Dissipation Factor:	0.01 (measured at 1 MHz)
Breakdown Voltage:	3100 Volts/mil
HiPot Voltage:	250 Volts DC

Performance Characteristics:

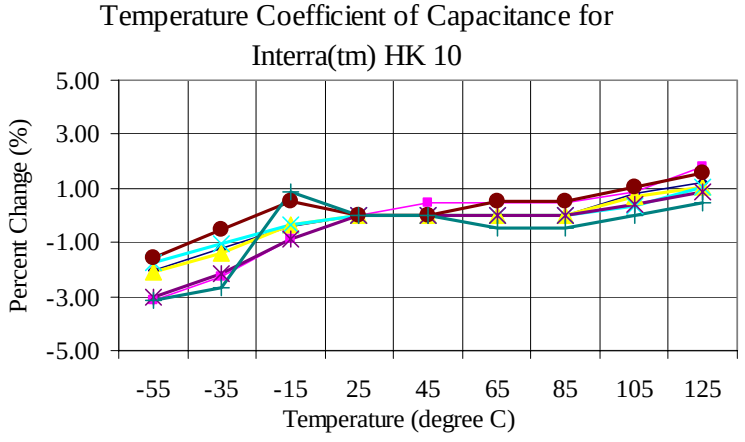


Figure 4. Temperature Coefficient of Capacitance for Interra™ HK 10

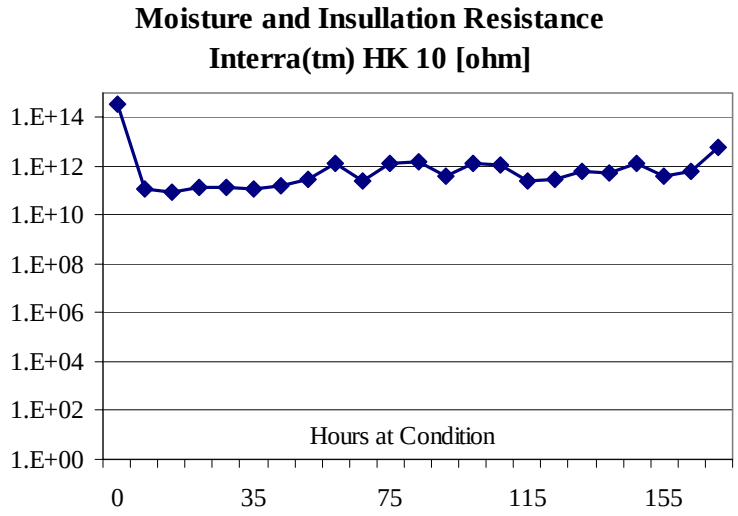


Figure 5. Moisture and Insulation Resistance of Interra™ HK 10

Reliability Test Results:

85/85 Capacitance Change:	3% change after 1000 hours
Solder float peel strength:	5% decrease after 288°C / 10 seconds

Interra™ HK 11

Physical Characteristics:

Dielectric Material:	Polyimide with barium titanate filler
Thickness:	14 microns
Copper Thickness:	36 - 72 microns
Copper Type:	RA
Maximum Sheet Size:	19.5” x 51”
Standard Sheet Size:	18 - 18.5” x 24 - 24.5”

Physical Properties:

Peel Strength:	13 pli
Water Absorption:	0.5% (100% RH for 48 hours)
UL	
Flammability:	Completion expected 1/04
RTI:	Completion expected 1/04
Dissimilar Materials w/FR-4:	Pending.

Electrical Properties:

Dielectric Constant:	11
Capacitance Density:	4.5 nF/in^2 (measured at 1 MHz)
Dissipation Factor:	0.02 (measured at 1 MHz)
Breakdown Voltage:	2500 Volts/mil
HiPot Voltage:	100 Volts DC

IV. Experience

Interra™ HK 04

Interra™ HK 04 is based on the same platform as our all polyimide flex laminate where millions of square feet have been manufactured. Thirteen fabricators have built a variety of rigid boards designs using HK 04 and have been able to process it successfully.

Because it is a thin laminate, some learning is usually required for material handling. Otherwise HK 04 can be processed through all normal printed wiring board operations. Drilling and permanganate desmear performance is very good as shown in the example below.

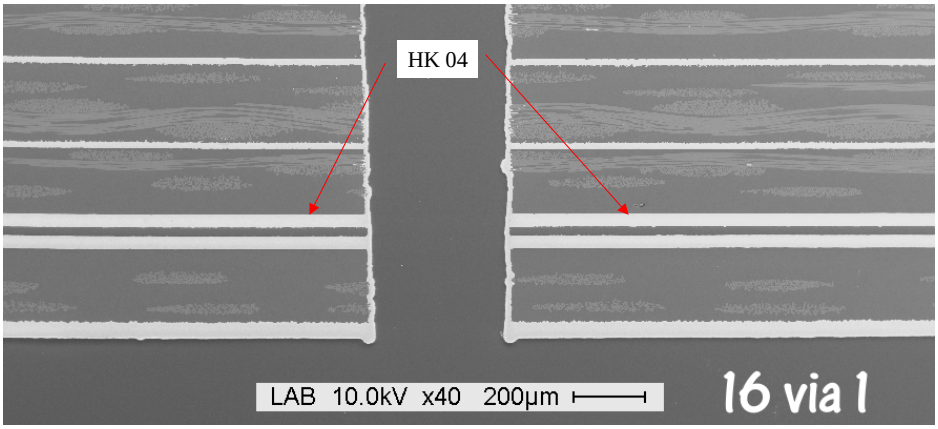


Figure 6. Cross Section View of Interra™ HK 04

Because surface mount capacitors used for decoupling active devices are placed in parallel to reduce inductance, most of them can be eliminated when using a thin core laminate for power and ground. One example is shown in Figure 7 below.

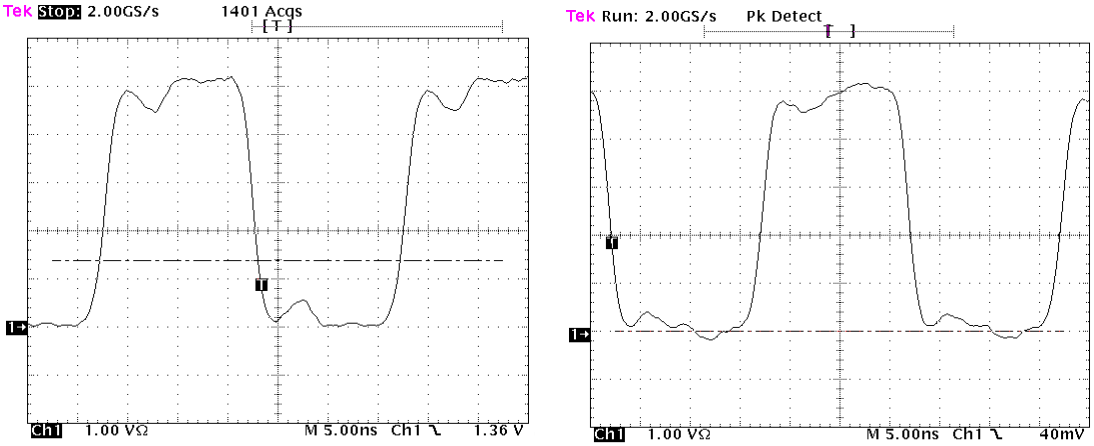


Figure 7. Comparison of Signal Between Normal Board (left) and Board Containing Interra™ HK04 with 400 SMT Capacitors Removed (right).

This was a comparison of a conventional high-speed video board and the same board made with HK 04. In this comparison the conventional board was populated with all the surface mount capacitors. On the board made with HK 04, 400 surface mount capacitors were not populated, leaving all the stubs and empty surface mount pads. The left trace in Figure 7 shows a measured signal from the conventional board. The right trace shows the same signal measured for the HK 04 board. The signal is slightly better with the HK 04 even though the stubs were present. The active devices worked as designed and radiated EMI was reduced.

Figure 8 shows the impedance as a function of frequency for several thicknesses of polyimide dielectric. As observed in other studies the impedance is reduced with thinner dielectric.

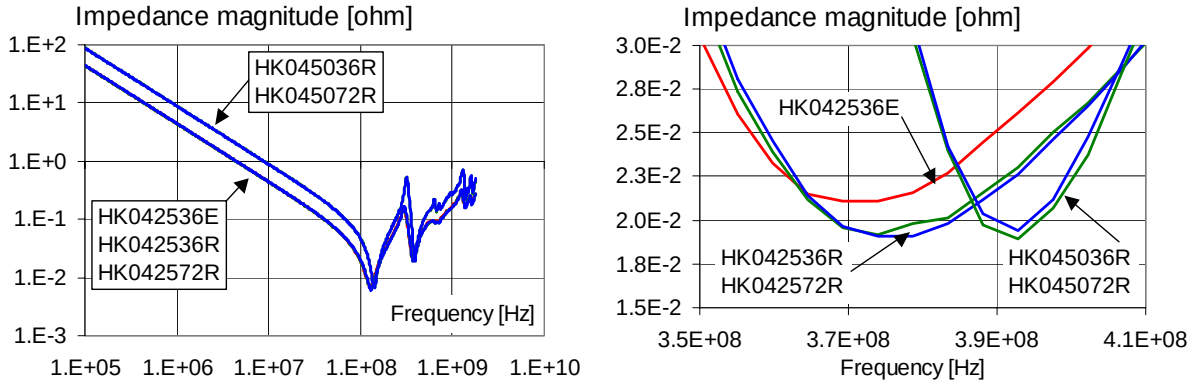


Figure 8. Self-impedance plot of bare test boards with five different HK04xxx laminates. Full scale shown on the left, zoomed graph on the right. Data from SUN Microsystems.

Even though HK 04 is only 25 microns thick, it is processable double-sided. Copper can be removed from both sides simultaneously during etching. Boards have been fabricated using existing automated handling equipment with excellent results. Multilayer lamination is done at the lamination press cycle used for the FR-4 laminate of choice. In fact, experience has shown that the bond between the HK 04 dielectric and a variety of glass/epoxy prepregs is excellent.

Interra™ HK 10

Tens of thousands of square feet of Interra™ HK 10 have been manufactured and 10 fabricators have experience processing it. Even though this is a filled dielectric it can be processed double-sided with care paid to material handling.

Interra ™ HK 10 requires only minor deviation from normal PWB processing used in most shops. Plasma etching is required for drilled hole desmear (no permanganate) and an alternate multilayer bonder chemistry is required (no black oxide). Drilling, plating, and all other processes are normal.

Interra™ HK 11

Tens of thousands of square feet of Interra™ HK 11 have been manufactured and multiple fabricators have experience processing it. Unlike HK 04 and HK 10, this laminate must be processed using a sequential lamination approach. In this process the first side of the laminate is imaged, leaving un-

etched copper on the second side. This is then laminated to another single-sided layer or another copper foil using prepreg to create a subpart. The subpart becomes an innerlayer with copper on both sides. Because this subpart innerlayer is now rigid enough, it is processed double-sided. During this step, the second side of the HK 11 is imaged.

Drilling, desmear and plating are all done conventionally, meaning that either plasma etching or permanganate may be used for through-hole desmear. Figure 9 shows 2 layers of HK 11 in a board. The picture on the left shows the quality of the dielectric after drilling, desmear and plating. Boards have been fabricated and tested through 6X, 288° C solder shock with zero failures.

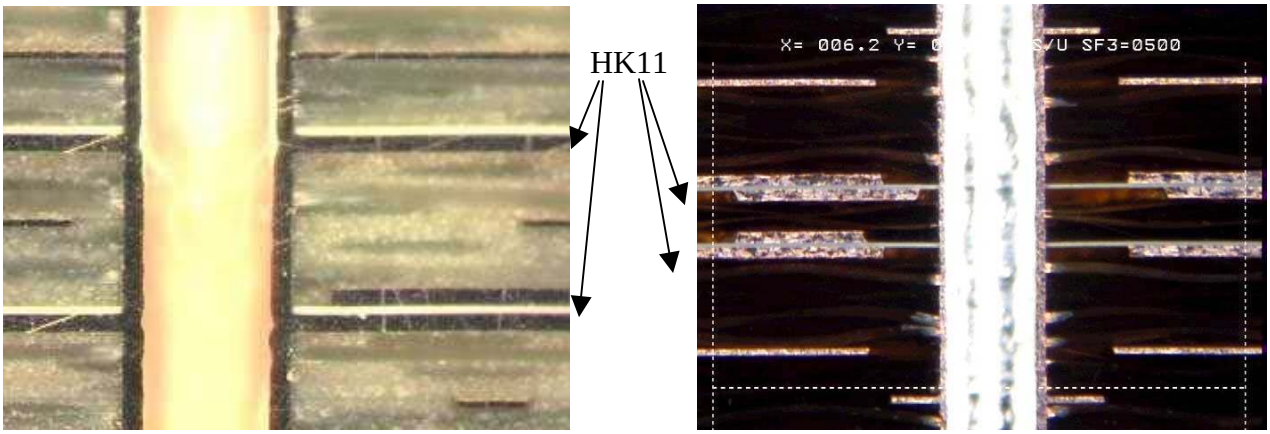


Figure 9. Cross Sections Showing Two Layers of Interra™ HK 11

V. Summary

Three commercial laminates are available for use for low impedance and embedded planar capacitance in printed wiring boards. These laminates are based on polyimide chemistry, the same polyimide that has been used for many years in the flex industry. It is very robust and its attributes have made it desirable for very demanding military applications. These same attributes are present in the thin core laminates discussed here. The HK 04 laminate has passed full UL qualification at three fabricators and since the Dissimilar Materials test has been completed for use with FR-4 the amount of UL qualification needed by the fabricator has been reduced.

Two of the laminates can be processed double-sided. Since they are both 25 microns thick, they have similar impedance curves with respect to frequency. For those desiring higher dielectric constant, HK 10 is available.

One of the laminates is 14 microns thick, has reduced impedance with respect to frequency and also has a high dielectric constant.

All three laminates have been manufactured multiple times, have been processed at well known printed wiring board fabricators and been tested by OEMs.

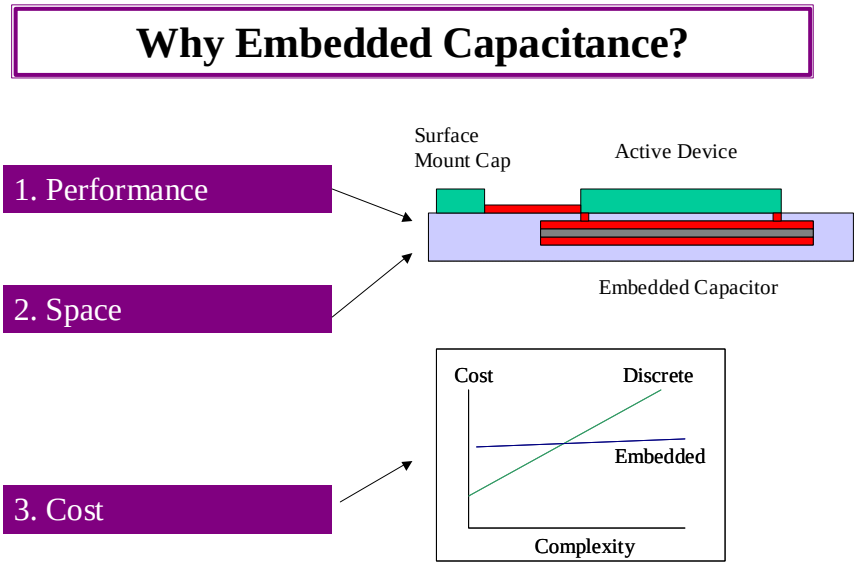
VI. Acknowledgements

The author wishes to express his gratitude to Thomas D. Lantzer and G. Sidney Cox for their collaboration in preparation of this paper.

Part II. Ultra-Thin, Loaded Epoxy Materials for Use as Embedded Capacitor Layers

Bill Balliette, 3M Electronic Solution Division

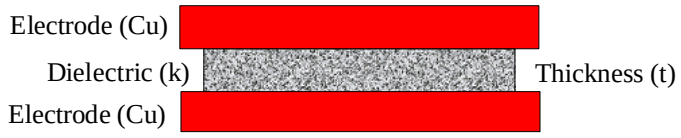
Bill Balliette is a business development manager in the Electronic Solutions Division of 3M. He is responsible for commercialization of advanced materials including embedded capacitor materials and liquid crystal polymer flex circuits. He holds a BS in mechanical engineering from Dartmouth College, and an MBA and MS in manufacturing systems engineering from the University of Texas at Austin. Contact him at wmballiette@mmm.com or by phone at 512.984.7324.



Reasons for Embedded Capacitance

Potential Benefits	Performance	Space	Cost
Faster signaling/Reduce power bus noise	√		
Reduce design time & redesigns	√		√
Eliminate capacitors		√	√
Reduce layer count			√
Enable DS to SS assembly			√
Reduce via count		√	√
Simplify rework			√
Reduce board size, thickness		√	
Reduce assembly time			√
Enable decoupling w/back-side heat sinks	√		
Reduce weight	√		
Reduce opportunities for damaged components	√		√
Improve PWB panel utilization			√
Reduce EMI	√		√

Thin-Film Capacitor Technology



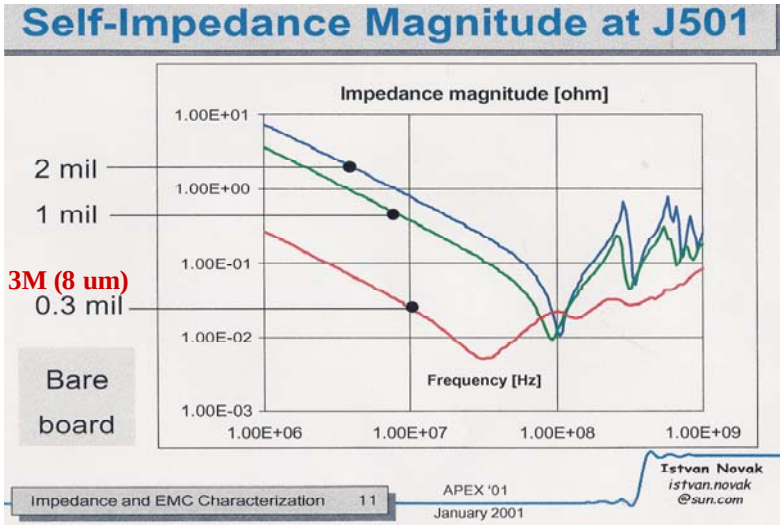
- **Capacitance per unit area (C/A) is proportional to k and inversely proportional to t**
- **Vary C/A by varying thickness (t) or dielectric constant (k)**

3M™ Embedded Capacitor Material Properties ("3M C-Ply")

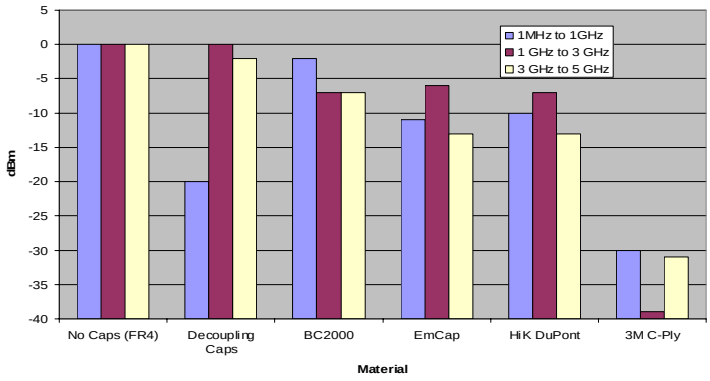
Attribute	Value
Capacitance /area - 16 um - 8 um*	5 nF/in2 10 nF/in2
Dielectric Constant	16
Freq., Voltage, Temperature	Meets X7R
Dielectric Strength	~130V/um
Breakdown Voltage - 16 um - 8 um*	>100V, 500V* >50V
Copper Thickness	35 um
Flammability Rating	94V-0

*** In development**

Impedance Comparison



Power Bus Noise on Test Vehicle



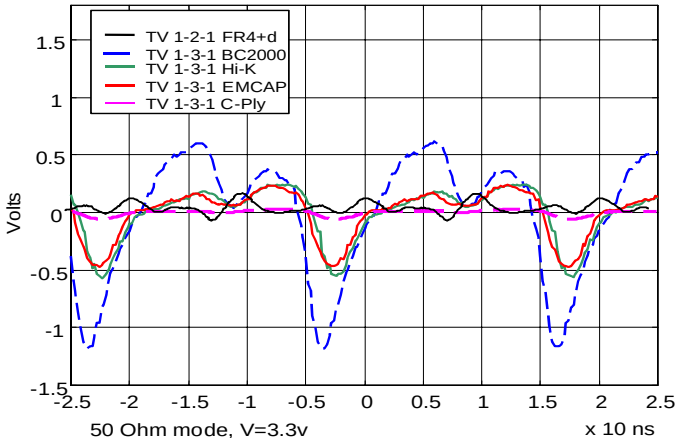
Less Noise

- **Traditional decoupling capacitors are not effective at frequencies above 1 GHz**
- **C-Ply layer has excellent performance to 5 GHz**

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

Power Bus Noise

(Time Domain - 50 MHz)

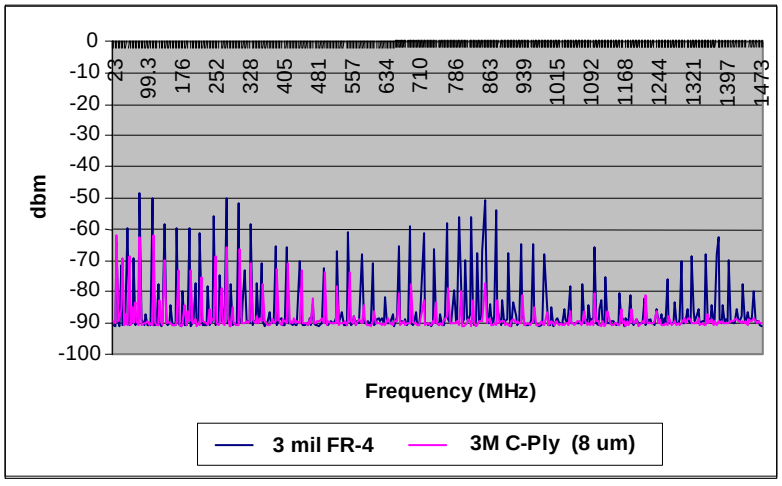


Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

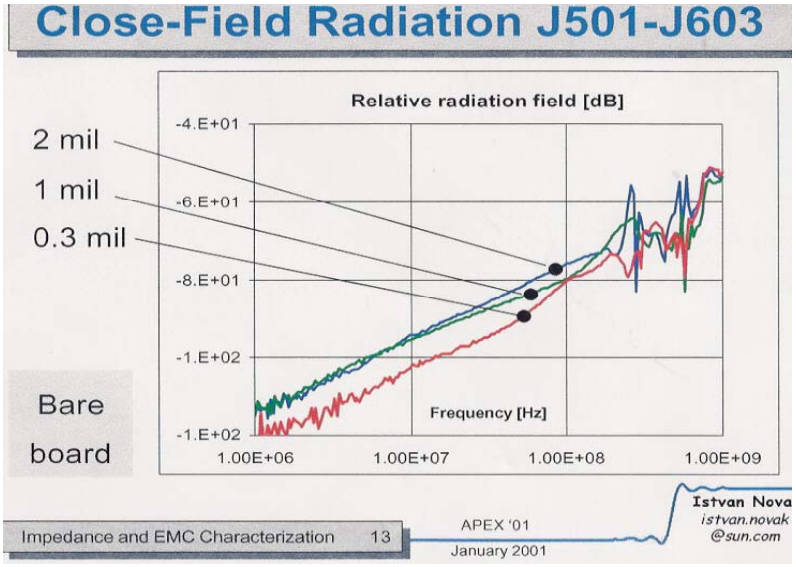
Power Bus Noise

Power-Ground Core Material	Nominal Capacitance (nF)	Peak-to-Peak Voltage (mV)
FR-4 (with 33 discrete SMT caps)	330	214
BC2000™ (50 um)	3	1,740
HiK (40 um)	10	816
EmCap™ (100 um)	13	712
3M Embedded Capacitance Material (5 um)	107	89

Power Bus Noise vs. Frequency (H.P.)



Radiated Emissions Comparison



Environmental Testing

Test	*Property*	*Result*
High Temp (125°C)	Capacitance	No Change (1000 hrs)
Thermal Cycle Thermal Shock	Capacitance	No Change (1000 cycles)
High Humidity (85°C/85% RH)	Capacitance Dissipation Factor	10-15% Increase* 0.4% to 0.9%*
TMA (T260)	Life	>5 minutes
***THB* (85C/85%RH/15 V)**	Life	>1000 hrs
ESD (2-25 kV)	Capacitance/D.F.	No change
Pressure Cooker (121C/2 atm)	Capacitance/D.F.	No change after bake
Bend Test	Capacitance	No change (200 cycles)
Multiple Reflow (3X)	Capacitance	No change

***Returned to pre-test level after bake**

UL Testing

Test	*Property*	*Result*
Laminate	Flammability	94V-0
Laminate	Solderability Limits	288C/30 sec
Laminate	Relative Thermal Index	130C
Board (Merix)	Flammability	94V-0
Board (Merix)	Max Operating Temp	130C

PCB Processing - 1

- **Compatible with all rigid and flex PCB processing (including laser ablation)**
- **Material handling is most significant issue (compares to bare 2 ounce copper)**
- **A sequential lamination process is recommended**
  - **Pattern 1st side copper**
  - **Laminate patterned side to another layer of prepreg**
  - **Pattern 2nd side copper**

PCB Fabrication - 2

- **If a sequential build up process is utilized, there are no design limitations**
- **Many high end fabricators with thin core processing equipment have successfully fabricated numerous prototype lots**

Examples of Embedded Capacitance Replacing Discretes

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Capacitance Removed
EDC TV1	**330** *33 x 0.01 uF*	**105**	**3.1**	**100%**
OEM A	**12,600** *126 x 0.1 uF*	**300**	**42.0**	**NA**
OEM B	**6,310** *62 x 0.1 uF* *11 x 0.01 uF*	**210**	**30.0**	**>60%**
OEM C	**3,180** *29 x 0.1 uF* *28 x 0.01 uF*	**~300**	**~10.6**	**>75%**
OEM D	**52,900** *529 x 0.1 uF*	**1969**	**26.9**	**>75%**

Summary

- **Surface mounted discrete capacitors are ineffective above 1 GHz**
- **Low impedance and high capacitance are ideal for power supply decoupling at high frequencies**
- **Impedance is more critical than capacitance at high frequencies**
- **Thin dielectric materials dampen noise at high frequencies**
- **Lower power bus noise can result in reduced radiated emissions**
- **Ultra-thin, loaded laminates used for power-ground cores have the potential to remove most or all of the high frequency decoupling capacitors**
- **Initial data indicates that surface mounted capacitance can be effectively replaced by embedded capacitance with only a small fraction of the total discrete capacitance**

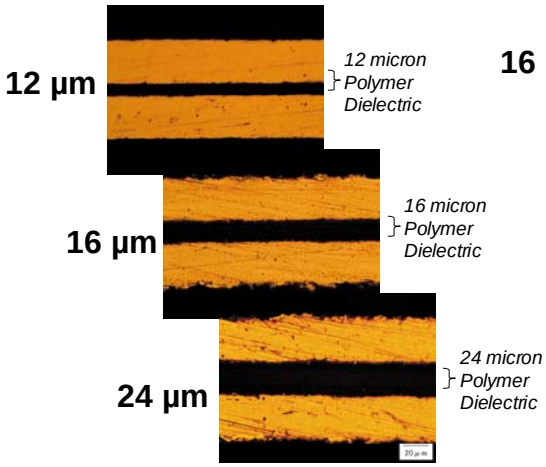
Part III. Performance of Polymeric Ultra-thin Substrates For use as Embedded Capacitors: Comparison of Unfilled and Filled Systems with Ferroelectric Particles

John Andresakis, Takuya Yamamoto, Pranabes Pramanik,
Oak-Mitsui Technologies, LLC
Nick Buinno, Sanmina-SCI Corporation

John Andresakis- Vice President of Strategic Technology for Oak-Mitsui Technologies (a wholly owned subsidiary of Mitsui Kinzoku), has over 22 years experience in the manufacturing of Printed Circuit Boards. Before Oak-Mitsui, he was Engineering Manager for Hadco Corporation (now part of Sanmina-SCI Corporation) at both their Owego, NY and Hudson, NH facilities. In addition to Hadco, John was in Technical Management at Nelco, Digital Equipment and IBM. He holds a Masters Degree in Chemical Engineering from the University of Connecticut and a Bachelors of Engineering Degree from Cooper Union. He is a member of the IPC Suppliers Technology Council. He has received 4 patents related to PCB Production.

Product Design

Construction



(16 µm with Filler is under development)

-Standard Copper thickness is 35 µm

Product Data

Electrical Properties

Characteristics	Condition	Unit	24µm	16µm	12µm	8µm	16µm-Filler
Capacitance	1GHz	nF/cm^2	0.14	0.23	0.31	0.45	1.75
Dk	1GHz	N/A	4.4	4.4	4.4	4.4	30.0
Df	1GHz	N/A	0.015	0.015	0.015	0.016	0.019
Dielectric Thickness	Nominal	Micro-Meter	24	16	12	8	16

Product Data

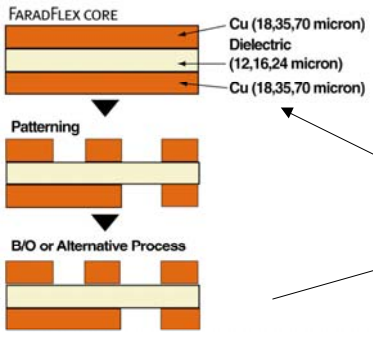
Physical Properties

Characteristics	Condition	Unit	24µm	16µm	8&12µm	16µm-Filler
Tg	DMA	Celsius	200	200	200	200
Peel Strength	As received	lb/in	>6.0	>6.0	>6.0	>4.0
Young's Modules	JIS 2318	GPa	4.8	5.8	7.2	TBD
Tensile Strength	JIS 2318	MPa	180	180	180	TBD
CTE	IPC TM650	PPM	30	30	30	TBD
Breakdown	1kV/sec	V	>5000	>4000	>4000	TBD
Insulation Reliability	85C/85%/35V	hr	>1000	>1000	>1000	TBD

PWB Manufacturing Process

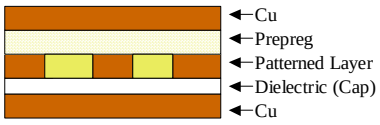
Thin Substrate without Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative



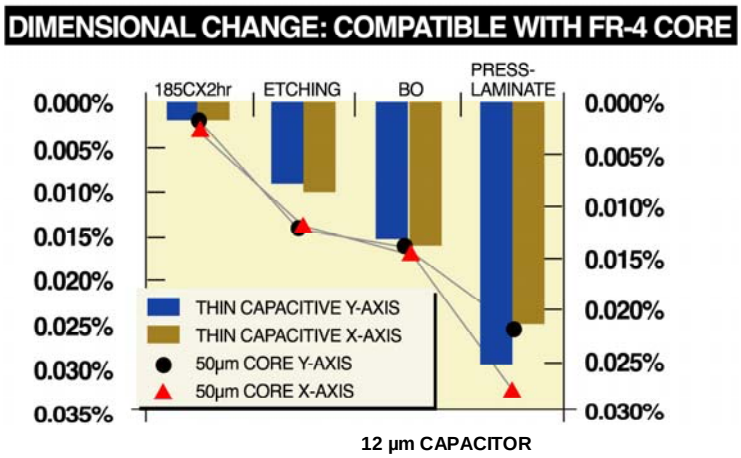
Thin Substrate with Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative



Subassembly

PWB Manufacturing Process



PWB Manufacturing Process

Summary of Unfilled Substrates (approx. 1000 panels)

- Substrates Processed at 10 Major PCB Facilities
- Standard I/L Processing
- Results
    1. **No loss** due to jams
    2. **No "blow out"** of Clearance holes
    3. **No separation** from border pattern
    4. **100 % Yield (due to material issues)** at Hi-Pot (500 Volts)
    5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
- PWBs available from ZBC™ Licensed Fabricators

Summary of Filled Substrates(<100 panels)

- Substrates Processed at 2 Major PCB Facilities
- Standard I/L Processing with additional steps
- Results
    1. **No loss** due to jams
    2. **No "blow out"** of Clearance holes
    3. **No separation** from border pattern(Cu to edges)
    4. **100 % Yield** at Hi-Pot (100 Volts) (limited quantity)
    5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
    6. **Registration between *buried* and outer core layers on subassembly critical**
- PWBs available from ZBC™ Licensed Fabricators

Availability

- 12,16 and 24 micron unfilled materials are commercially available
- 1 oz. Copper is standard and can be delivered quickly (other copper weights will take longer initially until inventory established)
- 8 micron unfilled and 16 micron filled materials available for testing (commercially available by 2Q04)

Cost/ft^2

- Quotes available upon request
- Competitive with other sub 1 mil materials
- Price reductions in future based on production optimization and reduced raw material prices.

Reliability Tests

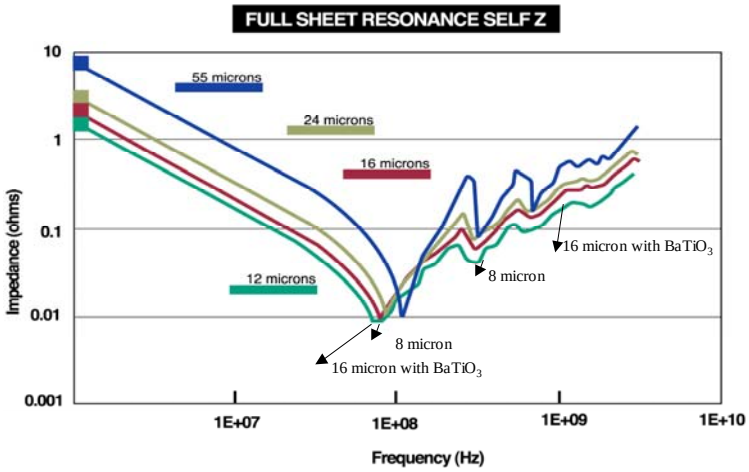
- Dielectric Withstanding Voltage : 500V Passed, No failure
- T-260 Time to Delamination : 1*2 µm*- 6.3min, *24 µm*- 5.2min
- Blind Via Plating Defects : No defects found
- Thermal Solder Shock (288^{o}C)– 10x : No defects found
- Liquid-Liquid : *24 µm* 4.2%(500 cycle)
- IST Testing: Passed 500 Cycles

Approvals

- Unfilled 12, 16 and 24 micron materials are UL approved (94VO, 130 Operating Temp.)
- PCB Shops submitting their UL samples (2 already submitted)
- Telcordia samples being prepared
- 8 micron unfilled and 16 micron filled materials are in for UL approval

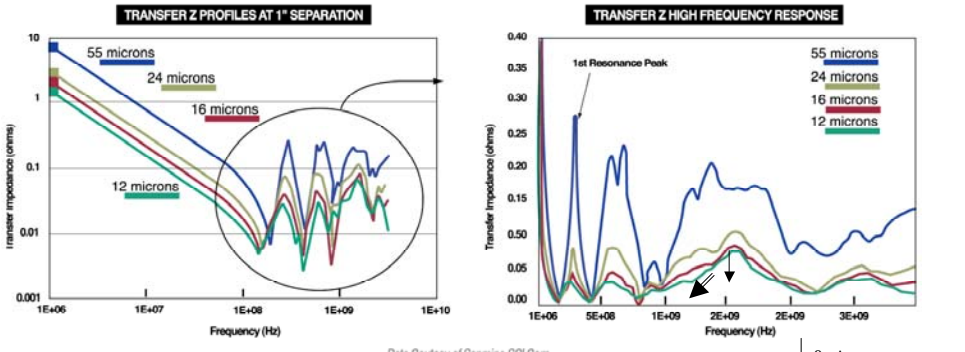
PWB Electrical Performance (Self Z)

Significant Reduction on Impedance



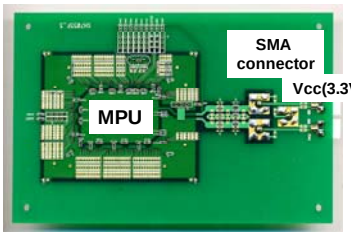
PWB Electrical Performance (Transfer Z)

Significant Reduction on Impedance

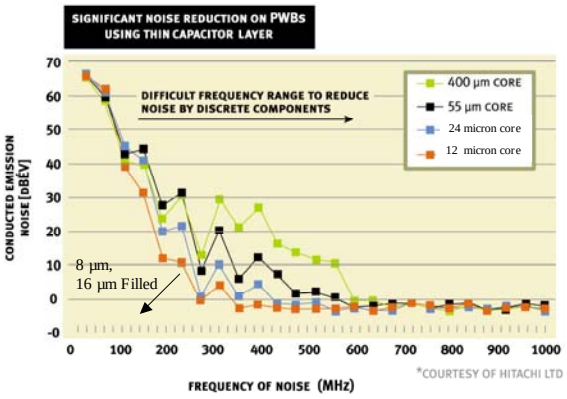


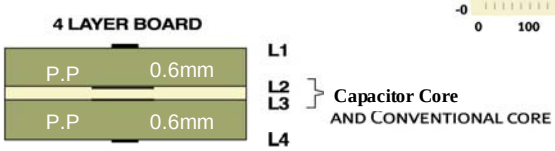
PWB Electrical Performance (Transfer Z)

Significant Reduction of EMI



MPU (40MHz) is mounted on the other side of the board.





Comparison Summary

Unfilled Substrates Versus Filled Substrates

Property	Unfilled Thin Substrates	Filled Substrates
Impedance Reduction/lower noise		+
Electric Strength/ High Potential Testing	+	
Ease of PCB Processing	+	
Cost of Substrate/Raw Board	+	
Cost of Assembled Board	?	?

Conclusion

- Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency
- New Substrates have demonstrated *excellent* electrical performance and physical properties.
- They are *compatible* with PWB processing; a truly “drop in” material.
- Materials are commercially available from Licensed Fabricators
- The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
- The Technology can Improve System Price/Performance by
  - Reducing Discrete Caps
  - Reducing PWB size
  - Increasing Functionality
- Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PWBs
- Additional work is ongoing to
  - Improve PWB manufacturing process of filled substrates

Part IV. SANMINA-SCI, Thin Core Buried Capacitance Processing and Reliability

Cindy Gretzinger, Chad Kormanek, Sanmina-SCI Corporation

Cindy Gretzinger is currently the Inner Layer Engineering Manager at Sanmina-SCI Corporation in Owego, NY. Over a 19 year career, she has been responsible for imaging processes, chemical etching processes, materials, oxide, plating , AOI and Electrical Test. Prior to Sanmina-SCI , Ms. Gretzinger was a Staff Engineer with IBM Federal Systems Division. She holds a Bachelor of Science Degree in Chemical Engineering from Michigan Technological University.
cindy.gretzinger@sanmina-sci.com (607) 689-5507

Outline

I. Processing
- A. Thin Core Processing Capabilities
- B. Material UL Status

II. Reliability
- A. Thermal Analysis (T288/T300/T350)
  - 1. Core Material
  - 2. Hybrid Package without Copper
  - 3. Hybrid Package with Copper
- B. IST Data
  - 1. Test Design
  - 2. Temperature and Humidity Stressed Testing
- C. Assembly Rework Simulation
  - 1. Solder Float Testing
  - 2. Multiple Pass Through Reflow (standard and lead free temperature)

Part V. Processing Thin and Very Thin Laminates: What Is New in 2004?

Bob Greenlee, Merix Corporation

Job Title and Current Responsibilities: Advanced Development Engineer, responsible for process development of the embedded resistor and capacitor materials used in the NIST AEPT Consortium.
Educational Background: 1995 M.S. in Chemical Engineering from Washington State University
Work Experience: 1995 – 2003: Process Engineer, Quality Engineer, and Advanced Development Engineer at Merix Corporation.

Introduction

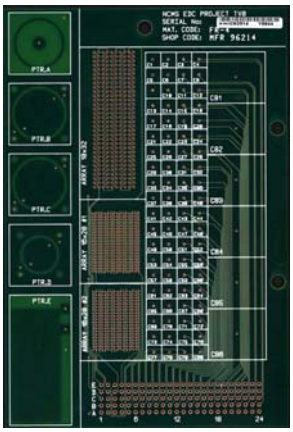
At DesignCon 2002, we reported our processing experiences with very thin (< 25 μm) laminates, based primarily on our experience in the NIST Advanced Embedded Passives Technology (AEPT) consortium. At that time, most of our processing was with 3M's C-Ply, an 8 μm non-reinforced ceramic-loaded high dielectric constant epoxy-based laminate, and some of DuPont's thin polyimide ceramic-loaded experimental materials. Since that time, we have gained experience with other thin and very thin laminates, including:

- a 16 μm version of C-Ply
- DuPont's HK-4, a 25 μm non-reinforced, non-loaded polyimide based laminate
- DuPont's HK-10, a 25 μm ceramic-loaded high dielectric constant polyimide based laminate
- Oak-Mitsui's FaradFlex, a 12 – 25 μm non-reinforced, non-loaded epoxy based laminate.

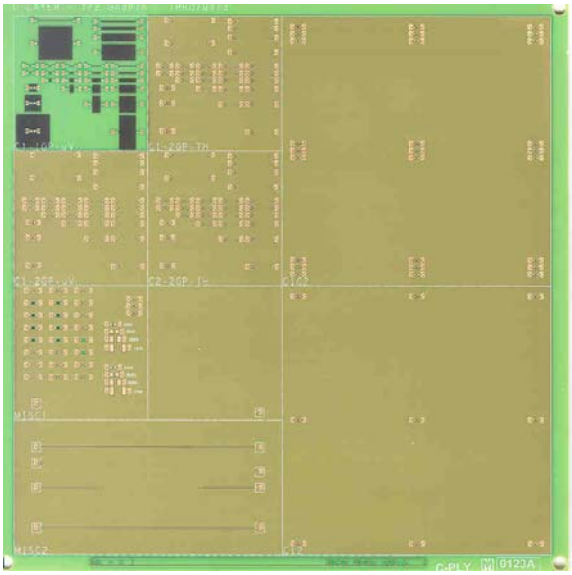
This paper will summarize the lessons we have learned since our initial work with these materials, as well as their current qualification status.

Thin Laminate Board Builds

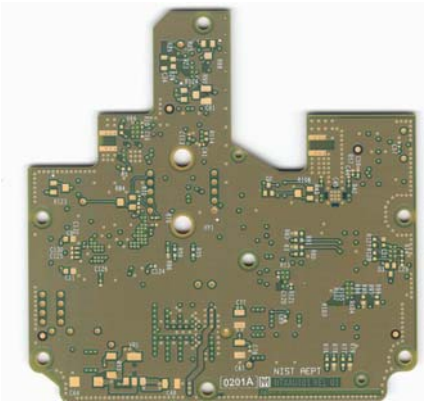
Within the NIST consortium we built several NIST AEPT test vehicles (the TV1-C and the TV2-C) using the thin and very thin materials. We also had the opportunity to build two emulators with the C-Ply material. In addition to the Nortel high-speed emulator mentioned in the DesignCon 2002 presentation, we built the Hewlett-Packard iPaq emulator boards, using two sheets of 8 μm C-Ply. We also built, and numerous impedance test boards for Sun using various thicknesses of C-Ply and DuPont's HK-4.



NIST AEPT TV1-C

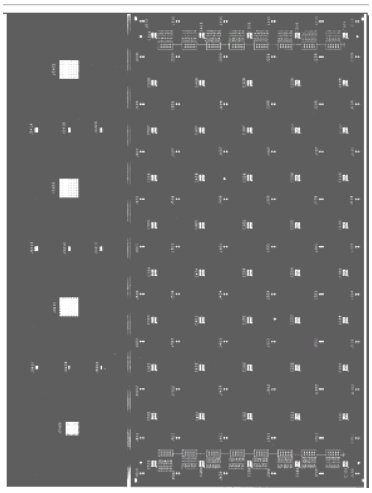


NIST AEPT TV2-C



Nortel Transceiver Module

HP iPaq Emulator



Sun Impedance Test Board

As interest in these new technologies grows, we have built prototypes with both ceramic-loaded and non-loaded materials for customers, some in combination with embedded resistors.

Processing Challenges

One of the major differences we found between the ceramic-loaded and non-loaded materials is that it is necessary to process the ceramic-loaded laminates as a subpart, etching one side before laminating to another piece of material and etching the second side. The non-loaded materials are generally able to withstand the pressures of the etcher sprays, and both sides can be etched simultaneously.

The second major difference is that the ceramic-loaded materials have a lower dielectric withstanding voltage, and so must be high-pot tested at a lower voltage.

Lastly, and perhaps not surprisingly, even though the non-loaded laminates can be etched on both sides at the same time, they can be somewhat more difficult to convey through an etcher than the ceramic-loaded laminates. This is for the simple reason that when etching the ceramic-loaded laminates, the copper is completely left on one side of the panel, which provides extra support as it is conveyed from section to section and through the pinch rollers. Therefore, depending on the panel layout and whether or not there are natural "fold" lines in the etched panel, it may be necessary to use leader boards when processing thin non-loaded materials through the DES line.

In general, though, all of the thin and very thin laminates have one thing in common: the dielectric is thinner than the copper! Since most of their rigidity comes from the copper foil, conveyor systems have to be will-maintained. Misplaced rollers or guide fingers replaced incorrectly may not affect processing of thicker laminates so much, but will spell disaster for these thin, flexible laminates. We found that by using "dummy" material made of 2-oz. copper foil, we could check the processing through the conveyorized equipment without risking the loss of the more expensive laminates.
One piece of equipment, the dry film photoresist autolaminator, is particularly sensitive to these very thin laminates. Again, good maintenance is critical to ensure that the tension of the top and bottom rolls of photoresist is balanced, and that the myriad of other parameters are correctly adjusted. On the positive side, we found that once the equipment was set up correctly, standard product would also run trouble-free. These thin laminates, while stretching the capability of some of our equipment, also widen the process window for other product.

We also found that the ease with which thin laminates process through certain modules may depend in part on the type of copper used. For example, shiny, rolled-annealed copper seems to have more surface tension as it goes through pinch rollers between tanks of rinse water and acid preclean, and may be more likely to wrap around the rollers. Therefore, we prefer reverse treat copper foil be used on thin laminates, since it seems to process with less difficulty.

Other minor modifications were required for post-etch punch and AOI. Specifically, the contrast between the copper and the dielectric had to be "dialed in" so that the optical systems could readily distinguish targets.

Perhaps the most important tool for improving the processing of these thin materials was training technicians to handle them as they would film, i.e., holding it by opposite corners to prevent handling damage.

UL Qualification and IPC Standards

At Merix, we have qualified both 3M's C-Ply materials and DuPont's HK-4 materials with UL. We have started the process of getting UL qualification for Oak-Mitsui's FaradFlex materials.

As far as IPC standards for thin materials is concerned, we have completed most of the work on the board performance specification, but are waiting for an opportunity to include it in a forthcoming revision of IPC 6012. A significant amount of progress has also been made on IPC design and material standards for both thin core embedded capacitance materials and embedded resistor materials.

A good deal of reliability testing has been done on all of these materials, both within the NIST AEPT consortium and outside of it, and there is yet more testing that will be done.

Conclusions

OEMs are showing greater interest in thin and very thin laminates as they consider the gains they can make in performance, size reduction, and EMI noise reduction by incorporating these materials. Although these materials are somewhat challenging to process, good equipment that is well maintained, and technicians that are sensitive to the flexible nature of these materials, can handle them without too many problems. The benefit of developing the capability to process very thin materials is that is makes processing of standard thickness materials easier and more robust.

Part VI. Processing Thin and Very Thin Laminates: Unicircuit's Experience

Lance Riley, Unicircuit Inc.

Mr. Riley is Vice President of Sales and Advanced Technology for Unicircuit, Inc. Mr. Riley joined Unicircuit in 1996. Mr. Riley has been in the printed circuit board industry for 20 years, and has held various management positions in manufacturing and sales, including Product Development Manager, Advanced Technology Director, and National Sales Manager. As the V.P. of Sales and Advanced Technology he is responsible for research, and market analysis to identify industry trends and developments in technology. Mr. Riley engages with the technology driven companies to assist in cost vs. performance analysis, mission critical/schedule driven programs, and the signal integrity of interconnect structures for system level performance.

Materials Utilized:

- 3M C-Ply
- Gould Upilex
- Nelco N4000-6
- Polyclad 371

Manufacturing Issues & Lessons Learned:

- Artwork modifications
- Material stabilization
- Transportation approach for .001 & .002 cores
- .002 cores with 2oz Cu
- Hipot testing
- Lamination
- Thermal stress testing
- IST testing

OEM Product Deployment:

- Raytheon
- Lucent
- Agilent
- MIT
- Motorola SPS
- Rockwell Collins

Summary:

- End item performance data is very closely held by OEM's and is considered to be confidential and proprietary.
- Products are being deployed in a number of different market sectors.
- Robust manufacturing guidelines have been established.
- In process and final yield data supports that the product is mature, and is production worthy.

Part VII. Benchmark's Experience with Thin Laminates

Steve Patrick, Benchmark Electronics, Inc.

Outline

1) Photos will show no signs of delamination after 6X solder shock

2) The polyimide copper plating adhesion performs well, even when exposed to 6X solder shock.

3) Copper plating adheres well to copper clad of polyimide at interface in the drilled hole even after 6 X solder shock.

4) After BEI's processing of approx. 85 assemblies (some partial, some full assemblies) with 2-4 Dupont layers each, it has been determined that:

   (a) No special handling was required, i.e. temperature, fixturing, etc.
   (b) Not a single failure occurred related to the 1 mil material

5) For full acceptance of the 1 mil material, HALT / HASS testing of a minimum of 6 fully populated units (a seventh unit will be used to establish the recipe for the six) should be performed with the following parameters considered:

   (a) Temperature cycling from -20*C to 100*C at a ramp rate of 60*C per minute and a dwell time of 3 minutes.
   (b) Six axis Random vibration across the unit.
   (c) Units to be system tested after each cycle.

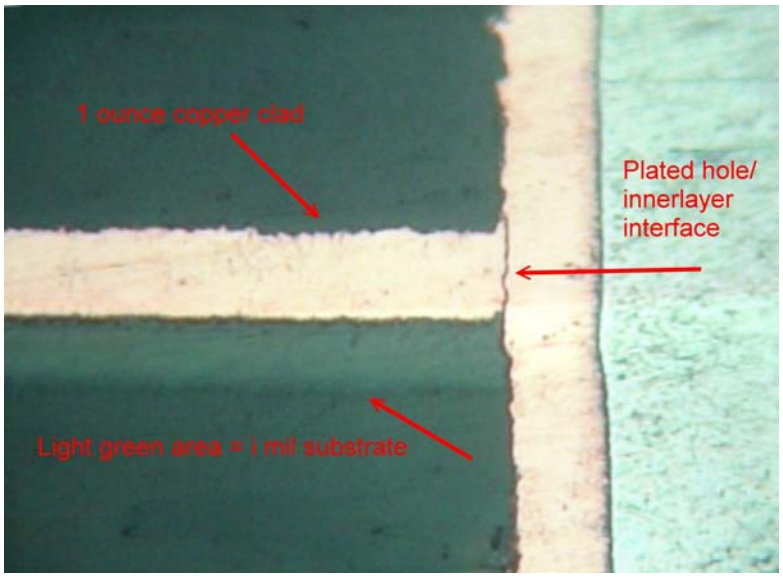


Figure 1: Plated hole inner layer interface. The light green area is the 1-mil substrate.

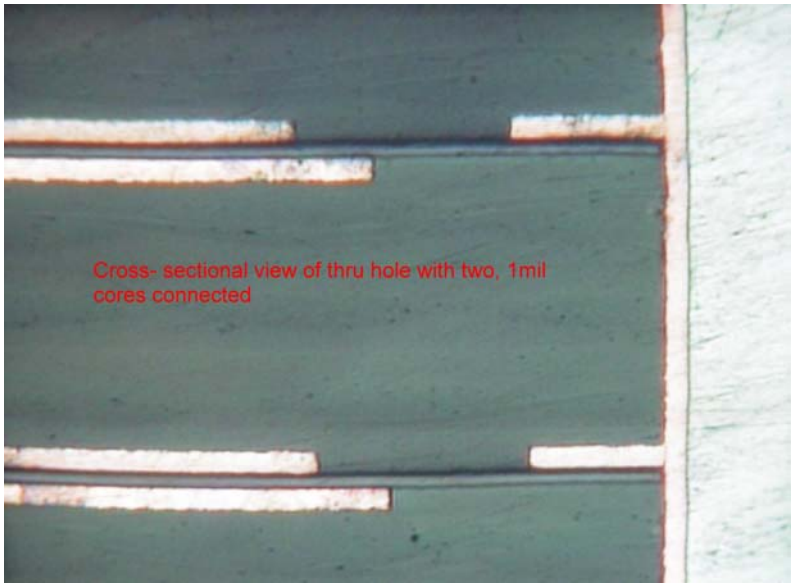


Figure 2: Cross sectional view of through hole with two 1-mil cores connected

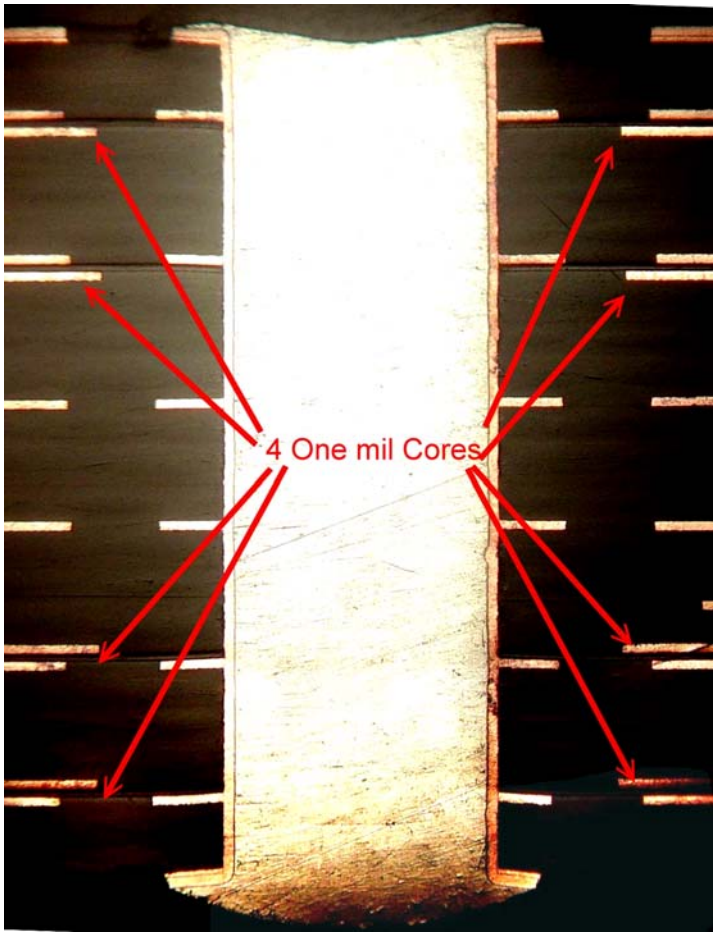


Figure 3: Through hole with four 1-mil core connected.

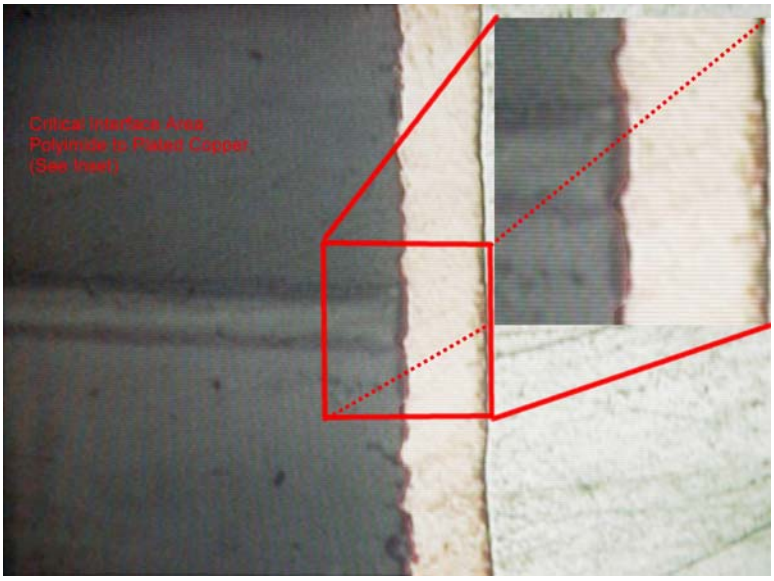


Figure 4: Critical interface area of polyimide to plated copper is shown magnified on the upper-right insert.

Part VIII. Thin Laminates and Power Plane Noise

John Grebenkemper, Ph.D.
NonStop Enterprise Division, Hewlett-Packard Company

Dr. Grebenkemper has worked in the area of signal integrity and high-speed design since 1991. He founded and managed the signal integrity department at Tandem Computers Incorporated, which has recently been acquired by HP. The department was responsible to ensure quality design practices were used in the design of the NonStop® computer systems. For the last few years he has focused on the management of power distribution noise. Previously he has managed departments responsible for printer hardware and software development, product design verification, EMI, and safety. Before going into management, he has worked on projects developing satellite communications systems and microwave receiver design. Dr. Grebenkemper received his PhD in EE from Stanford University. He has received seven patents and published more than 30 papers.

Abstract

Thin laminates that are placed between a power and ground plane may be used to substantially reduce noise in digital systems. The thinness not only increases the capacitance between the power and ground, but also reduces the inductance of the power distribution and increases the loss for any noise that is generated.

Introduction

Lower supply voltages, higher switching currents, and decreased edge rates are all increasing the noise susceptibility of digital systems. The equivalent series inductance of bypass capacitors is decreasing their effectiveness to deal with the increasing noise due to the faster switching rates. Thin laminates between power and ground planes is one of the few methods that can still be used to reduce the noise on power planes.

This paper will look at both predictions and measurements of the noise reduction capability of thin laminates. The predictions were done with an internal HP tool that uses frequency domain analysis to compute the noise level given a set of switched current sources, a power and ground plane pair to distribute power, and a set of bypass capacitors. The measurements were done on a CPU daughtercard that included a MIPS processor and secondary cache.

Theory

Consider a power and ground plane separated by a dielectric material such as FR-4. An active device is connected across the power and ground planes by a pair of vias. When the current demand of the active device increases, it attempts to draw more current between the power and ground planes. Initially, the energy for this additional current comes from the electric field between the power and ground planes, which causes the voltage across the power and ground planes to decrease. Halving the thickness of the laminate between the two planes will double the electric field strength which provides additional charge to support the extra current demand.

The drop in voltage across the section of the plane around the via pair will now cause more charge to flow into this region from other adjacent sections of the power and ground plane pair. The rate at which this current can flow into the charge depleted region is limited by the series inductance of the power and ground planes to the adjacent sections. Halving the thickness will halve the series inductance which allows the additional charge to flow to support the extra current demand.

The power and ground plane form a two-dimensional transmission line so the impedance is not constant as in the more familiar one-dimensional transmission line. However, the impedance is proportional to the laminate thickness. This means that halving the laminate thickness will decrease the distribution impedance by half. In this case, an instantaneous current step will generate an instantaneous voltage step that is half the value compared to the original thickness.

However, doubling the dielectric constant will not halve the noise. It will have no effect on the size of the initial noise step due to an instantaneous current change. The reason for this has to do with the effect of the dielectric constant on the propagation velocity. If we double the dielectric constant, we will reduce the propagation velocity by the square root of 2. The area from which we can extract charge in a given propagation time is reduced by a factor of 2. So the net effect is that the amount of charge available to supply the extra current remains exactly the same.

From these various arguments we might conclude that the total noise between a power and ground plane will be halved if we reduce the thickness of the laminate by a factor of two. However, this is not the case because it does not include the effects of the components connected across the power plane and the noise propagation between the power and ground planes.

When the current draw of an active device changes, it causes a radial wave to propagate from the point on the power and ground plane pair where the current change was initially drawn. This wave will propagate outwards at the speed of light in the laminate. When the wavefront reaches the edge of the power and ground plane pair, it will be reflected back into the board. Since most boards are not circular, the waveform quickly becomes quite complex with its amplitude depending on the location on the power plane. In the frequency domain, this will be seen as resonances in the board at the higher frequencies.

There are several mechanisms that dissipate this noise power, but on most boards they are not sufficient to damp the wave until it has reflected from the board edges multiple times. The resistance of the copper in the power and ground planes creates I^2R loss. The conductance of the laminate dielectric has V^2G loss. The resistance in bypass capacitors and the load resistance of the active devices also contribute to the wave attenuation. These loss mechanisms eventually attenuate the noise from a single event.

Predictions

The predictions assume that the power plane and ground plane pair is 3” by 6” (7.6 cm by 15.2 cm) with a separation of 4 mils (10^{-4} meters). The noise source was assumed to be a 2 ns pulse width with a 200 ps risetime. The calculations were done for a specific board size and noise source pulse. Changing these parameters will change the absolute magnitude of the results. However, the general trends are still applicable.

The thickness of the laminate that separates the power and ground planes plays an important role in reducing the noise on the power plane. A thinner laminate layer will create more capacitance, which can

provide additional charge when the active devices change their current demands. Additionally, the decreased spacing between the power and ground planes will reduce the series inductance, which results in a lower impedance of the power distribution network. Finally, a thinner laminate also increases the dissipation of noise on the power plane. This occurs because a thinner layer generates a higher electric field between the power and ground planes, which causes more current to flow in the copper conductors and increases the I^2R loss in the conductor.

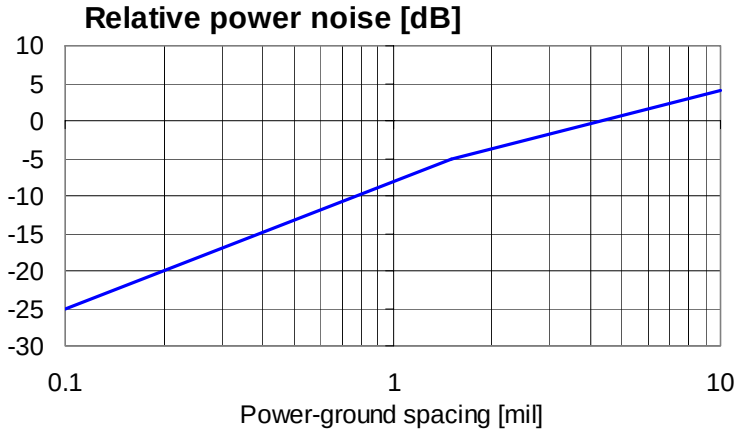


Figure 1. Predicted total RMS noise on a printed circuit board power plane as a function of the power to ground plane spacing. A decrease in the spacing reduces the noise.

Figure 1 shows the total RMS noise on the test board as the spacing between the power and ground plane is varied. The total noise falls by about 10 dB per decade for spacings greater than 1.5 mils, and at 20 dB per decade for smaller spacings. There is a significant benefit to make the spacing less than 1 mil. Reducing the dielectric thickness from 3 mils to 0.3 mils would reduce the total RMS noise by about 15 dB.

Measurements

From the above predictions, we would expect that reducing the laminate thickness would significantly reduce the noise on an actual board. A comparison was done on a processor daughtercard that contained a 550 MHz MIPS R14K processor and nine secondary cache SRAM's. The processor daughtercard was 5 ¼ by 5 ¼ inches.

One version of the daughtercard was built with a 3 mil FR-4 type laminate separating the power and ground planes. The other was built with 8 micron (0.3 mil) C-Ply laminate supplied by 3M. The C-Ply material has a dielectric constant of 16 and a loss tangent of 0.005 at 10 kHz to 0.1 at 1 GHz.

The measured power plane used a number of bypass capacitors shown in the table below.

Quantity	**Value**	**Package**
9	2.2 µF	8-pin IDC
15	0.1 µF	0603
15	1000 pF	0603
15	100 pF	0603

A power spectral measurement was made of the two different processor daughtercards. The connection to the power and ground planes was brought out on a pair of vias specially created for this purpose. The one with the 3-mil FR-4 core showed significant peaks and far more energy in the noise between the

power and ground planes. The one constructed with the C-Ply laminate greatly reduced those peaks, especially at higher frequencies. A third measurement was made on the C-Ply laminate by removing all of the high frequency bypass capacitors. Below 50 MHz, the noise increased due to insufficient low frequency capacitance to handle the switching current transients. Above this frequency, the noise between the two cases is nearly indistinguishable.

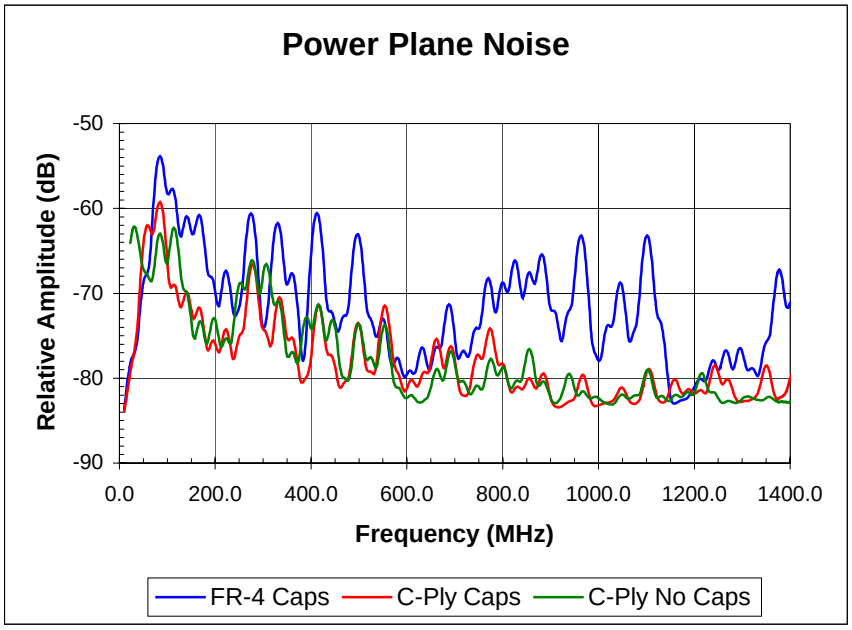


Figure 2 Power spectrum of processor daughter card constructed with FR-4 and C-Ply cores. The noise floor of the measurement was –83 dB on this plot.

The total noise power from the spectrum analyzer measurement was integrated over a frequency range of 50 to 1400 MHz to determine the noise reduction due to the change in laminate thickness. The following table shows the results.

FR-4 with no HF bypass capacitors	+6.8 dB
FR-4 with HF bypass capacitors	+0.0 dB
C-Ply with no HF bypass capacitors	-6.5 dB
C-Ply with HF bypass capacitors	-7.1 dB

There is only a 0.6 dB difference in the noise on the C-Ply core when it is measured both with and without high-frequency bypass capacitors. The C-Ply board with no high-frequency bypass capacitors is nearly as quiet as the one with all of the high-frequency bypass capacitors. It should be possible to add some additional low-frequency bypass capacitors on this board to reduce the noise below 50 MHz and otherwise not use any high-frequency bypass capacitors.

Conclusions

Thin laminate materials can significantly reduce the noise on a power plane compared to standard FR-4 materials. This is particularly true at frequencies above 100 MHz. There is little benefit at frequencies below 100 MHz. In this lower frequency range, the bypass capacitors are much more effective and the physical size of the board is not likely to generate resonant frequencies of the board.

Part IX. Frequency Dependent Capacitance and Inductance of Thin and Very Thin Laminates

Istvan Novak, SUN Microsystems

Istvan Novak is signal-integrity senior staff engineer at SUN Microsystems, Inc. He designs high-speed serial and parallel buses, power-distribution networks, bypassing and decoupling of packages and printed-circuit boards for workgroup servers. He creates simulation models, and develops measurement techniques. Istvan has more than twenty years of experience with high-speed digital, RF, and analog designs. He is Fellow of IEEE and has a PhD in Electrical Engineering.
istvan.novak@sun.com, (tel): 781-442-0340

Abstract

As a figure of merit, thin dielectric laminates are usually characterized by their low-frequency static capacitance. For simulation purposes, the high-frequency limit inductance is used. It is shown that various dielectric materials have differing frequency dependence of their static capacitance, and in thin laminates, where the conductive layer's thickness is not negligible compared to the dielectric thickness, inductance also shows a strong frequency dependence. Thirteen different thin laminates have been characterized in the same test board. Over three decades of frequency, polyimide dielectric showed a capacitance drop of about 1%, whereas epoxi-based dielectrics had approximately 10% capacitance drop. Inductance also drops as frequency increases: at low frequencies the average current-loop height equals the sum of dielectric and conductive layers. At high frequencies, the loop height approaches the dielectric thickness. With sub mil dielectric thickness values, a one or two ounce copper layer created a more than 2:1 change in inductance over the 10-300MHz frequency range.

I. Introduction

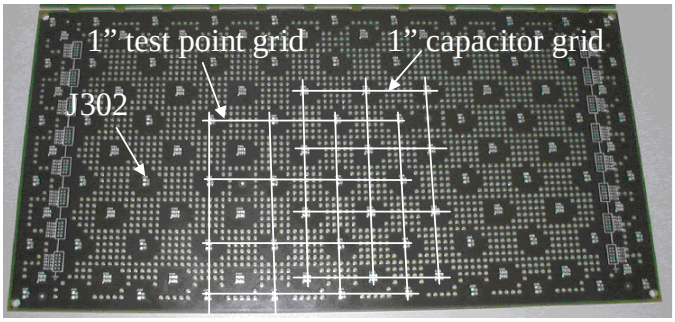
Thin and very thin laminates for power-distribution applications have been extensively described in the literature. For low-power and low-current applications, the static plane capacitance is the important parameter; thin laminates for such applications are marketed as embedded capacitance [1]. For high-power applications, and above the series resonance frequency of power/ground planes, the inductance is the primary parameter [2]. The capacitance of laminates is usually specified at 1MHz, whereas the inductance is usually calculated as the high-frequency limit inductance, which assumes that the current penetration of the conductive planes is negligible compared to the dielectric thickness. For thin and very thin laminates, however, the inductance, and/or capacitance may be a strong function of frequency. Power-ground laminates can be simulated (among other options) with transmission-line grids [3], or by using analytical cavity-resonance formulas [4]. An important goal of power-plane simulations is to identify potential plane resonances. To do this accurately, the frequency dependent inductance and capacitance values should be known. In this paper the measured frequency dependent capacitance, resistance and inductance curves are presented for thirteen thin and very thin laminates:

- five laminates from DuPont's Interra™ HK04 series [5] (three 25um laminates with one and two-ounce RA and ED copper; and two 50um laminates with one and two-ounce RA copper)
- three laminates from the Oak-Mitsui FaradFlex™ unreinforced epoxi series [6] (24um, 16um and 12um laminate thickness with one-ounce ED copper)
- two glass-reinforced epoxi laminates from Matsushita [7] (ZBC2000™ and ZBC1000™).
- three laminates from 3M's C-Ply™ series of unreinforced filled epoxi line (24um, 12um, and 8um laminate thickness with one-ounce copper) [8]

II. Test board construction and measurements

The same impedance-characterization test board (described in detail in [8]) was built with the laminates. The boards were manufactured in three groups, by two different fabricators. The impedance profiles of the bare and shorted 10”x5” main areas of the test boards were measured with the instrumentation and methodology described in [9], the frequency-dependent capacitance and inductance were extracted as described in [10]. Each board has two uniform one-inch grids with a half-inch offset: one of the grids defines the locations of 66 test points, where the impedance measurements were taken. The second grid defines the locations of the 50 eight-terminal 1206-size capacitor pads. The short was implemented by soldering solid copper strips across the pads of the 28 capacitor locations along the board periphery. The shorted capacitor pads were previously characterized: they each create a 50pH inductance in series to 0.5 milliohms resistance. The 28 shorted capacitor pads thus cumulatively create a short along the board’s periphery with less than 2pH inductance and less than 20 microohms resistance. The bare and shorted boards were measured for self and transfer impedances in the 1kHz to 1.8GHz frequency range, with an HP4395A network analyzer below 10MHz, and an HP4396 network analyzer above 100kHz.

The board is shown in Figure 1 (on the left), with the two 1” grids identified. The self-impedance traces of the bare and shorted boards were measured at test-point location J302. It was found that at least 1” away from the shorting positions, the location of test point had very minimal influence on the measured resistance and inductance in the self impedance of the shorted board. This is illustrated by the extracted inductance surface of Figure 1 (on the right), which shows the inductance data extracted from a full scan of a shorted ZBC2000 test board.



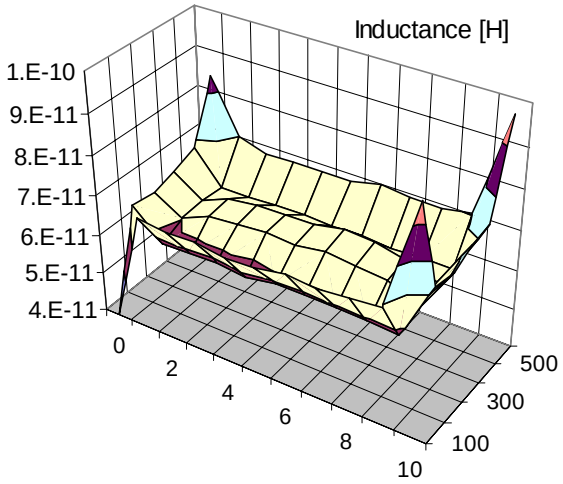


Figure 1: Test board geometry and test point on the left. Extracted inductance surface at 100MHz on a shorted ZBC2000 test board is shown on the right.

III. Extracted characteristics

The graphs below show the static capacitance extracted from the bare-board self-impedance data, and the resistance and inductance extracted from the shorted board self-impedance data.

Note that the static capacitance was corrected for the plane inductance, which extends the validity of capacitance curves up to about the first modal resonance minimum. For the given size board and dielectric materials, this first minimum is in the 40-70MHz for filled and in the 100-150MHz range for unfilled resins. The sharper decline of capacitance close to and above the first modal minimum should not be considered in the laminate comparison.

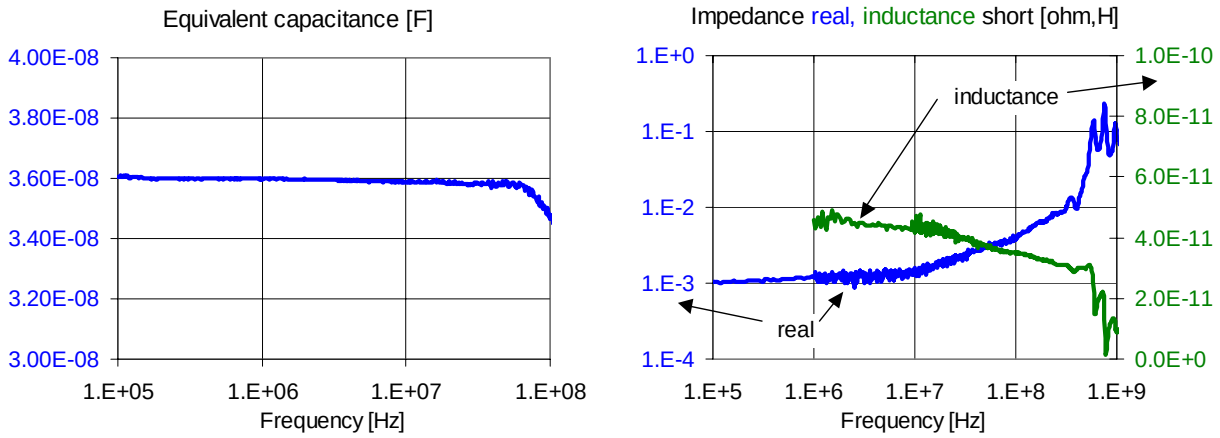


Figure 2. Capacitance, resistance and inductance of board with HK042536E laminate.

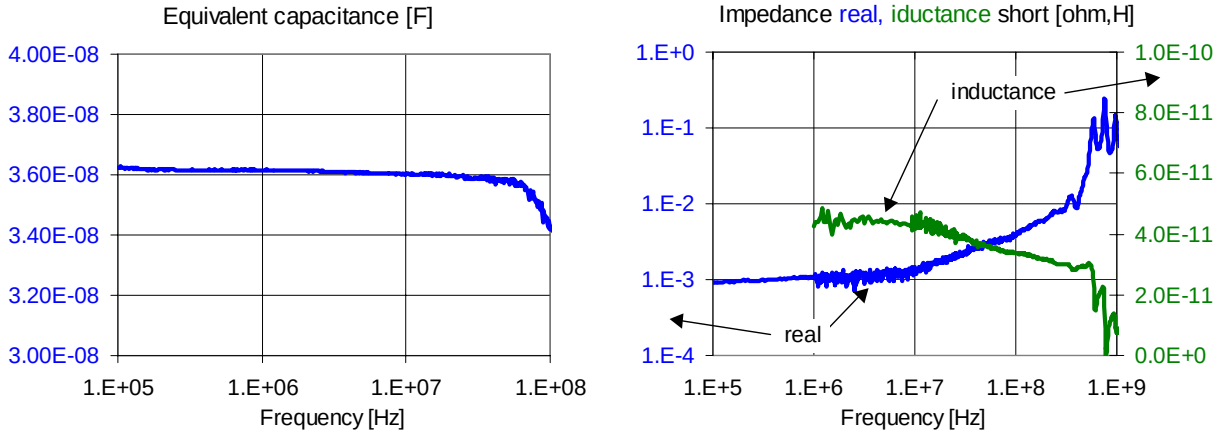


Figure 3. Capacitance, resistance and inductance of board with HK042536R laminate.

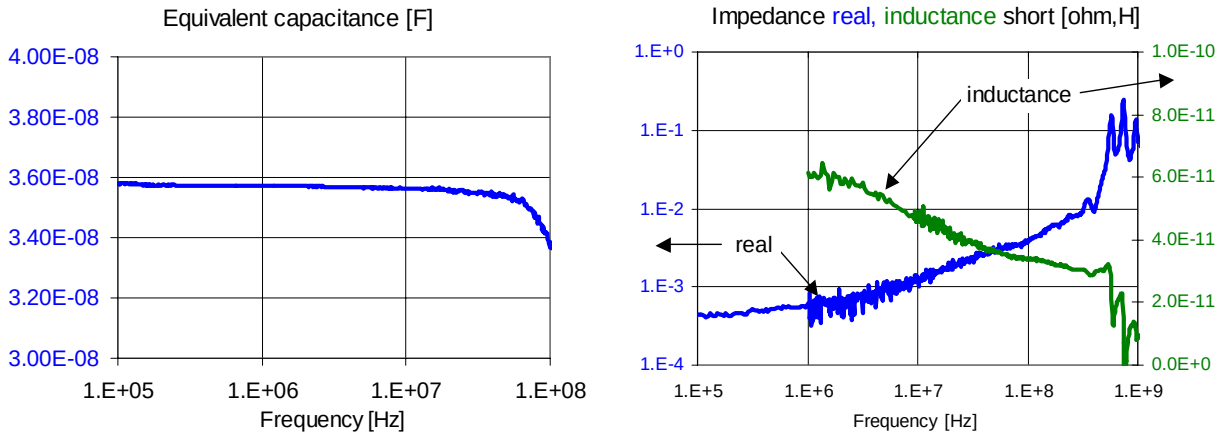


Figure 4. Capacitance, resistance and inductance of board with HK042572R laminate.

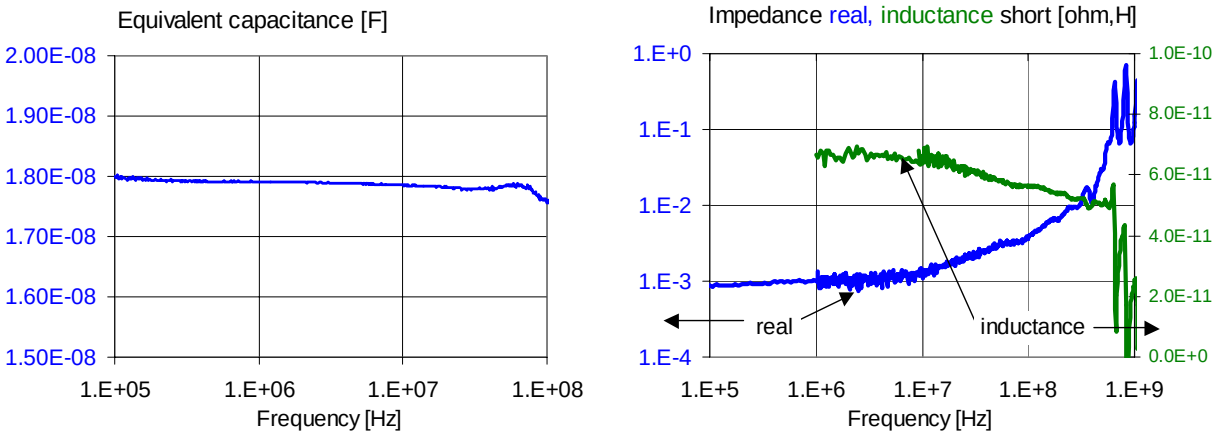


Figure 5. Capacitance, resistance and inductance of board with HK045036R laminate.

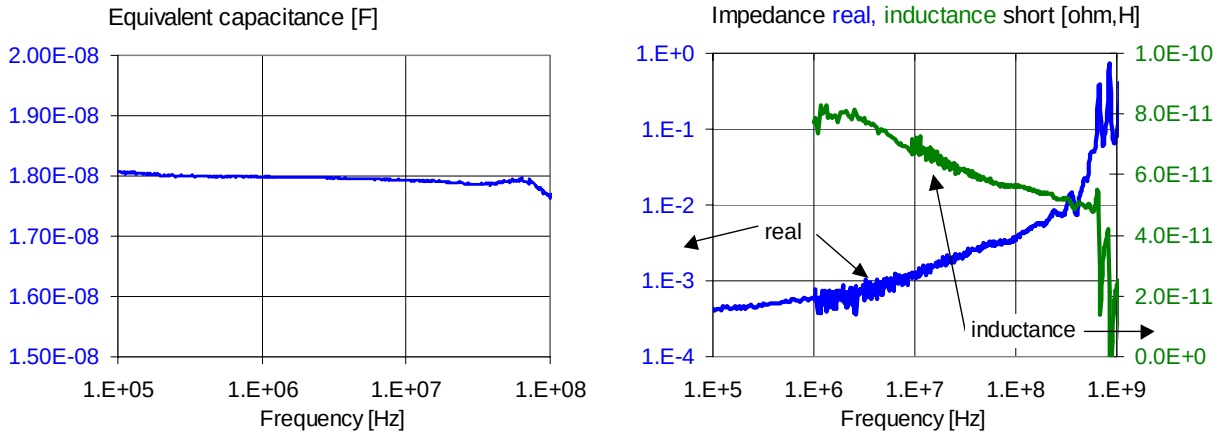


Figure 6. Capacitance, resistance and inductance of board with HK045072R laminate.

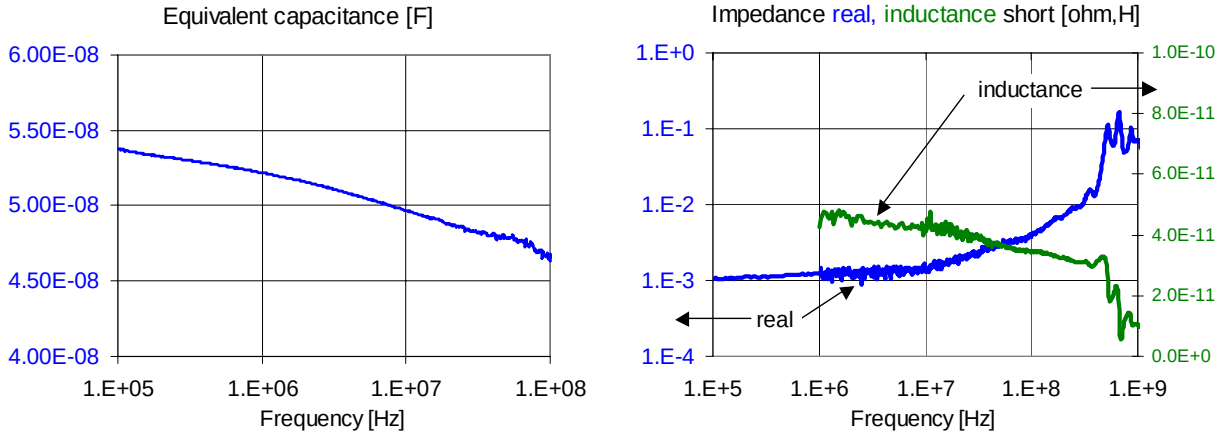


Figure 7. Capacitance, resistance and inductance of board with FaradFlex BC24 laminate.

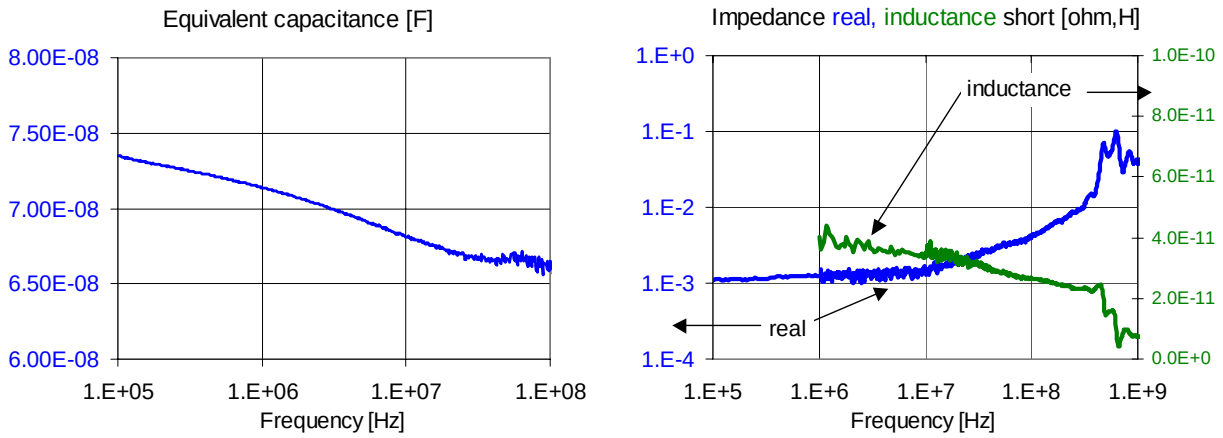


Figure 8. Capacitance, resistance and inductance of board with FaradFlex BC16 laminate.

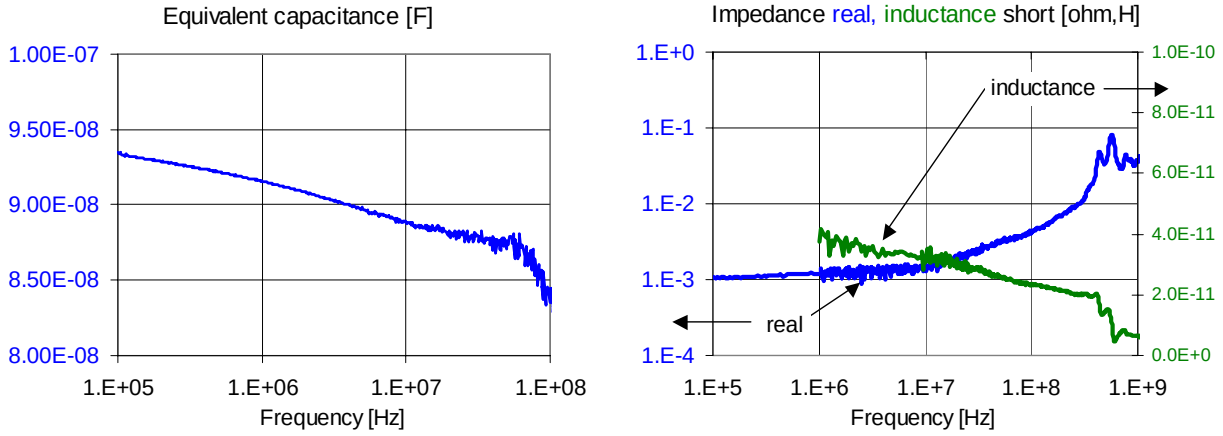


Figure 9. Capacitance, resistance and inductance of board with FaradFlex BC12 laminate.

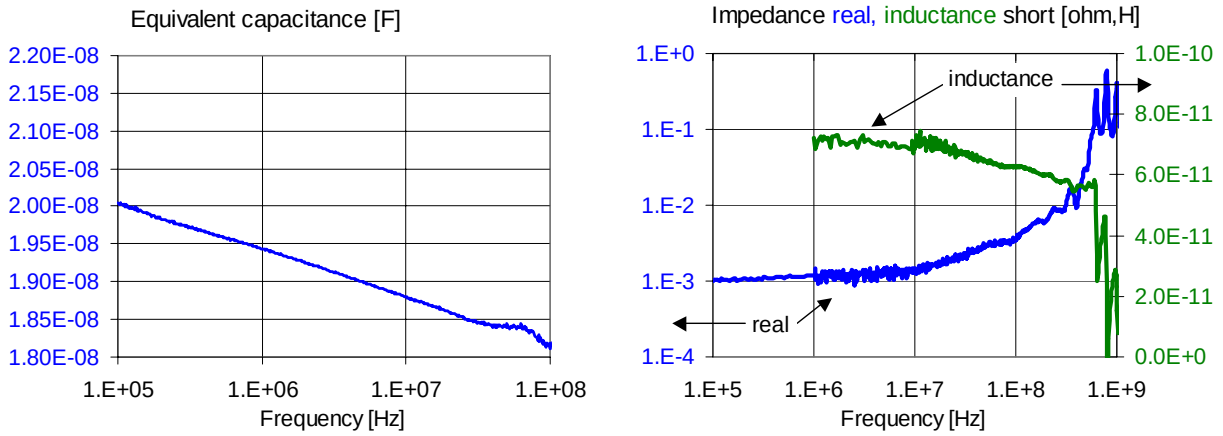


Figure 10. Capacitance, resistance and inductance of board with Matsushita ZBC2000 laminate.

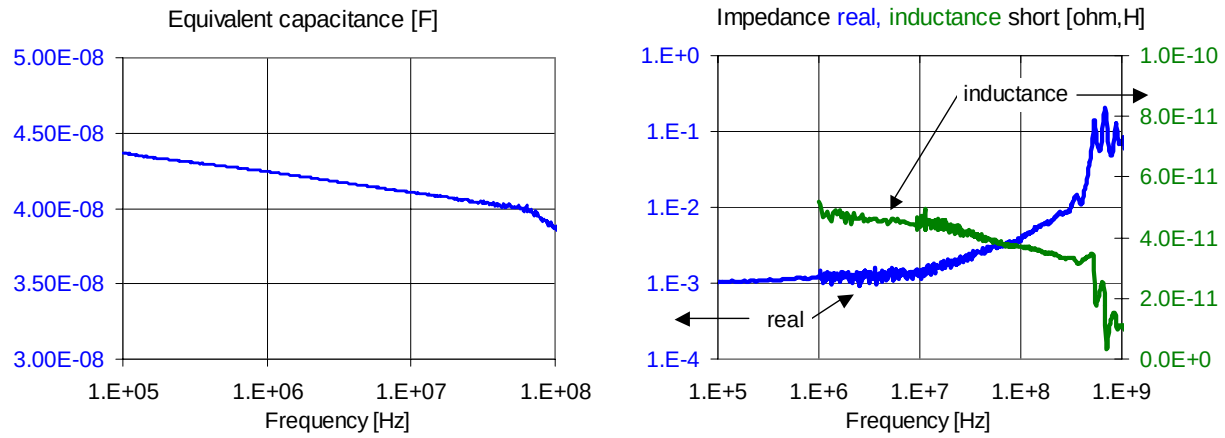


Figure 11. Capacitance, resistance and inductance of board with Matsushita ZBC1000 laminate.

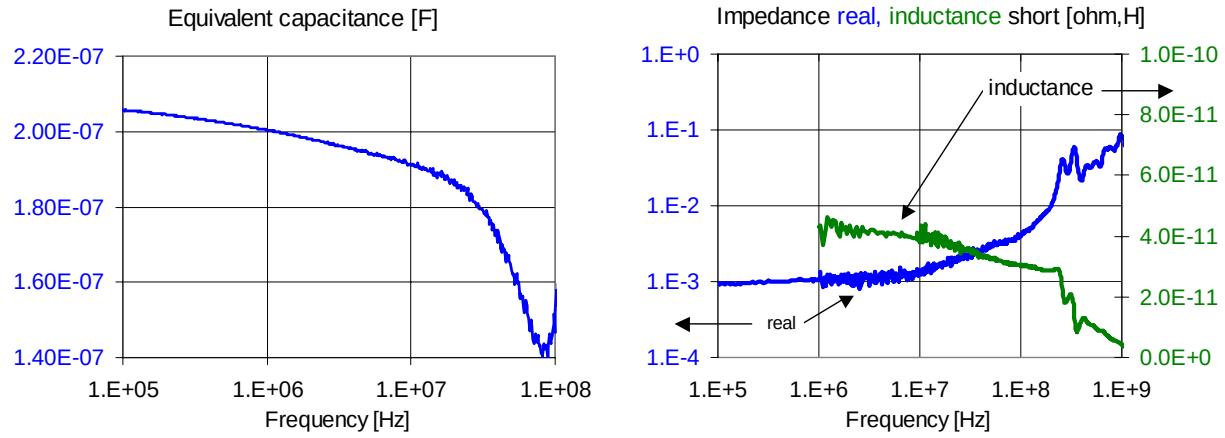


Figure 12. Capacitance, resistance and inductance of board with 3M C-Ply 24um laminate.

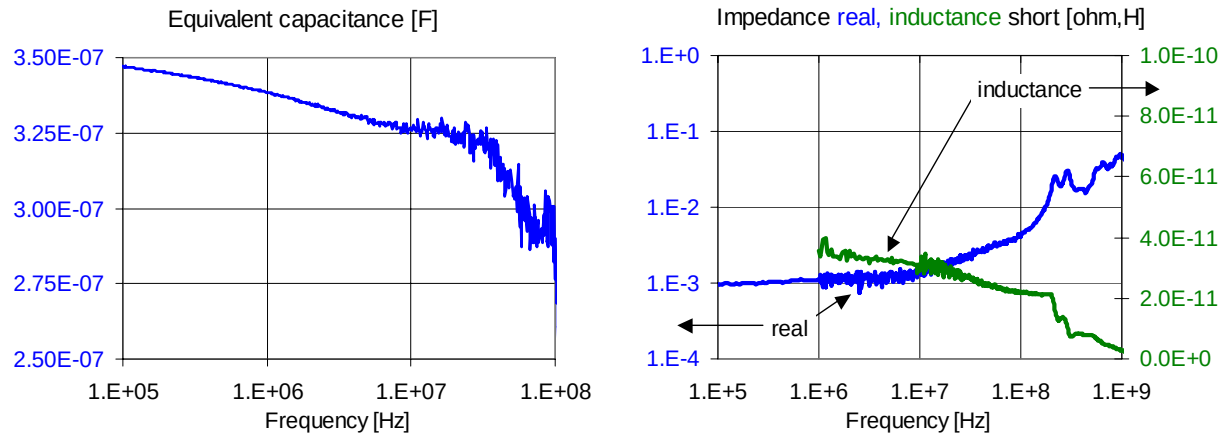


Figure 13. Capacitance, resistance and inductance of board with 3M C-Ply 12um laminate.

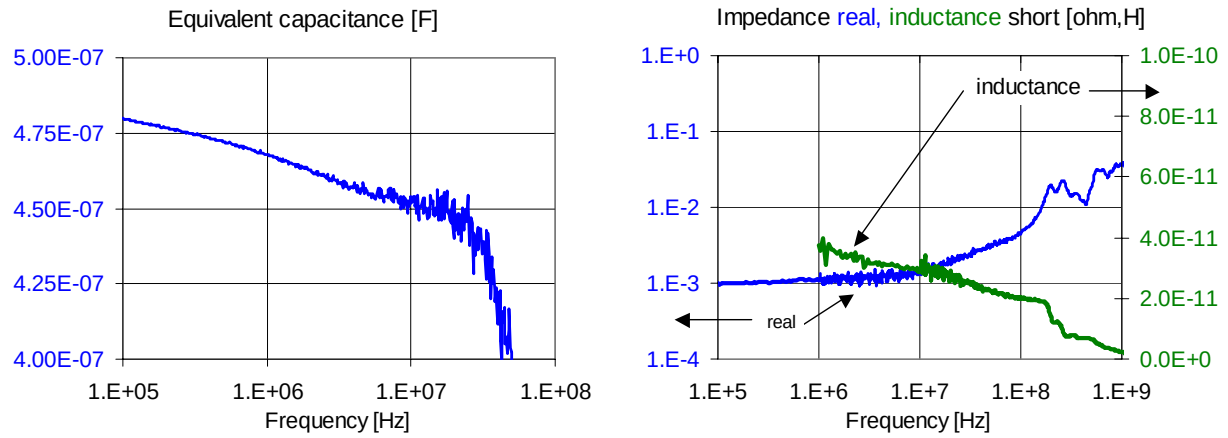


Figure 14. Capacitance, resistance and inductance of board with 3M C-Ply 8um laminate.

The shorted plane's impedance is dominantly resistive at very low frequencies, making the inductance extraction very noisy; therefore the inductance curves are plotted only above 1MHz.

The shorted boards' impedance profiles show a dominant parallel resonance between the plane's static capacitance and shorting structure, followed by structural resonances. The lowest resonance frequency for the given-size boards is in the 400-600MHz range for unfilled, and in the 200-300MHz frequency range for filled resin laminates. The inductance cannot be extracted beyond the lowest modal resonance peak, therefore the sharp drop in the extracted inductance beyond this lowest parallel resonance frequency should not be considered in the laminate comparison.

Note that over more than two decades of frequency there is a noticeable change of both resistance (real part of impedance) and inductance: as frequency goes up, resistance increases and inductance decreases. There is more inductance variation in laminates where the ratio of copper thickness and dielectric thickness is higher.

IV. Laminate comparison

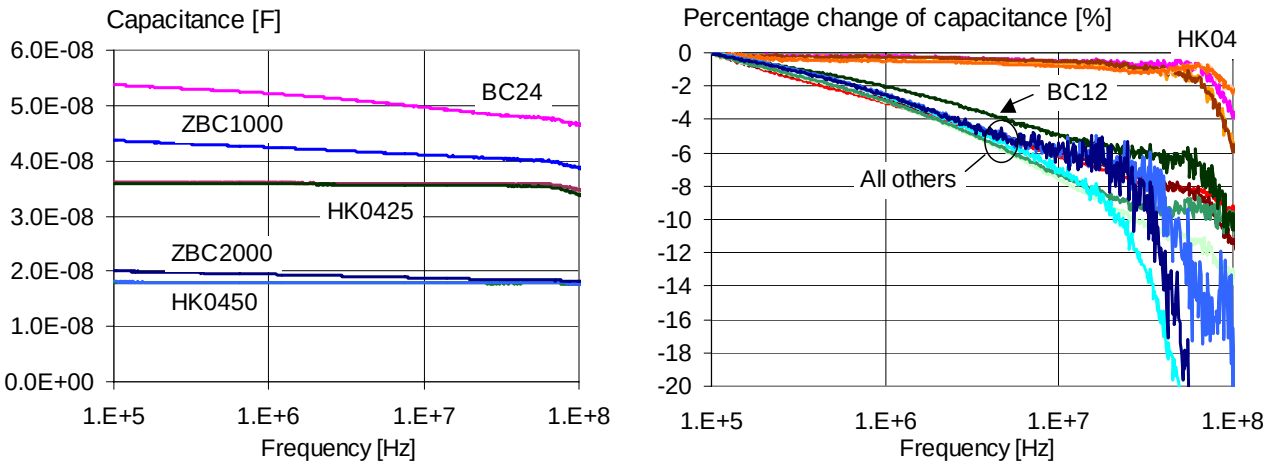


Figure 15: Absolute capacitance versus frequency of unfilled laminates on the left, percentage loss of capacitance versus frequency of all measured laminates on the right.

Figure 15 through 17 compare the capacitance and inductance of the measured laminates. Note that the capacitance of unfilled polyimide stays within 1% of its low frequency value over three decades of frequency. Over the same frequency range, the capacitance of filled and unfilled resins drops approximately 10%. As expected, thinner dielectrics exhibit overall lower inductance. With thinner dielectrics and/or thicker copper, the frequency variation of inductance becomes stronger. Figure 17 shows good correlation between the measured and estimated frequency dependence of inductance based on the dielectric thickness and skin depth within the conductive layers.

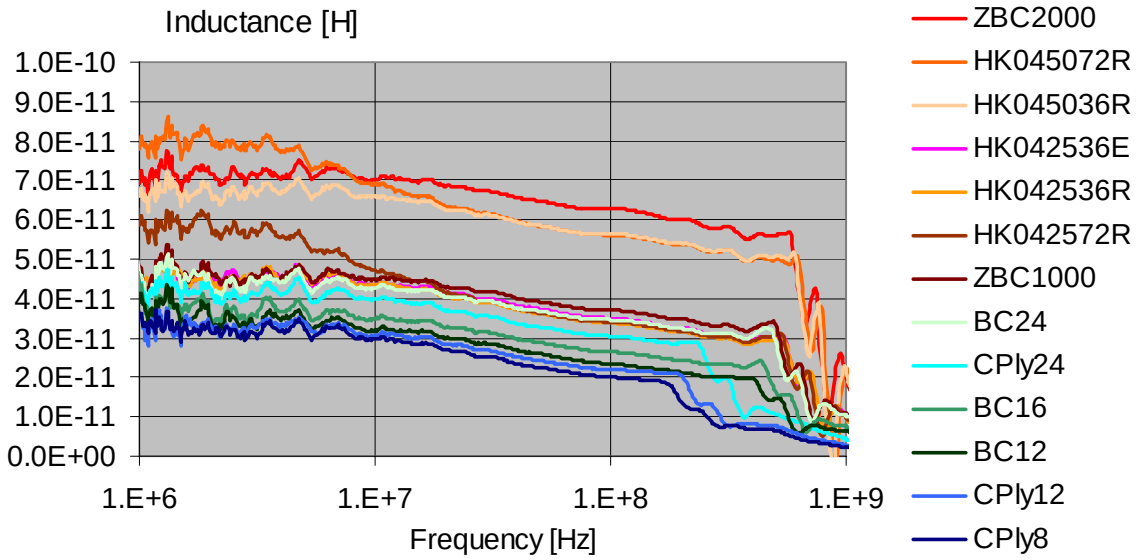


Figure 16: Inductance versus frequency curves of various laminates. The sequence of legend on the right corresponds to the top-down sequence of curves.

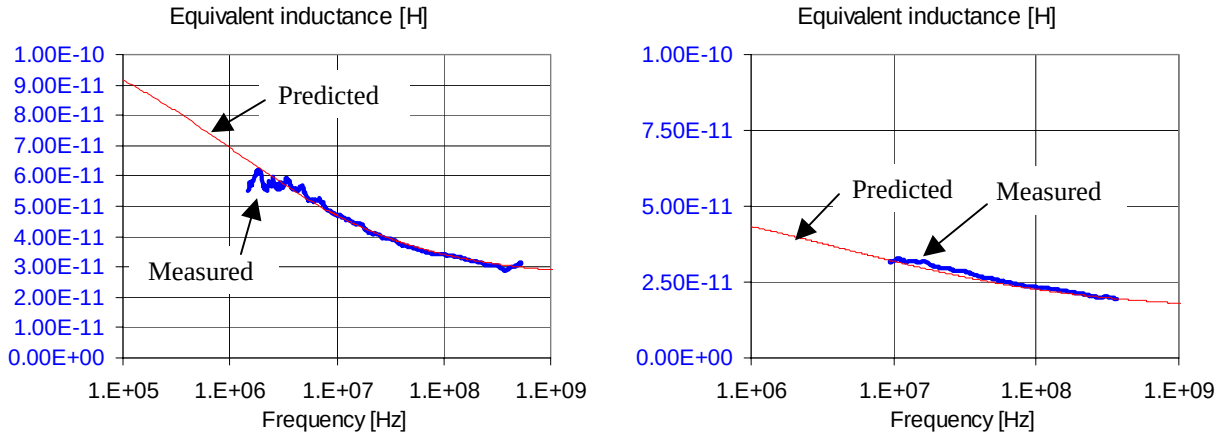


Figure 17: Measured versus predicted inductance for board with HK042572R (left graph) and BC12 (right graph) laminate.

Acknowledgements

The author wishes to thank Merix and Sanmina-SCI to create the test boards. Interra, FaradFlex, ZBC2000, ZBC1000, C-Ply are trademarks of DuPont, Oak-Mitsui, Sanmina, Sanmina, and 3M, respectively.

References

[1] Charbonneau, “An Overview of the NCMS Embedded Capacitance Project,” NCMS Embedded Capacitance Conf., Tempe, AZ, February 28-29, 2000.

[2] Valerie St. Cyr, Istvan Novak, “Thin Laminates for Power Distribution – How Thin is Thin Enough,” Half-Day TecForum at DesignCon2002, High Performance System Design Conference, Jan. 28 – Feb. 1, 2002, Santa Clara, CA

[3] Smith, Roy, Anderson, “Power Plane Spice Models for Frequency and Time Domains,” Proceedings of EPEP2000, October 23 – 25, 2000, Scottsdale, AZ.

[4] Eged, Balogh, “Analytical Calculation of the Impedance of Lossy Power/Ground Planes,” Proceedings of the Instrumentation and Measurement Technology Conference, May 21-23, 2001, Budapest, Hungary

[5] http://www.dupont.com/fcm/interra/

[6] John Andresakis, Takuya Yamamoto, Pranabes Pramanik, Nick Biunno, “Performance of Polymeric Ultra- thin Substrates For use as Embedded Capacitors: Comparison of Unfilled and Filled Systems with Ferroelectric Particles,” TecForum TF9; DesignCon 2004, February 2-5, 2004, Santa Clara, CA

[7] http://www.matsushita.jp

[8] Joel Peiffer, Bob Greenlee, Istvan Novak, "Electrical Performance Advantages of Ultra-Thin Dielectric Materials used for Power-Ground Cores in High-Speed, Multilayer Printed Circuit Boards" IPC Expo 2003, Long Beach, CA, March 25-27, 2003

[9] "Frequency Domain Power Distribution Measurements - An Overview" in HPTF1: Measurement of Power-Distribution Networks and Their Elements, at DesignCon 2003 East, June 23-25, 2003, Boston, MA

[10] Istvan Novak, Jason R. Miller, “Frequency-dependent characterization of bulk and ceramic bypass capacitors,” Proceedings of EPEP2003, October 27-29, 2003, Princeton, NJ.