Manuscript for TF-MP3 “Controlled-ESR Bypass Capacitors Have Arrived” at DesignCon 2007, January 29 – February 1, 2007, Santa Clara, CA

DesignCon 2007

History of Controlled-ESR Capacitors at SUN

Istvan Novak, Gustavo Blando, Jason R. Miller

Sun Microsystems, Inc.
Tel: (781) 442 0340, e-mail: istvan.novak@sun.com

Author Biographies

Istvan Novak is signal-integrity engineer at SUN Microsystems, Inc. Besides signal-integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is Distinguished Engineer of SUN and Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

Gustavo Blando is a signal Integrity engineer with over 10 years of experience in the industry. Currently at Sun Microsystems he is responsible for the development of new processes and methodologies in the areas of broadband measurement, high speed modeling and system simulations. He received his M.S. from Northeastern University.

Jason Miller is currently a Staff Engineer at Sun Microsystems where he works on ASIC development, ASIC packaging, interconnect modeling and characterization, and system simulation. He received his Ph.D. in Electrical Engineering from Columbia University.

Abstract

Power distribution networks can benefit from bypass capacitors with specified minimum/maximum ESR. Controlled-ESR capacitors can be created in several different ways. In bulk capacitors it is mostly a sorting requirement. In MLCC parts the task is two-fold: increasing and controlling ESR. This paper summarizes the major steps undertaken at SUN Microsystems Workgroup Server business unit in creating controlled-ESR capacitors.

I. Introduction

Figure 1 shows two illustrations from SUN servers. The photo on the left shows the CPU module from a SUN Enterprise 450 server. The 4”x6” board, designed in the mid 1990’s, had one CPU, two major supply rails, and a total of 351 bypass capacitors. The photo on the right shows the CPU module from a V880 server. The 10”x20” board, designed a few years later, has two CPUs, eight major supply rails, and a total of 1907 bypass capacitors.

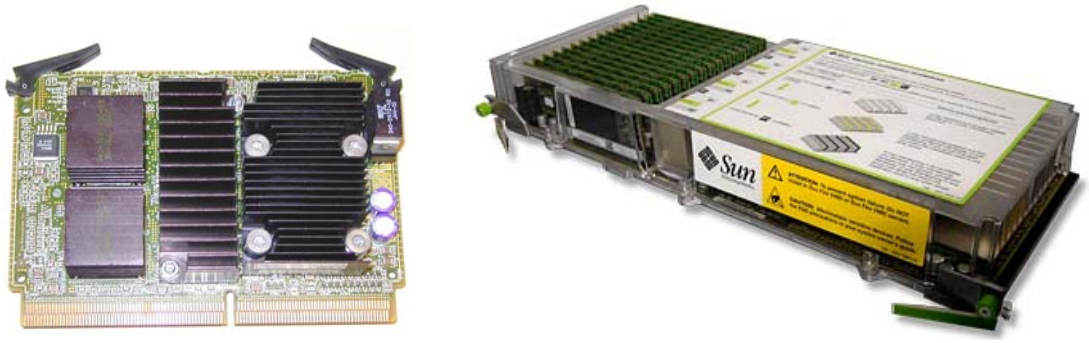

Figure 1: *Two illustrations from SUN servers. Left: E450 CPU module, approximately 4”x6” in size, designed in the mid 90’s. Right: V880 CPU module, approximately 10”x20” in size, designed in the late 90’s. Note that the scales are different for the two photos.*

The increase in board size, in total power and in signaling speed of single-ended system buses brought the realization that the power-distribution network design methodology tailored to the needs of the previous generation [2] would not provide the optimum solution. Large-size planes may resonate at frequencies close to clocks and system-bus frequencies. To suppress plane resonances one possible option is to provide resistive damping to the plane, in form of R-C termination along the plane edge [3]. Another option is to use very thin power-ground laminates, such that the copper losses combined with the low characteristic impedance of the planes suppress modal resonances [4]. At the time of the design, very thin laminates, which are becoming more readily available today [5], were not widely available yet. To implement the resistive termination of planes, series capacitors have to be used to avoid large DC current through the termination network. A convenient choice with discrete implementation is to use bypass capacitors with ESR values such that it matches the resistance value of an R-C termination element. For typical designs this would require ESR values in the hundreds of milliohm to ohm range. Moreover, the part would need to exhibit low inductance. Multi-layer ceramic capacitors (MLCC) have the required low inductance, but their typical ESR is orders of magnitude lower: usually in the milliohm to tens of milliohm range. Tantalum and electrolytic capacitors may have the sufficiently large ESR, but those parts usually come with much higher inductance, unacceptable for high-frequency applications. In addition, traditionally capacitors are specified either with a maximum or typical ESR value, the minimum ESR is not guaranteed.

In the same timeframe it was also realized that not only suppressing plane resonances, but creating flat impedance profiles, too, can benefit from capacitors with increased and/or controlled ESR [6]. Flat impedance profiles of the power-distribution network guarantees the lowest value of worst-case transient noise [7].

The above realizations initiated the search for controlled-ESR bypass capacitors.

II. Discrete implementations

Plane termination elements with an ohm or higher resistance value can be constructed of a discrete capacitor and a discrete resistor. The two parts together will inevitably have higher inductance then the inductance of just one of the parts. With small-size components and aggressive layout/mounting, 1 nH inductance may be achievable. The 1 nH inductance has an approximately 150 MHz cutoff frequency with a 1-ohm resistance, which is acceptable for large board applications. *Figure 2* illustrates the impact of resistive plane termination (Dissipative Edge Termination; DET) in the measured impedance profile.

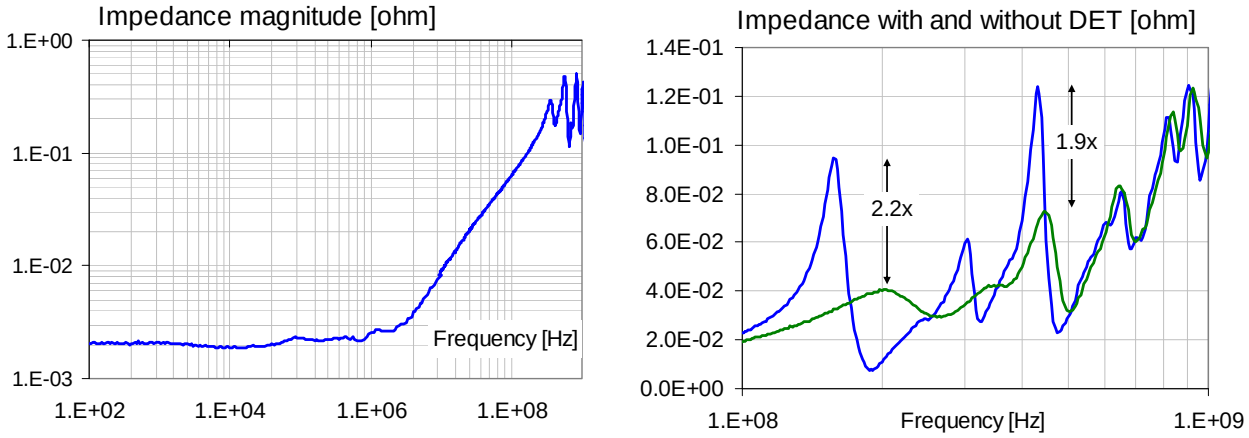

***Figure 2**: Left: measured wide-band self-impedance profile on a SUN CPU module, high-current rail. Right: high-frequency impedance profile of the same rail with and without Dissipative Edge Termination.*

III. Embedded implementations

For power-distribution designs with multiple thin laminates, the required resistance and inductance values become unmanageable in discrete form. However, sub-ohm resistances can be created with very low inductance in embedded printed form [8].

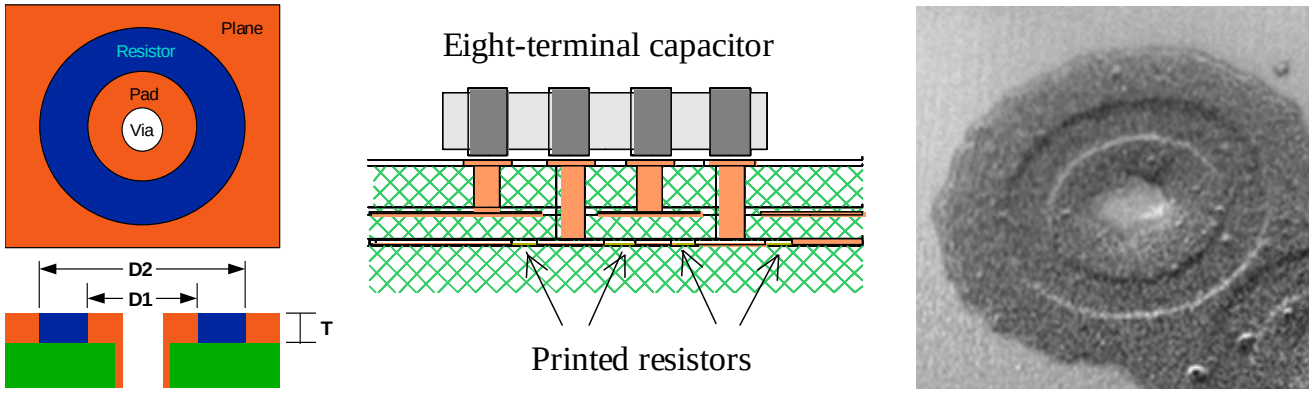

***Figure 3:** Annular-ring resistor to create controlled-ESR capacitors. Left: construction concept. Middle: side-view of eight-terminal capacitor with printed annular resistors on the plane. Right: photo of printed resistor on an inner plane layer.*

Figure 3 shows a thick-film printed implementation. The annular-ring resistor is printed in the antipad void, bridging the plane to the pad. The printed resistors are directly underneath the multi-terminal capacitor, achieving a few hundred pH of total loop inductance. *Figure 4* shows two versions of the E450 CPU module from Figure 1, side-by-side: one with conventional bypass capacitors, the other with multi-terminal capacitors and embedded printed resistors.

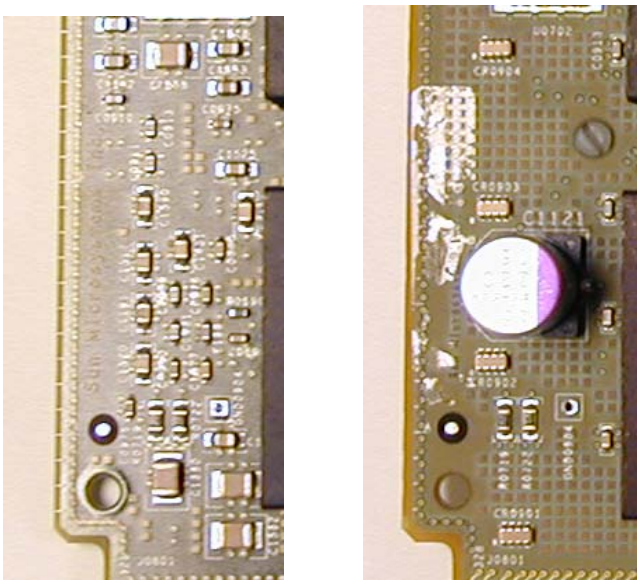

Figure 4: *Left: board detail of CPU module with more than 250 pieces of conventional mid-frequency bypass capacitors. Right: same module with 50 multi-terminal capacitors and embedded printed resistors.*

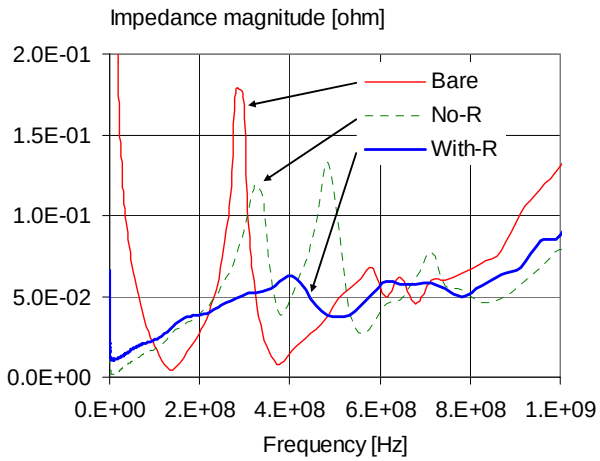

Figure 5: *Self-impedance measured on a 10"x5" test board with 26 pieces of 8-terminal capacitors with and without the embedded resistors. The three traces: a) thin continuous line: impedance of the bare board (for reference), b) dashed line: impedance of the same board with only bypass capacitors, without embedded resistors, and c) solid heavy line: impedance with bypass capacitors and embedded resistors.*

The effectiveness of the solution is shown in *Figure 5*. The graph shows that by adding the embedded resistors in series to the conventional low-ESR low-ESL multi-terminal bypass capacitors, the impedance at 324 MHz is reduced from 0.119 ohms to 0.052 ohms, and at 480MHz the impedance peak is reduced from 0.133 ohms to 0.038 ohms.

IV. Controlled-ESR capacitors

With the realization that discrete R-C implementation compromises the electrical performance, while embedded printed resistors add to the cost, a search started to find a solution to create cost-effective controlled-ESR capacitors with minimal performance compromise. The Workgroup Servers business unit of SUN Microsystems engaged selected capacitor vendors to find a solution. This section gives a brief summary of some of the milestones and results.

AVX experimented with various options of increasing and controlling ESR of MLCCs [9]. *Figure 6* shows the measured impedance profiles of AVX experimental ceramic capacitors with different values of ESR.

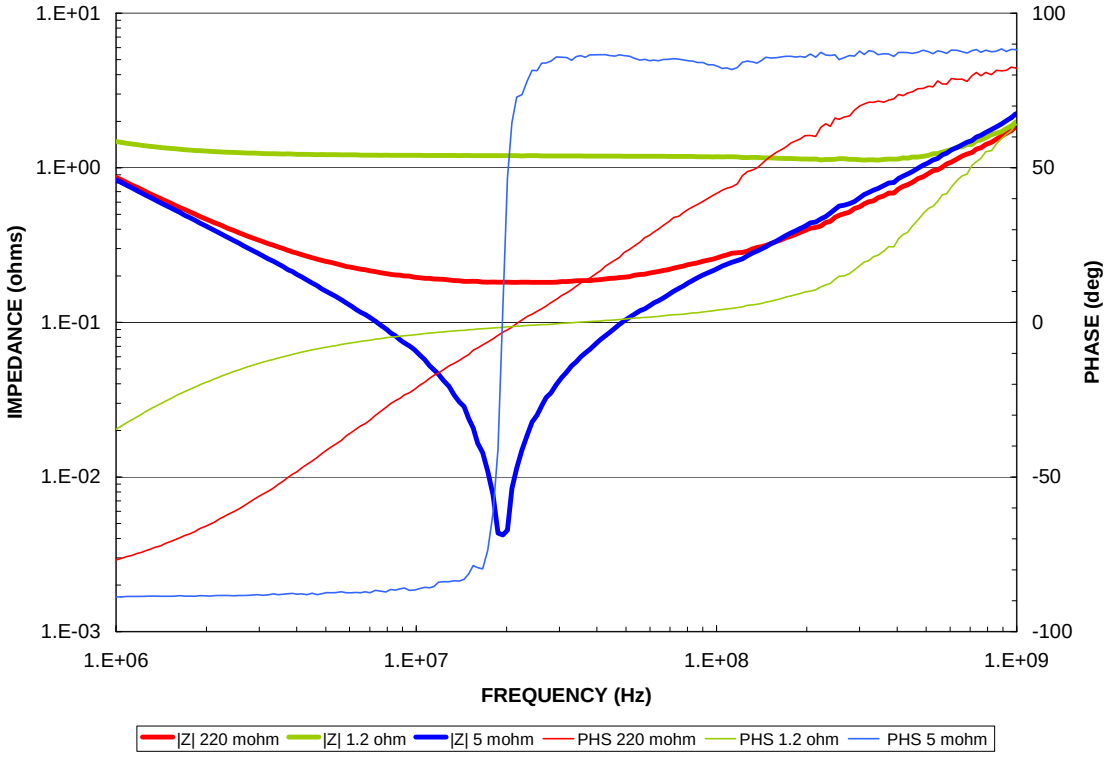

Figure 6: *Manipulation of the parasitic resistive contributions allows deliberate ESR variations of 5-1000 mohm in 0306 0.22µF LICC capacitors. Figure from [9], courtesy of AVX.*

In MLCCs there are various options for increasing ESR. Some of them were overviewed in [10]. *Figure 7* shows a few possible ways to increase ESR by manipulating the connection geometry of MLCC capacitor plates.

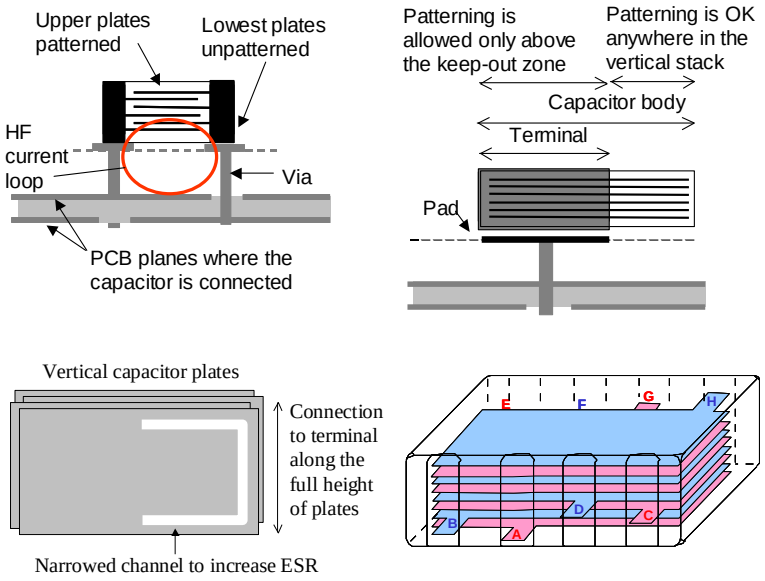

***Figure 7**: Adjusting MLCC ESR by changing the connection geometry of capacitor plates.*

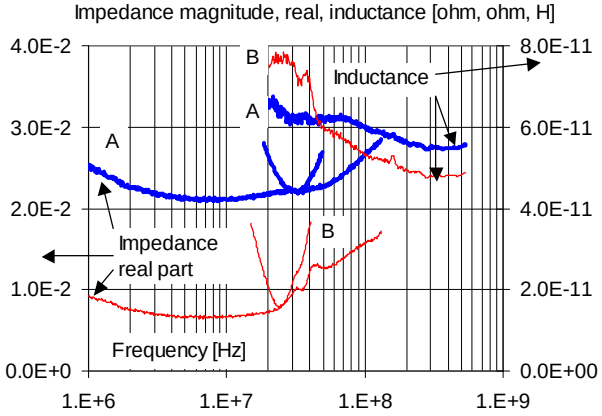

***Figure 8**: ESR increase achieved on a TDK 8-terminal capacitor by implementing the connection scheme from the lower right of Figure 7 [10]. Impedance real part and inductance of multi-terminal capacitors with single-terminal plate connection (traces with label B) versus all-terminal plate connection (traces with label B). For both capacitors, SRFs are indicated by a short V-shape segment of their corresponding impedance magnitude curves.*

Figure 9 is an illustration of changing ESR by adjusting the conductivity of the capacitor plates and/or the conductivity of terminals. The sketches on the left show the concept, the graph on the right is the measured impedance profile of an experimental high-ESR MLCC part from Maruwa [10].

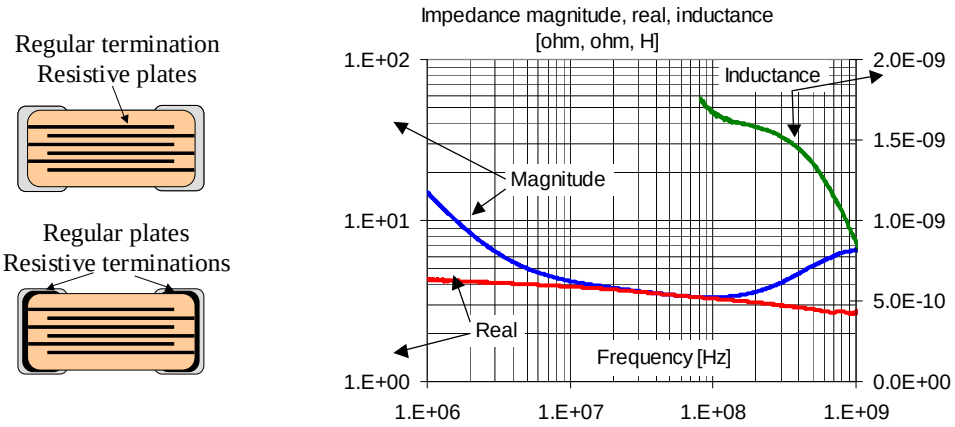

Figure 9: *Left: two construction options to add resistive material to multi-layer capacitors. Right: impedance magnitude, impedance real part and inductance of a 10nF 603-size capacitor with resistive plates, ESR=4 ohms.*

It was also shown that not only the internal connection geometry but also the external part of the current loop around the bypass capacitor has an influence on ESR, which means that ESR of the part is not unique. *Figures 10* and *11* illustrate this with an experiment made with regular low-inductance capacitors [11].

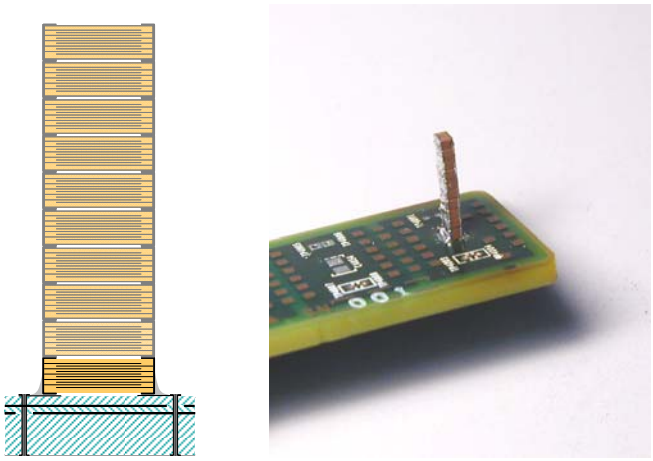

Figure 10: *Side-view sketch and photo of stacked 10uF 0508 reverse-geometry capacitors mounted on a small test fixture. The plane pair was 400mil x 600mil of size. The 2-mil dielectric laminate was 4-mil below the surface. The nine grayed-out capacitors in the sketch indicate that these were optional, and were added one-by-one to the stack.*

Figure 11 shows the impedance real part with 1, 2, 3, 4, 6 and 10 parts stacked. Traces for 5, 7, 8 and 9 stacked parts followed the same trends and those traces were left out to increase the clarity of graphs. First it was verified that as more capacitors were added, the impedance magnitude below SRF moves to the left in accordance with the increased total capacitance. We can also notice on the full-range plot on the left that above 10MHz all traces run on top of each other, which was also true for the impedance

magnitude. The extracted inductance plots confirmed the empirical findings reported earlier that the capacitor height does not degrade (nor does it improve) the inductance associated with the part at high frequencies. Regarding the plots around SRF, one would expect that as we add capacitors on top of the stack, the impedance minimum continues to go down, maybe saturating beyond a certain height (certain number of parts stacked). Note, however, that the measured data shows something strikingly different: as we add parts, the impedance minimum monotonically keeps going **up**. This happens in spite of the fact that we only add parts to the top of the stack, without changing the geometry of the parts already on the fixture. The large dots on the traces on the right indicate the resonance frequencies, where the impedance magnitude had its minimum. The impedance minimum with one part on the fixture is 3.5 milliohms. It goes up to 4.3 milliohms and 5.1 milliohms as soon as we stack a second and third part on top of the first, respectively. With four parts stacked, the impedance minimum is 5.9 milliohms. By the time we have a stack height of six and ten parts, the impedance minimum rises to 7.6 milliohms and 11 milliohms, respectively. This data also suggest that increasing the capacitor height not only increases ESR, but it also creates a wider frequency band over which the higher ESR is maintained with less fluctuation.

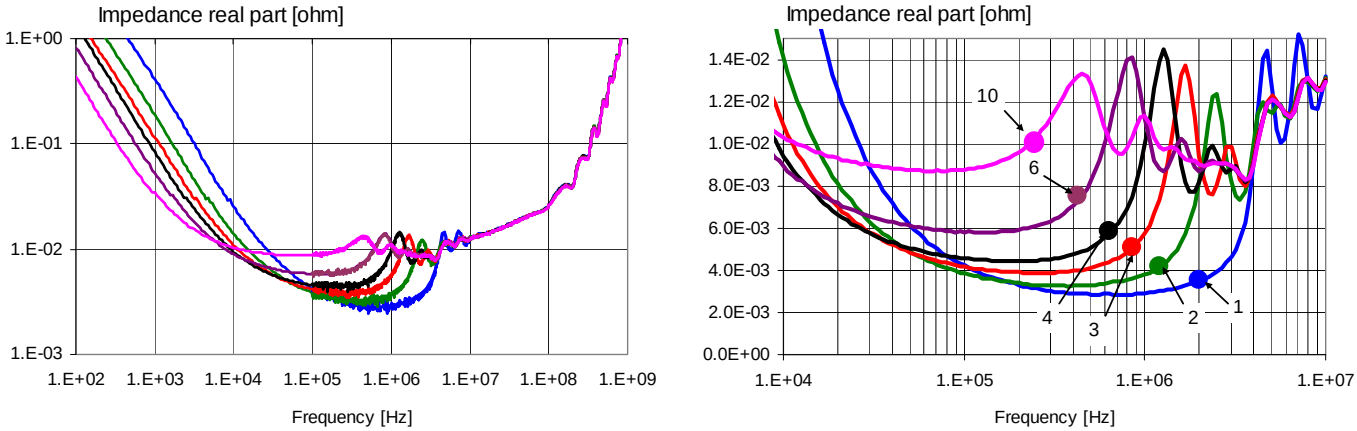

Figure 11: *Impedance real part of 1-10 stacked 10uF 0508 MLCC parts. Full frequency range on the left, zoomed portion around SRF on the right. The dots on each trace show the frequency point, where the impedance-magnitude minimum occurs. The labels show the number of parts stacked.*

Figure 12 shows controlled-ESR bulk capacitor results from [10]. Tantalum and electrolytic capacitors in the multi-hundred uF capacitance range may exhibit ESR in the tens of milliohm range. The large volumetric capacitance allows us to create small-size capacitors, which could have low inductance and low Q. Traditionally, however, even the brick-style tantalum capacitors exhibit large inductance. This is due to the clip-style connections at both terminals in brick packages. Recently multi-anode constructions were introduced, which reduce mostly ESR, but reduce inductance only proportionally to ESR. Face-down constructions [12], on the other hand, can lower both inductance and Q. The construction of such a capacitor from Sanyo and its measured impedance and inductance profiles are shown in *Figure 12*, traces A. As a comparison, conventional-construction capacitor of the same capacitance and case style are shown in traces B. Some of these capacitors are offered in different ESR bins. This means each part has to be tested for ESR, and this raises the possibility of obtaining these capacitors with a known and guaranteed range of ESR.

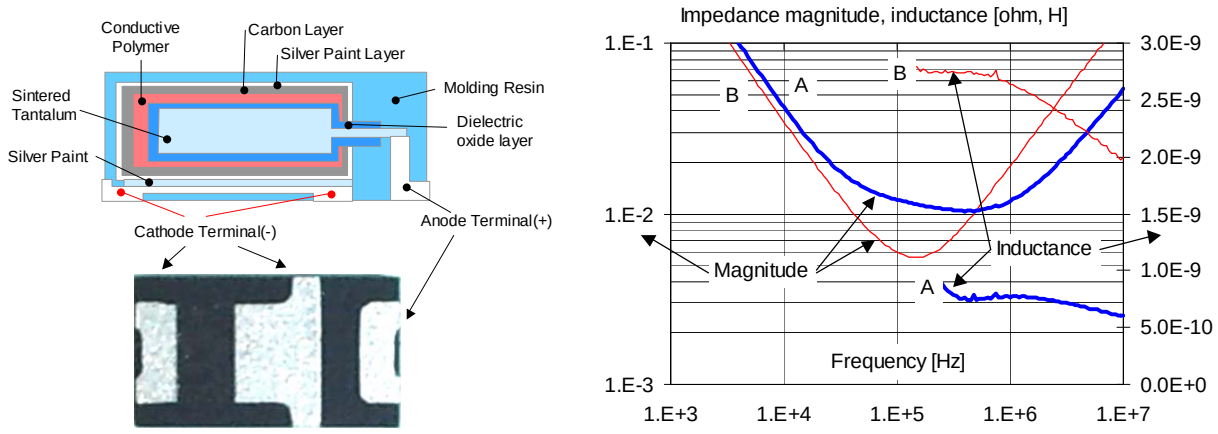

Figure 12: *Left: construction of face-down capacitor in a 7343-size case. Right: impedance magnitude and inductance versus frequency measured on two 470uF D-size capacitors. Traces A: face-down construction from Sanyo, Traces B: conventional construction from vendor B.*

Controlled-ESR bulk capacitors can achieve fairly tight ESR regulations through individually measuring ESR of parts and binning them. Since each part has to be measured for ESR even if only the maximum ESR is guaranteed, the binning process invokes little extra cost. *Figure 13* shows measured results on three-terminal face-down tantalum capacitors from Kemet [13]. The left graph shows the impedance magnitude and phase of one of the samples. The plot on the right compares the impedance real part at 100 kHz from ten samples.

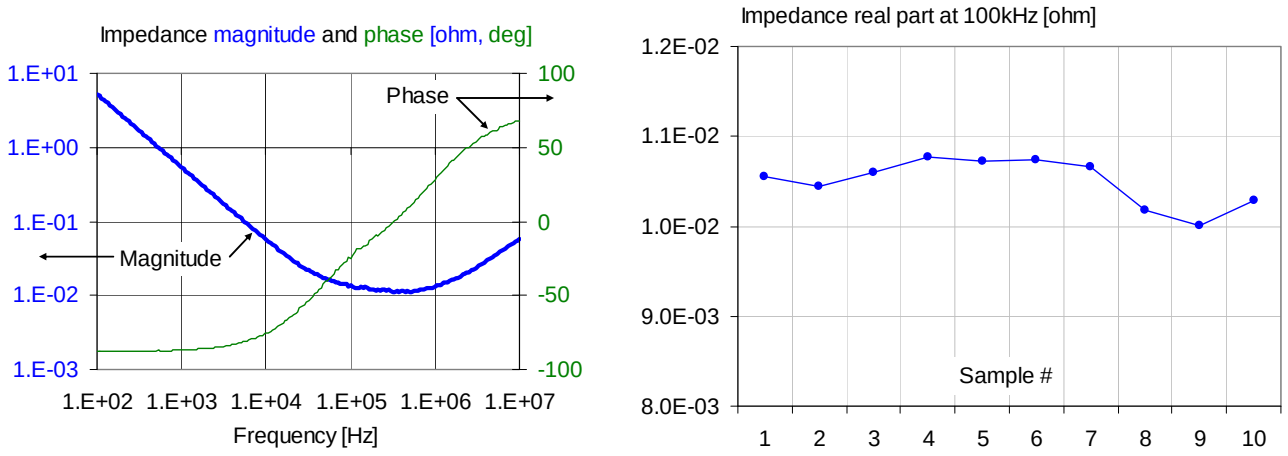

Figure 13*: Performance plots of Kemet T528 capacitors. Impedance magnitude and phase on the left, sample-to-sample variation of impedance real part across ten samples on the right.*

Conclusions

After several years of R&D work at major capacitor manufacturers, controlled-ESR capacitors with guaranteed and user-selectable ESR start to appear. The paper showed illustrations of some of the techniques available for ESR control, together with measured data on engineering sample parts and parts in volume production.

References

[1] Istvan Novak, “Comparison of Power Distribution Network Design Methods: Bypass Capacitor Selection Based on Time Domain and Frequency Domain Performances,” TF-MP3 at DesignCon 2006, February 6-9, 2006, Santa Clara, CA

[2] Larry D. Smith, et-al, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Tr. AdvP, Vol. 22, No. 3, August 1999, pp284-291

[3] “Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination,” IEEE Transactions of CPMT, ITAPFZ, Vol.22, No.3, August 1999, pp. 274-283.

[4] Istvan Novak, Leesa M. Noujeim, Valerie St. Cyr, Nick Biunno, Atul Patel, George Korony, Andy Ritter, "Distributed Matched Bypassing for Board-Level Power Distribution Networks," IEEE Transactions on Advanced Packaging, Vol. 25, No.2, May 2002, pp.230-243

[5] TecForum TF9: Thin and Very Thin Laminates for Power Distribution Applications: What Is New in 2004?; Proceedings of DesignCon 2004, February 2, 2004, Santa Clara, CA

[6] Alex Waizman, Chee-Yee Chung, “Extended Adaptive Voltage Positioning (EAVP),” Proc. of EPEP conference, October 23-25, 2000, Scottsdale, AZ

[7] Drabkin, et al, “Aperiodic Resonant Excitation of Microprocessor power Distribution Systems and the Reverse Pulse Technique,” Proceedings of EPEP 2002, p. 175

[8] Valerie St. Cyr, Istvan Novak, Nick Biunno, Jim Howard, “ARIES: Using Annular-Ring Embedded Resistors to Set Capacitor ESR in Power Distribution Networks,” EPEP2001, October 29 – 31, 2001, Boston, MA

[9] George Korony, Andrew Ritter, Carlos Gonzalez-Titman, Joseph Hock, John Galvagni, Robert Heistand II, “Controlling Capacitor Parasitics for High Frequency Decoupling” Proceedings of IMAPS2001, 2001 October 9-11, 2001, Baltimore, Maryland

[10] Istvan Novak, Jason. R. Miller, Sreemala Pannala, "Overview of Some Options to Create Low-Q Controlled-ESR Bypass Capacitors," Proceedings of EPEP2004, Portland, OR, October 25-27, 2004

[11] Istvan Novak, “A Black-Box Frequency Dependent Model of Capacitors for Frequency Domain Simulations,” Proceedings of DesignCon East 2005, September 19-21, 2005, Worcester, MA

[12] Michihiro Shirashige, Keiji Oka, Kazuto Okada, “New Structure 1608 Size Chip Tantalum Capacitor - 6.3WV 1uF -with Face-down Terminals for Fillet-less Surface Mounting,” Proc ECTC2001, Orlando, FL., May 2001

[13] Kemet T528 family, http://www.kemet.com