DesignCon 2012

Panel discussion:

What is New in DC-DC Converters?

Panelists:

V. Joseph Thottuvelil	GE Energy
Chris Young	Intersil Zilker Labs
Steve Weir	IPBLOX
Istvan Novak*	Oracle

* panel organizer and moderator

Abstract:

The panelists plan to cover and discuss topics including but not necessarily limited to: trends, current state of the art in power density, selection criteria among packaging options (open frame, embedded, modules, semi-modules), state of the art and forecast of efficiency, power density, switching frequency, loop bandwidth, output noise, the signature and bandwidth of output periodic and random noise, set-point accuracy, trends of number of phases, new features of digital telemetry, interaction of DC-DC converter performance with the power distribution environment, and last but not least, new options and features of design tools for users.

Panelist biographies:

Joseph Thottuvelil is the Director, Applications Engineering & Technical Marketing at GE Energy Power Electronics. He has over thirty years of experience in power electronics, in areas such as modeling and simulation of converters and power systems, development of control algorithms for DC battery plant applications and transient response improvement in dc-dc converters. He holds 28 US Patents and has published many papers and technical articles.

Chris Young is a Senior Manager of Digital Power Technology at Intersil responsible for leading digital power development within Intersil. Chris was the Chief Technical Officer of Zilker Labs which was acquired by Intersil in 2008. Prior to Zilker Labs, he was one of the founders and vice president of technology at ColdWatt, Inc. Prior to that, he held technical and engineering management positions at leading companies including Dell, Astec Power, Lucent/Bell Labs and Unison Industries. He has authored numerous publications and patents in the areas of pulsed power, power control and conversion, and stability analysis. Chris holds a Bachelor's degree in Physics from the University of Texas and a Master's degree in Electrical Engineering from Texas Tech University.

Steve Weir, CTO IPBlox, LLC Steve is an independent consultant with over 20 years industry experience and a broad range of expertise. Steve holds numerous patents, has authored more than a dozen papers on power integrity, and contributes regularly to the SI-List signal integrity reflector. Recent papers and presentations: PDN Application of Ferrite Beads, DesignCon 2011, 11-TA3 Winner best paper. Clock and Power for Low Jitter HSSI, 8/09, FPGA Camp Sunnyvale. PCB Power Delivery Optimizations for the Cost Driven Era, 2/09, DesignCon 2009. GSM Buzz of Death Causes and Remedial Measures, 1/09, SVCEMC

Istvan Novak is a Senior Principle Engineer at Oracle, Inc. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for Sun servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF and analog circuits, and system design. He is a Fellow of IEEE for his contributions to the fields of signal-integrity, RF measurements, and simulation methodologies.

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POLs and the Load

Basic Performance Needs

V. Joseph Thottuvelil, Director – Apps. Eng.
GE Energy, Power Electronics

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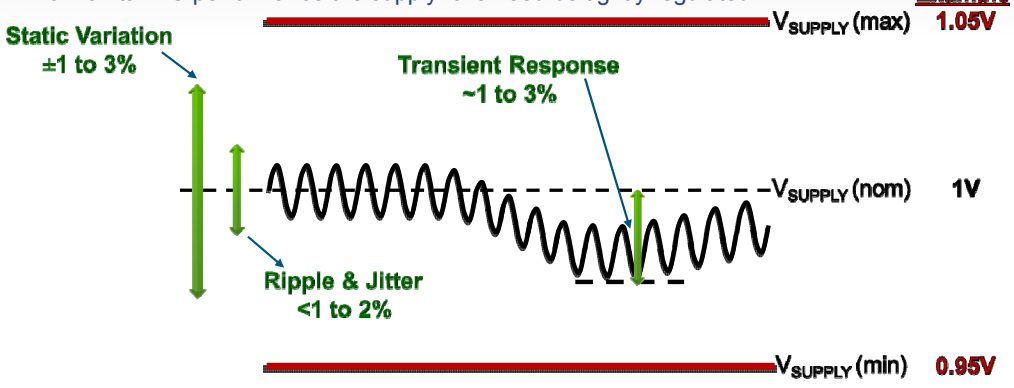
Voltage Budget Problem

- To maintain IC performance the supply rails need be tightly regulated



- Limiting Transient Deviation can be a tough problem. E.g. for a 33W IC
  - At 3.3V, 50% load transient is 5A and 2% of V_{SUPPLY} is 66mV
  - At 1V, 50% load transient is 16.5A and 2% of V_{SUPPLY} is 20mV
- 3.3X load current transient, 0.3X allowed voltage deviation – much harder problem

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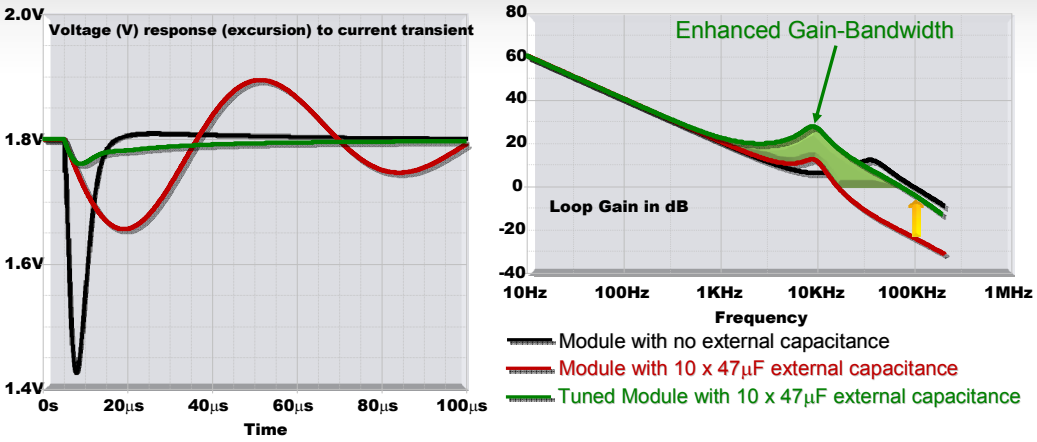
Improved Transient Response with Loop Tuning



- Adding capacitance has mixed effects – basically a brute force solution
- Pre-Tuning (e.g. Tunable Loop) or Auto-tuning change the loop to match the added external capacitance

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Board Designers Still Need to:

- Be able to predict transient response to make sure it is less than target
- Need to
  - Know the worst-case transient (load current) deviation
  - Maximum allowed supply voltage deviation
  - Be able to simulate transient response using accurate models for POLs and capacitors

- Digital Control Loops
  - Offer auto-tuning that help simplify the stability problem but transient deviation problem remains
  - Nonlinear control helps with improved (faster, smaller deviation) transient response but still need to be able to predict response
  - Generally more expensive and harder to use/optimize

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Other POL Design Considerations

- Size – smaller means more PWB area available for payload circuits
- Thermal Derating – better derating implies more robust design with better reliability
- Ease of use – generally modules offer easier design-in with fewer external parts and less work by the board designer
- Efficiency – getting more attention these days because of energy efficiency concerns – POLs efficiency has a significant multiplicative effect because they are downstream in the power processing chain
- Risk – modules offer lower design risk because more of the design is done

- And of course cost!

What is New in DC-DC Converters

A Silicon Supplier's Perspective

Chris Young, Sr. Manager, Digital Power Technology
Intersil, Corp

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- **Positive Trends Since 2007**
  - Technology has progressed
    - Digital Power is becoming more widely available and accepted
      - Expected to be as much as 30% of controller market in 2015
    - Smart Power is available
      - Automatic compensation
      - Auto-calibration
      - Self Optimizing
  - Better components are available
    - Better FETs
    - Better Magnetics
  - IP issues are getting resolved
    - Digital Power
    - IBC

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- **Negative Trends Since 2007**
  - Price pressures continue – it is the nature of a free market system (commoditization)
    - 2002 DSP Solutions = $ 5
    - 2007 State Machine Solutions = $ 2
    - 2011 Digital Wrapper Solutions < $ 1
  - Cost of Support has increased
    - Fewer power supply engineers
    - Stiffer competition
    - Faster time to market

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- **Today's Challenges**
  - Diverse customer base
    - No one part can be used everywhere
    - Experienced power supply engineers want different experience than non-power supply engineers
      - Modules vs Embedded solutions
  - Better, Faster, Cheaper…all three
    - Telemetry: 10%>5%>3%>?
    - Efficiency: 90%>92%>94%>?
    - Switching Frequency: 300kHz>600kHz>800kHz>1MHz>?
  - What is the next IP 'gotcha'?
  - Fab or Fab-less?

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What is New in DC-DC Converters

Trends in ICs and Power Switches

Steve Weir
CTO, IPBLOX, LLC

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Available Frequencies Are Moving Up

- Enables Smaller Energy Storage Networks
- Enabled by improved switching transistors and faster control silicon
  - Lower gate charge, low R_{DS} MOSFETs
  - mOhm FETs now available with Qg << 100nC
  - Low inductance packages
    - Some as low as 100pH

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Frequency Disparities

- Integrated hard-switching ICs and controllers widely available 2MHz and higher for many Ampere rails, 6MHz for low power rails
- Low cost power ferrite losses still degrade rapidly above 500kHz
  - Efficiency sweet-spot for hard-switching devices still in the 200kHz – 500kHz
    - Storage W/cc linear to frequency, losses square w/ frequency
- For discrete transistors package and PCB interconnect inductance is still a big issue
- Heat removal always a challenge
- Control loop improvements are hit and miss.
  - Some devices showing very good improvement in transient response vs. output filter size

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Market Trends

- More integrated power modules
  - “Lego (bricks) shall inherit the (DC-DC) earth.”
  - High volume, custom tooled packaging
    - Custom silicon
    - Optimized magnetics
    - Superior thermal relief
    - Superior interconnect parasitics
  - Difficult for all but high volume mfgs to affordably tool competitive packaging
    - Very difficult on short product development cycles

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Market Trends Efficiency

- Practical efficiencies in the high 80's% / low 90's%, hard-switching. Up to 98% soft-switching.
  - Driven by balance of perceived market balance of: cost, size, tolerable performance
  - Data sheet bullets of mid 90's% are often at reduced frequency and/or power levels
- Compelling real-estate & performance of integrated offerings will make it increasingly difficult for discrete solutions to compete

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Challenges / Opportunities

- Leverage Moore's Law
  - More cheap transistors affords unique control schemes:
    - Clever partitioning of digital / analog will further speed integrated module adoption over discrete designs
      - Flexible frequency response
      - Flexible efficiency vs. power handling
  - Good use of transistors will reduce design uncertainty

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Summary

- Physical limits of thermal and electrical performance are driving to integrated package solutions.
- For the time being, this presents heart-burn for those who want characteristics not available in standard offering.
- Postulate: The integrated module industry is at about the same point that the logic industry was with the introduction of GALs. Massive growth in control transistor count could soon take the DC-DC industry from a metaphoric PLD phase to the FPGA phase.

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An OEM's Perspective

Istvan Novak, Senior Principle Engineer
Oracle-America

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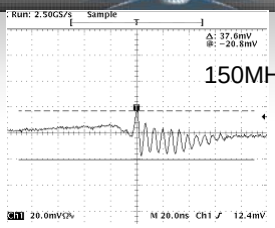
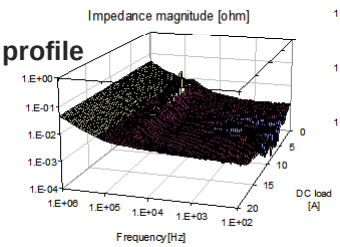
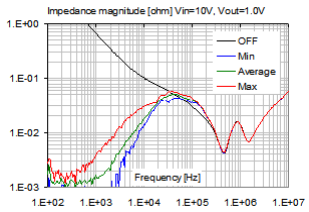
Concerns listed in 2007:

- **High-frequency ringing**
- **Low loop bandwidth**
- **Phase margin vs impedance peaking**
- **Unstable impedance profile**
- **Not enough models**



150MHz ringing





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What Happened Since Then

- **The good news:**
  - More simulation models and design help are available
- **The bad news:**
  - Several concerns are still unresolved. New concerns emerged

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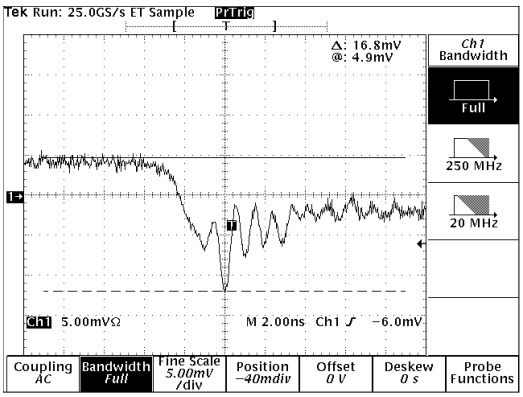
Concerns five years later:

- **Ringing frequency got higher**

~1GHz ringing



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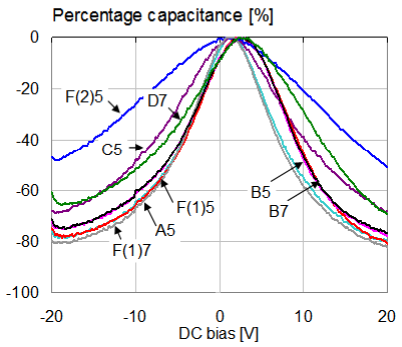
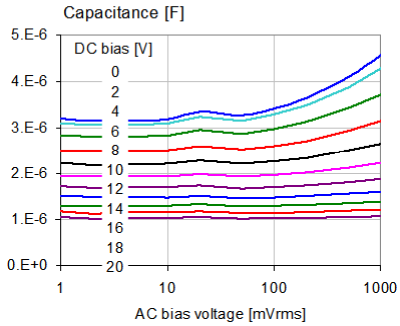
Concerns five years later:

- DC and AC bias sensitivity of MLCC capacitors





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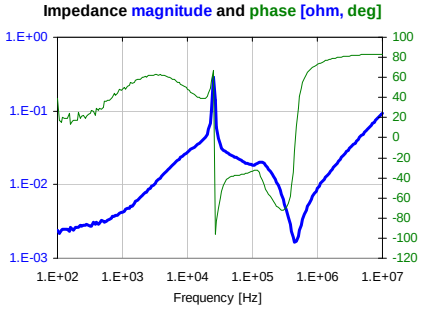
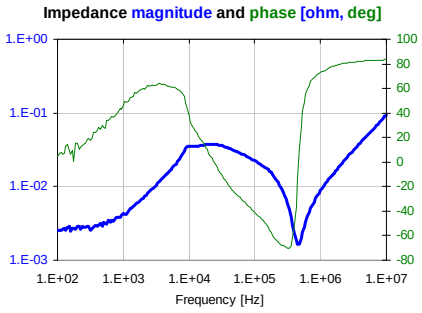
Concerns five years later:

- Effect of source impedance on output impedance





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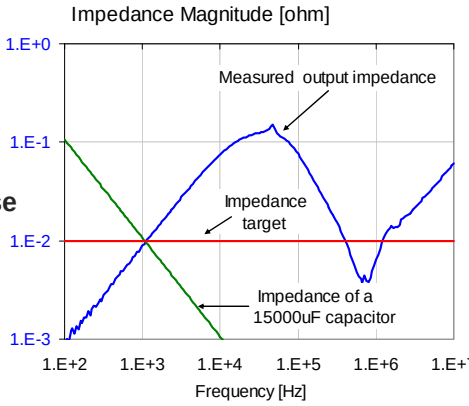
Concerns five years later:

- **In high-end applications impedance magnitude and/or loop bandwidth is still a concern**
- **Still no concise worst-case system-noise design procedure with nonlinear loops**



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References:

- **Emerging Challenges of DC-DC Converters, DesignCon2007, Santa Clara, CA, January 29-31, 2007**
- **DC and AC Bias Dependence of Capacitors Including Temperature Dependence, DesignCon East 2011, Boston, MA, September 27, 2011**
- **Dynamic Characterization of DC-DC Converters from a System's Perspective, DesignCon 2012, January 28 – February 1, Santa Clara, CA**