PCB007 QuietPower column

Prophecy from the past

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Early last year I wrote a column about the first DesignCon (or Hewlett Packard High Speed Digital Symposium as it was called that time) I attended in 1993 [1]. As engineers and organizers prepare for DesignCon 2015, I thought I would give a brief reflection on DesignCon twenty years earlier, or Design SuperCon 95 as it was called back then.

DesignCon in these years is a major engineering conference in Santa Clara, California, late January or early February each year, attracting many signal and power integrity practitioners from around the globe [2]. In the early 1990s it started out as a marketing event for Hewlett Packard and this might have contributed to the lack of archived conference proceedings identified by ISBN numbers. Before year 2000 the conference proceedings were handed out to attendees in hard-copy format and very few libraries collected or kept these booklets. Since I attended the event in 1993, 1995 and then 1999 onwards, I happen to have those proceedings, but came up empty when I was trying to locate the proceedings for the missing few years. Though technology progressed tremendously over the past twenty years, I still find it useful and enlightening to browse the old proceedings to see how it can help us to forecast and predict what lies ahead. Since I had no luck locating these old proceedings, I thought that some people will find it useful if I scan and make my copies from 1993 and 1995 available. Over the past two years I have scanned both proceedings little-by-little, and now they are available at [3] and [4]. Disclaimer: these are pdf files of scanned images of the individual pages, and not having done character recognition on the files, unfortunately these are not search-able. And be patient when you download them; these are very big files.

My memories about the 1993 event were summarized in [1]. In this column I will focus on the 1995 conference. You can find the cover page of the conference in *Figure 1*.

This was the first year that I presented at this conference series; in earlier years I attended and did publications mostly at IEEE EMC Symposia and IEEE Instrumentation and Measurement conferences. Being used to the technical scrutiny and process of paper selection of IEEE events, the process at this Hewlett Packard conference was surprisingly different. I do not recall exactly how I got the call for papers; in those years the public web was in its infancy, and though e-mail already existed, still a lot of communications happened through snail mail. It is highly likely that the call for paper was obtained through the local Hewlett Packard representative. The paper selection process had several steps, starting with the proposal. Once the proposal got accepted, there were several additional filters: there was an early deadline to send in preliminary slides, and another deadline later for final slides with the proceedings text. Finally in late 1994 we had to submit a video recording of the planned presentation. My impression was that the

scrutiny was more towards the marketing quality of the papers and presentations. In those days this conference was a marketing event for Hewlett Packard (and for the presenters). As you can see in the proceedings, the last slides in each presentation had recommended resources, listing (among others) Hewlett Packard HW, SW or services used in the preparation of the paper.

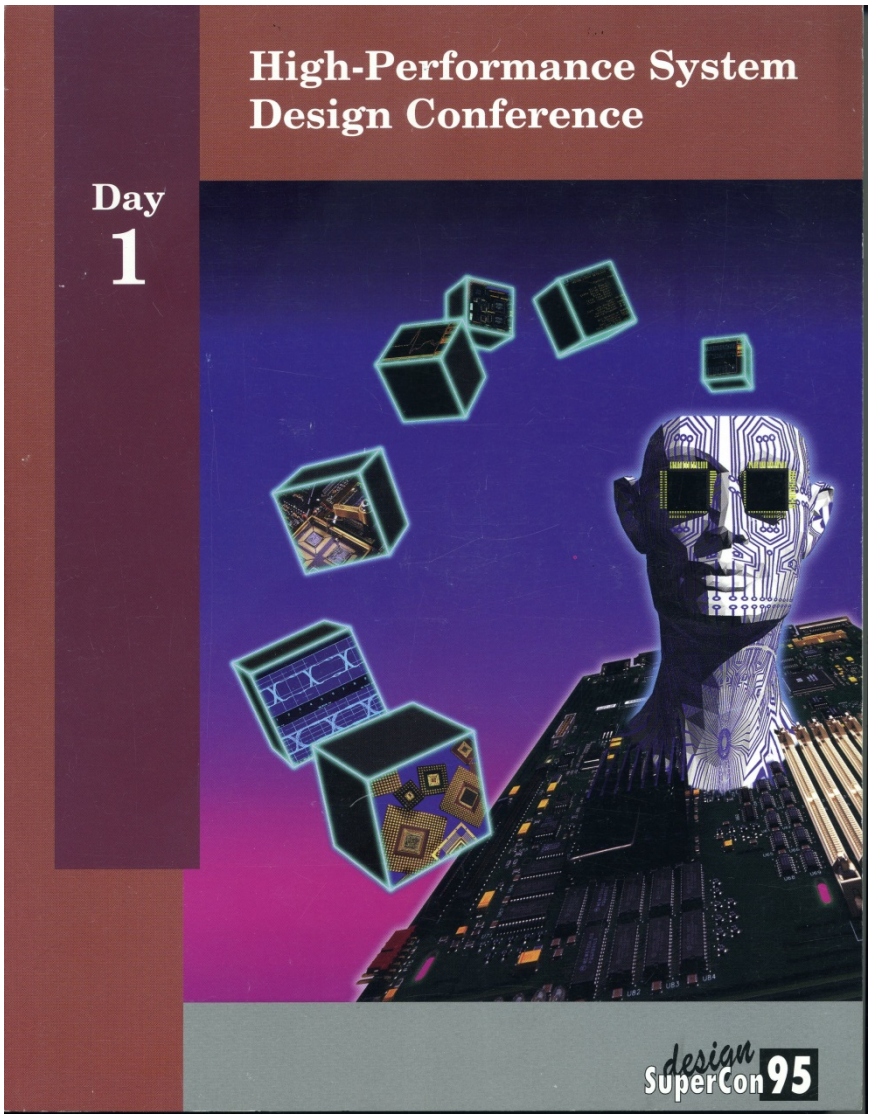
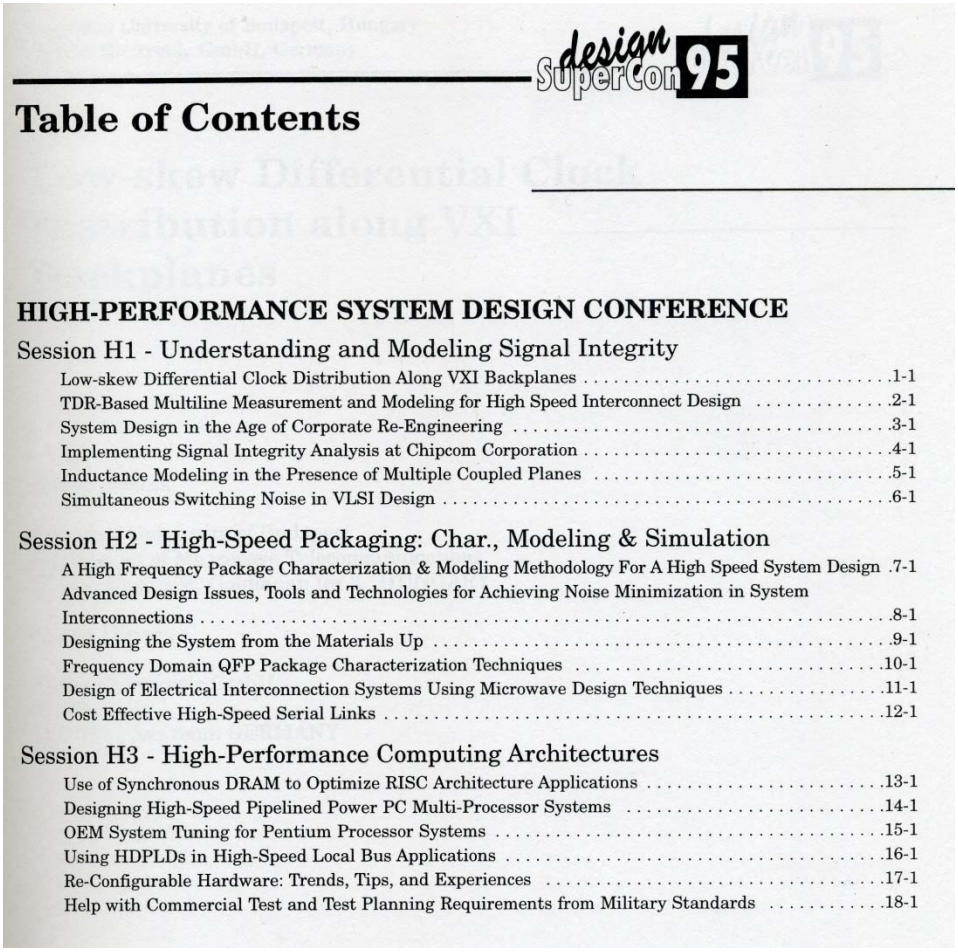


Figure 1: *Front page of the conference proceedings of Design SuperCon 95 for Day 1, sponsored by Hewlett Packard. The conference was held in early February in 1995, in Santa Clara, CA.*

Figure 2 shows the table of contents of the first day. The three parallel sessions covered signal integrity, modeling and architecture. Each paper presentation was an hour-long session, and the day concluded with demonstrations by the presenters on the exhibition floor.



design SuperCon 95

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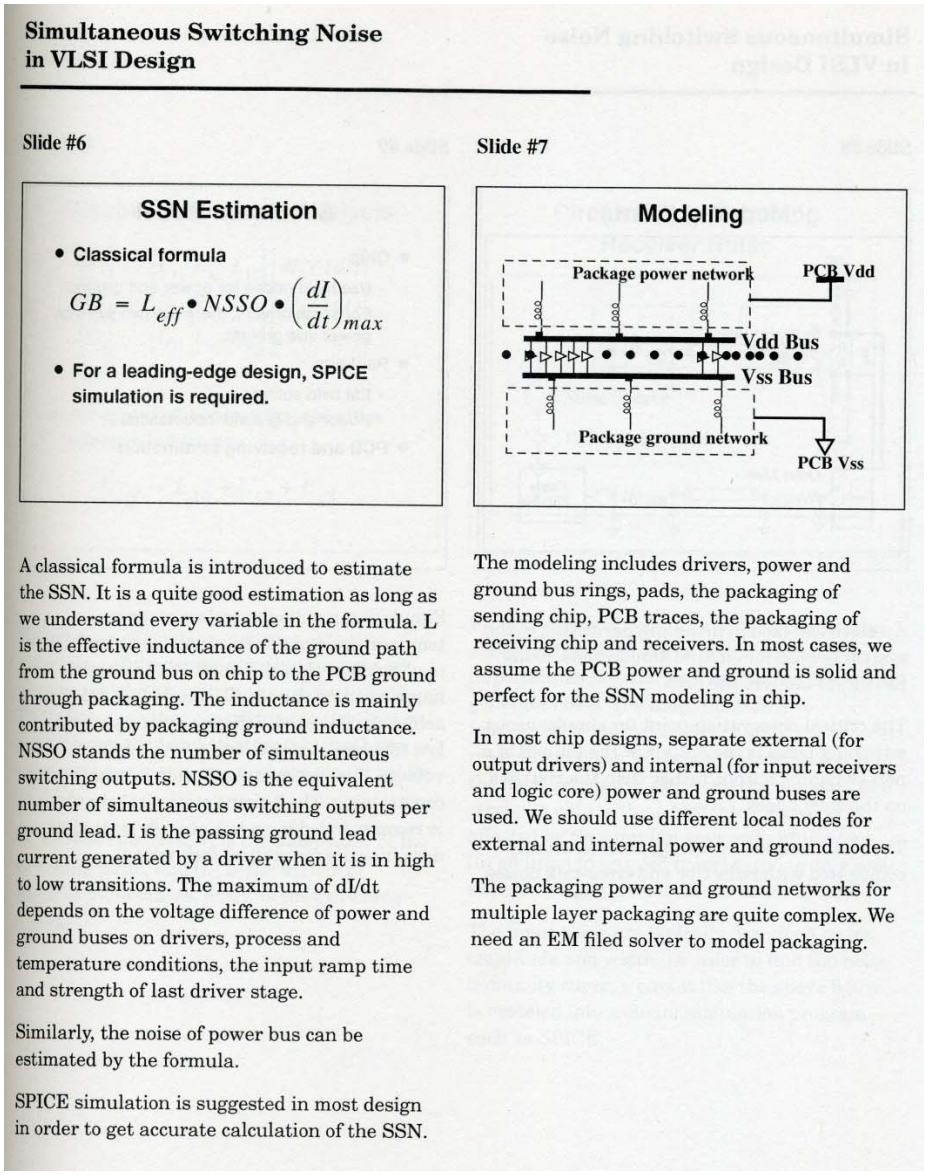
HIGH-PERFORMANCE SYSTEM DESIGN CONFERENCE

Figure 2: *Table of contents of the first day at Design SuperCon 95.*

As opposed to the conference in 1993, where in addition to the many signal integrity topics there were a few papers touching upon power integrity, presentations in 1995 were almost entirely about signal integrity.

The pressing challenges of the day were ‘static’ skew in clock distribution, simulation and modeling of trace impedance and simultaneous switching noise. When we put these topics into perspective, all of these three areas are still very important and continue to pose new challenges to the design communities. Skew twenty years ago was measured in nanoseconds and the biggest contributors were deterministic skew from electrical daisy-chain loading, routing on the board and routing on the package. Timing budget was loose enough that the miniscule details, like glass-weave effect did not matter back then. With the widespread use of gigabit serial interconnects, skew today is equally important but now we measure skew in picoseconds and more and more skew comes from random variables where the best we can do is to understand and characterize the statistics.
The characterization of trace impedance in 1995 was mostly about educating the audience about the TDR basics. Though it was already empirically observed and known that

losses create an upward tilt on the TDR response line even for uniform traces, how it actually relates to the losses and potential non-uniform behavior of interconnects, has only been analyzed in recent years. Simultaneous switching noise was a hot topic twenty years ago because the silicon industry and users alike just came to terms with the inevitable fact that this kind of noise is here with us to stay long term. Those basics shown in *Figure 3* are still valid today.



Simultaneous Switching Noise in VLSI Design

Slide #6

SSN Estimation

- Classical formula

$$GB = L_{eff} \bullet NSSO \bullet \left(\frac{dI}{dt}\right)_{max}$$

- For a leading-edge design, SPICE simulation is required.

A classical formula is introduced to estimate the SSN. It is a quite good estimation as long as we understand every variable in the formula. L is the effective inductance of the ground path from the ground bus on chip to the PCB ground through packaging. The inductance is mainly contributed by packaging ground inductance. NSSO stands the number of simultaneous switching outputs. NSSO is the equivalent number of simultaneous switching outputs per ground lead. I is the passing ground lead current generated by a driver when it is in high to low transitions. The maximum of dI/dt depends on the voltage difference of power and ground buses on drivers, process and temperature conditions, the input ramp time and strength of last driver stage.

Similarly, the noise of power bus can be estimated by the formula.

SPICE simulation is suggested in most design in order to get accurate calculation of the SSN.

Slide #7

Modeling

The modeling includes drivers, power and ground bus rings, pads, the packaging of sending chip, PCB traces, the packaging of receiving chip and receivers. In most cases, we assume the PCB power and ground is solid and perfect for the SSN modeling in chip.

In most chip designs, separate external (for output drivers) and internal (for input receivers and logic core) power and ground buses are used. We should use different local nodes for external and internal power and ground nodes.

The packaging power and ground networks for multiple layer packaging are quite complex. We need an EM filed solver to model packaging.

Figure 3: *Page 5 of Liren Chen's paper showing the simultaneous switching noise estimation and circuit model.*

Based on its title, probably the fifth paper in the first session "Inductance Modeling in the Presence of Multiple Coupled Planes" might have had something to do with power distribution. Unfortunately this paper was not included in the printed conference

proceedings and I must have lost my hard copy that was separately distributed during the presentation.

I have to admit that I hardly recall the specifics of any of these presentations, except the keynote speech, which I found intriguing back then and feel that its predictions were quite interesting. If my memory serves me well, the keynote speech was about the future of computer hardware and the key message was summarized in a very simple statement: "Computers in the future will look like hairy, steaming golf balls. They will be hairy because of the many peripheral cables. They will be steaming because of the large dissipation. And they will be the size of a golf ball." When we look at computers today, they are not the size of a golf ball, though whatever was a computer in 1995, using today's technology, it could easily fit in a golf ball. Network switches with all the cables certainly may look hairy, but the generic computers got a good shave from the various serial peripheral connection standards. What became painfully true is that computers today are steaming hot because of the power density we pack into them.

I am looking forward to DesignCon 2015 to hear the predictions how computers will look like in 2035.

If you are interested in the recent activities around DesignCon, you can follow the DesignCon Community website at [5].

References:

[1] http://www.electrical-integrity.com/Quietpower_files/Quietpower-25.pdf
[2] www.designcon.com
[3] http://www.electrical-integrity.com/Paper_download_files/HewlettPackard_DesignCon_1993_proceedings.pdf
[4] http://www.electrical-integrity.com/Paper_download_files/DesignSuperCon_1995.pdf
[5] http://www.edn.com/designcon