DesignCon 2016

Needs and Capabilities for Modeling of Capacitor Derating

Panel discussion

Brad Brim, Cadence Design Systems
Istvan Novak, Oracle
Tim Michalka, Qualcomm Technologies
Wilmer Companioni, KEMET Electronics
Shoji Tsubota, Murata Manufacturing
Sam Chitwood, Cadence Design Systems

Abstract

Capacitors vary with temperature, bias voltage and age; a phenomenon typically referred to as derating. Libraries of SPICE or S-parameter models are provided by component manufacturers for non-derated components - new capacitors at a specific temperature and bias. Detailed derating data and related methodologies are often considered manufacturer-proprietary. Some manufacturers provide software to generate and display derated models while others specify general derating behavior in data sheets.

OEMs have expressed a desire for more detailed and automated power integrity analyses to consider derating effects. Representatives from component manufacturers, OEMs and EDA will discuss these analysis needs and the electrical models required to support such. Audience participation is strongly encouraged to help judge the breadth of industry need in this area and help influence future contributions.

UBM

Needs and Capabilities for Modeling of Capacitor Derating

Moderator:

Brad Brim	(Cadence)

Participants:

Istvan Novak	(Oracle)
Tim Michalka	(Qualcomm)
Wilmer Companioni	(KEMET)
Shoji Tsubota	(Murata)
Sam Chitwood	(Cadence)

UBM

Needs and Capabilities for Modeling of Capacitor Derating

Brad Brim (Cadence)

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

Moderator

Brad Brim

Product Engineering Architect, Cadence Design Systems
bradb@cadence.com

Brad has been in the EDA industry for more than 25 years. His graduate studies and initial commercial contributions were in the area of electromagnetic simulation and passive component modeling for circuit simulation. Some of the products he has worked on include: Momentum, ADS, HFSS, PowerSI and OptimizePI. His roles have included software development, applications engineering and product marketing. Prior to joining Cadence as product engineer architect he held various roles with HP/Agilent (now Keysight), Ansoft (now Ansys) and Sigrity (now Cadence).

Discussion Topic

- Q2-15
  - OEMs requested EDA company support PDN analysis that includes capacitor derating w.r.t. bias voltage, component temperature, age, etc.
  - Initial discussions among small group, develop consensus vision
- Q3- 15
  - Added component vendor to the discussion
  - Component vendor withdrew from the discussion
- Q4-15
  - Other component vendors joined the discussion
  - Rapid progress to identify existing capabilities and brainstorm potential future directions
- Q1-16
  - Share discussion with and query the high-speed design community

Requirements

1. Include more general effects in PDN analysis
2. Non-disclosure of component vendor-proprietary information
3. Automation
4. Support of preferred analysis tools
5. Generality for future support of other component types and other analyses

Panel Participants

- **Istvan Novak**
  Senior Principal Engineer, Oracle
- **Tim Michalka**
  Sr. Director, Engineering, Qualcomm Technologies, Inc.
- **Wilmer Companioni**
  Technical Marketing Engineer, KEMET Electronics
- **Shoji Tsubota**
  General Manager (Capacitor, Div. 1), Murata Manufacturing
- **Sam Chitwood**
  Product Engineer, Cadence Design Systems

UBM

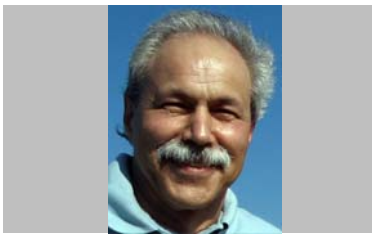
Panel discussion: Needs and Capabilities for Modeling of Capacitor Derating

OEM Wish-list for Models

Istvan Novak, Oracle

SPEAKER

Istvan Novak
Senior Principal Engineer, Oracle
istvan.novak@oracle.com



Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

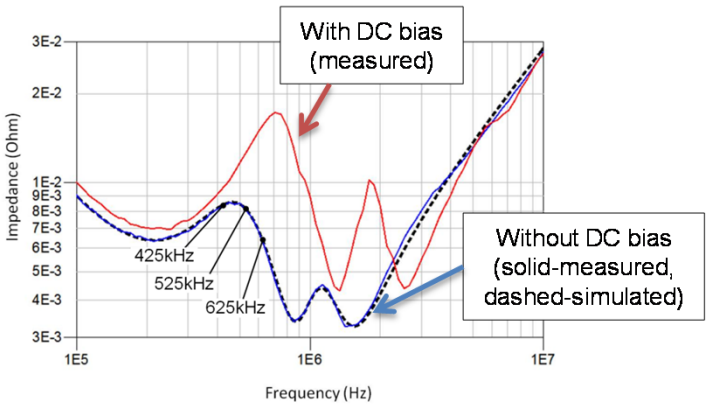
The Problem Statement

- Many passive components show significant parameter variations with
  - DC bias (voltage for capacitors, current for inductors)
  - AC bias
  - Temperature
  - Initial tolerance
  - Time (aging)
  - Pressure (piezo effect)
- Large boards may have the same parts working under different conditions
- Static models are not automatically available for the simulators

Illustrations

- Measured example: different capacitors in parallel with and without DC bias voltage applied
- Worst-case transient noise can significantly increase
- Increased component dissipation due to high Q at resonance may damage parts

Input filter of a DC-DC buck converter



For details, see [1]

What OEMs Need

- Models that 'understand' DC and AC bias, temperature, aging, tolerance
- A single model for each part, covering all parameters
- Models that are valid for arbitrary frequency range
- Model structure that can be used either for PI or SI simulations
- Models that run reasonably fast
- Models available for or compatible with multiple CAD tools
- Models that ensure fast simulations and good convergence

What OEMs Need

- Guaranteed passive models for passive parts (important for both SI and PI)
- Guaranteed causal models (important for SI, less important today for PI)
- Models that can automatically communicate input/output parameters through CAD tools
- CAD tools that 'understand' electrical and thermal parameters for the parts and can pass input/output parameters to/from models without user intervention
- Models for capacitors, inductors, ferrites, EMI filters (passive devices)

Reference

[1] Electrical and Thermal Consequences of Non-Flat Impedance Profiles, DesignCon 2016

Thank you!

QUESTIONS?

Tim Michalka
Sr. Director, Engineering
Qualcomm Technologies, Inc.

Discrete Device Modeling Issues

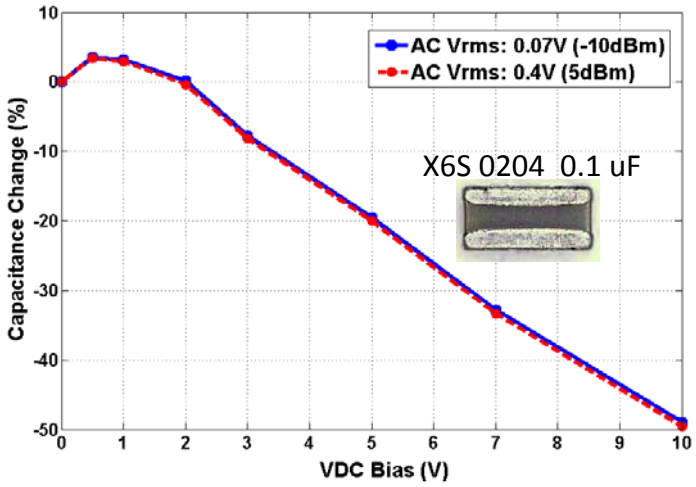
Outline

- My Perspective
- Modeling Challenges
- Multi-Terminal Device Challenges
- Sophistication & Accuracy

My Wants

- Simulation tool independent
- Component vendor independent
- Wideband accuracy, stability, & relevancy
- Process (Tolerance), Voltage, Temperature, Age
- Internally documented
- Passive devices – not just capacitors

DC Bias & AC Signal (VNA)



Yes - capture this type of behavior

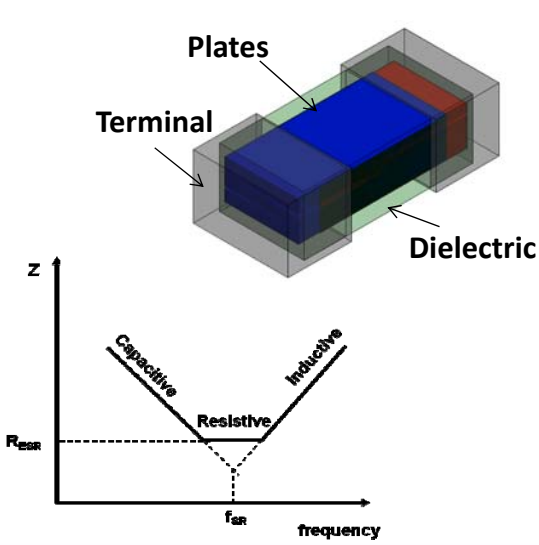
PDN Priorities?

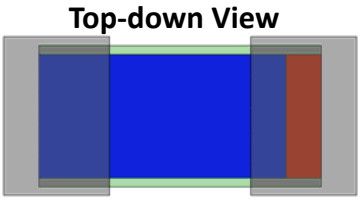
Priority	Buck C_in	Buck C_out	LDO C_out		PDN HF
1st	L	R	C		L
2nd	R	C	R		R
3rd	C	L	L		C

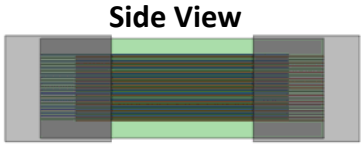
C not always the most important parameter in a capacitor

➔ Capacitance de-rating is an insufficient goal

Discrete Capacitor – or Distributed?



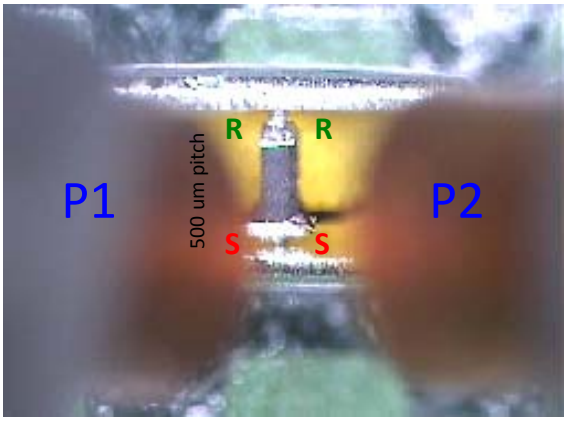




Simple Capacitor model

Measurement *v.* Use

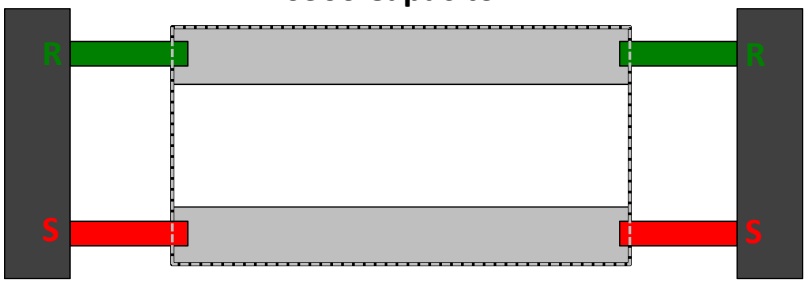
0306 geometry capacitor



Measurement "samples" small region

Direct Measurement Options

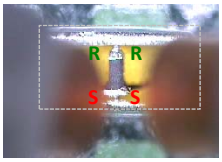
0306 Capacitor



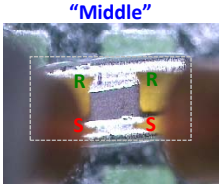
1. **Separation of the probes**
   - Far
   - Middle (1/3 of length)
   - Close (~50 um)
2. **Placement of the two probes**
   - Left
   - Center
   - Right

Example: 1 µF 0306 High ESR C

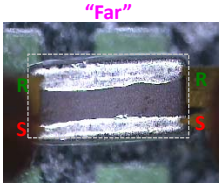
"Close"

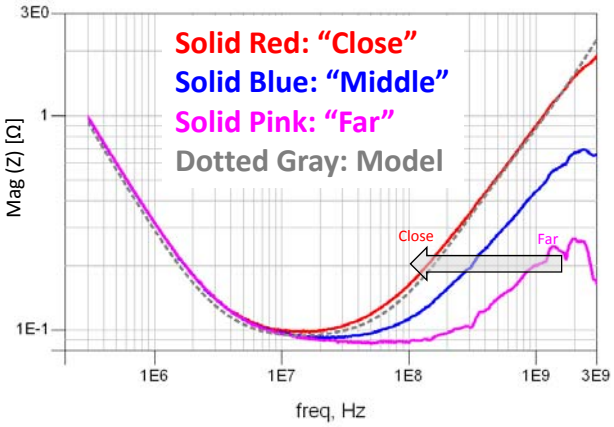


"Middle"



"Far"



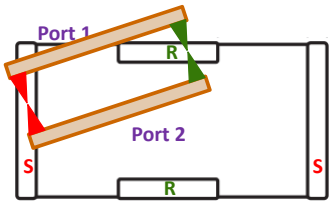


How should we measure and model multi-terminal devices?

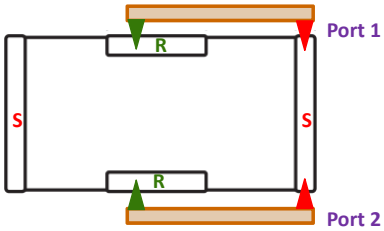
MULTI-TERMINAL CHALLENGES

"3-T" Cap – So Many Choices

2-Pad



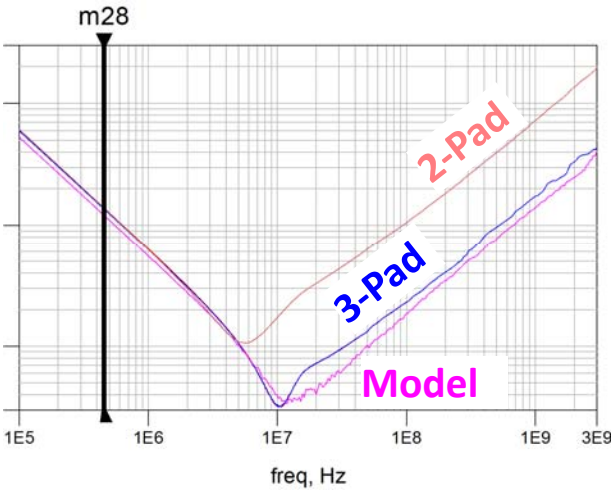
3-Pad



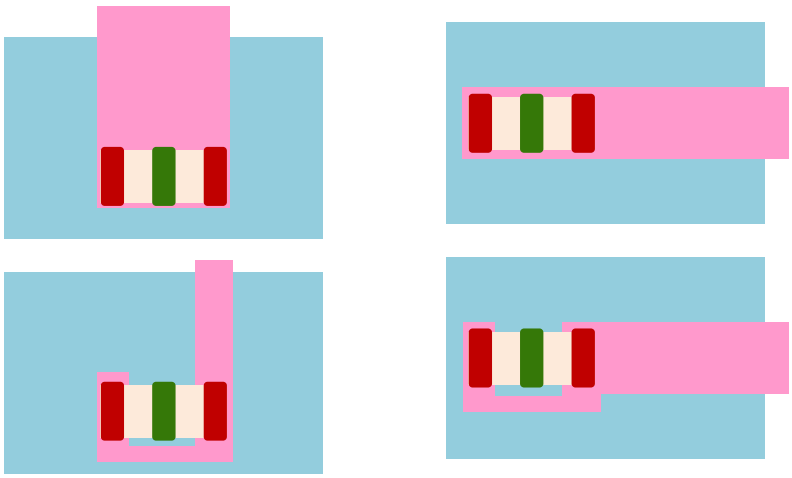
Model

(Model creation details?)

"3-T" Cap "Models"

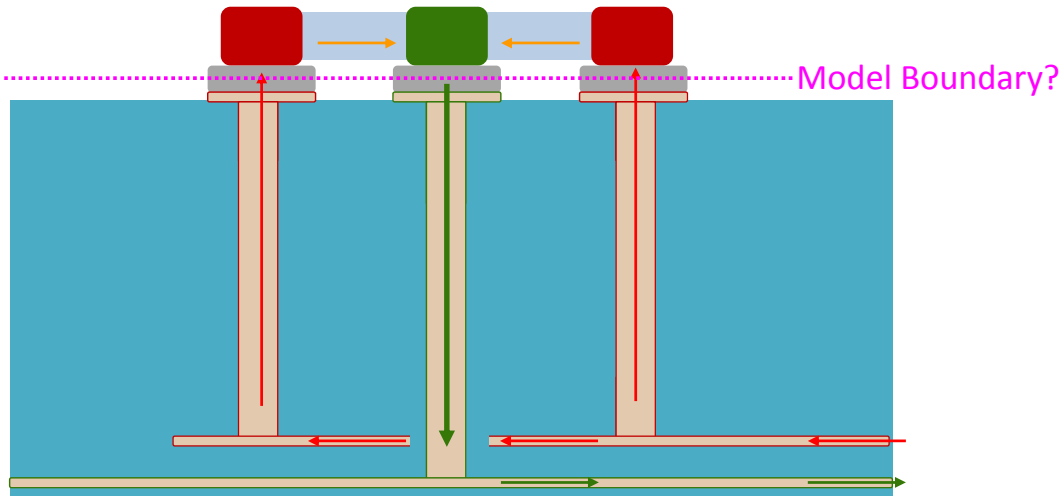


“3-T” Connection – Top Views

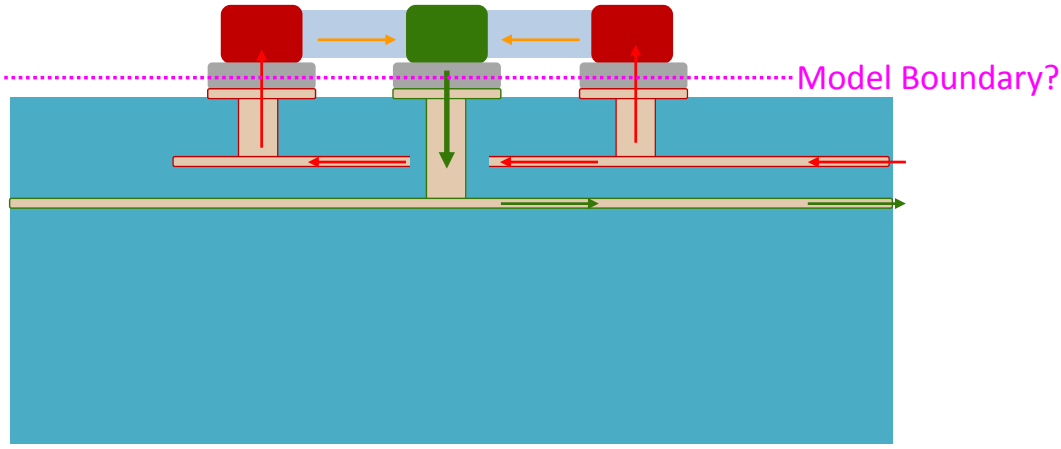


Via & Layer placement are additional variables

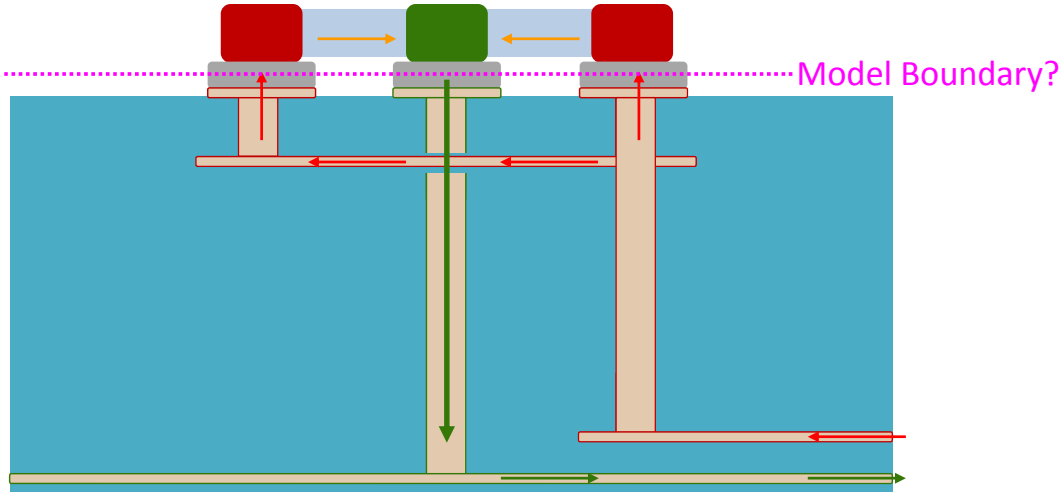
“3-T” End Connection – Long Via



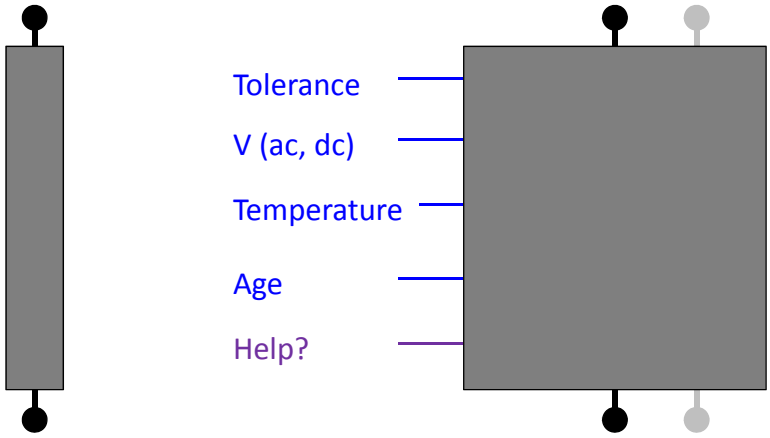
“3-T” End Connection – Short Via



“3-T” End Connection – Mixed Via

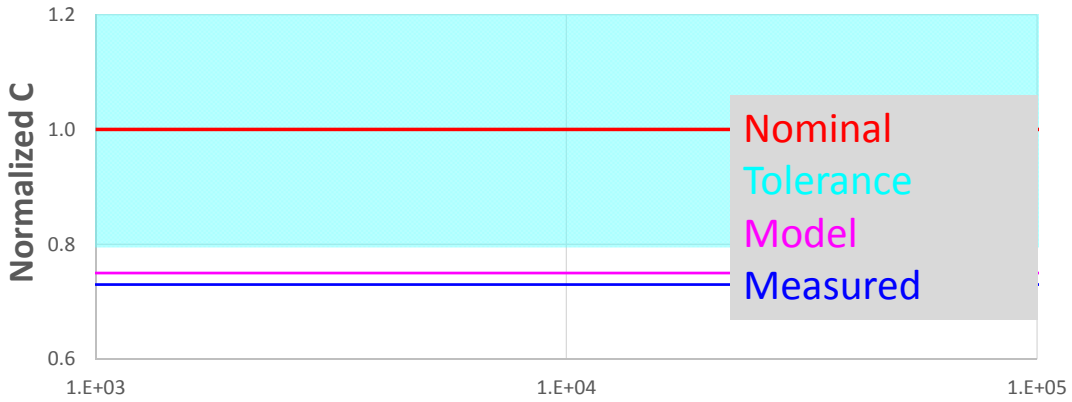


Sophistication & Accuracy



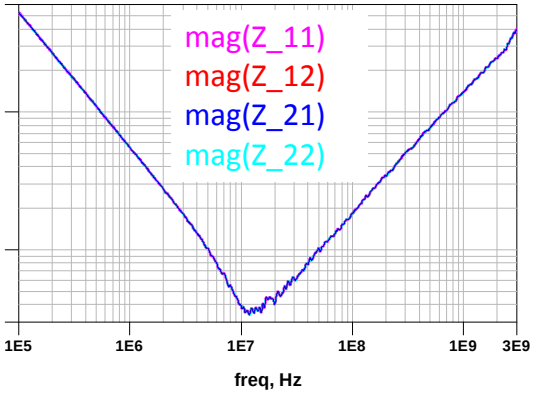
Want model to be both Sophisticated and Accurate

Model "Accuracy" – Synthesized Data



- Model is accurate, but device not in tolerance
- Accurate to manufacturing, not marketing

Example 2-Port "3-T" Model



Nominally a 2-port model (*.s2p file)

Functionally a 1-port model – all matrix elements are equal

Summary

- One model to rule them all
- Represent the device
- Measure/Model the way you use?
- Document constraints/assumptions

Thank you

Follow us on:

For more information, visit us at:
www.qualcomm.com & www.qualcomm.com/blog

UBM

Panel discussion: Needs and Capabilities for Modeling of Capacitor Derating

Delivering Models

Wilmer Companioni, KEMET Electronics

SPEAKER

Wilmer Companioni
Technical Marketing Engineer, KEMET Electronics
WilmerCompanioni@KEMET.com

With 10+ years of experience in both the design and business side of the electronics industry, Wilmer now handles technical marketing activities for KEMET Electronics. Main areas of responsibility include development and roadmap of KEMET's component simulation tool, K-SIM. In addition to K-SIM, Wilmer is also responsible for the production of technical marketing materials and training.

Capacitor Derating (one size does not fit all)

- MLCC characteristics are dependent on voltage, temp, and freq.
- Tantalum is stable over voltage, slightly less stable over freq and temp.
- Classic derating rules do not apply as capacitor technology changes.
- Different derating rules must be applied with each capacitor type.
- Conditions can also determine what derating to apply.
- Different characteristics de-rate differently.
- SOLUTION: Advanced in-situ component modeling

Capacitor Models

- Lumped Circuit Element (Static) Models

Pros	Cons
Wide Tool Acceptance	Instance Based
Human-Readable	Condition Dependent
Simplicity	

- Dynamic (Parametric) Models

Pros	Cons
Broadband Response	Limited Tool Acceptance
Frequency Independent	Limited Readability
Encryption Supported	

KEMET's Current Approach

- Generic parametric equations combined with measured data

$$Rs = Radj \times \left[1 + 10^{(Fx - \log(Ftest))} + 10^{(\log(Ftest) - Fh)} \right]$$

- Maintain web-based tool
- Frequent UI and model improvements
- Scheduled roll-out of new features and model support based on market needs
- Protect IP behind models
- Support as many tools as possible

Future of KEMET's tools and models

- Support common model formats
- Support parametric models for select tool vendors
- Support encryption of parametric models
- Support additional component types and families
- Scheduled roll-out of new features and model support based on market needs
- Make entire library readily downloadable
- Open online API for direct access from tool vendors?

Thank you!

QUESTIONS?

UBM

Needs and Capabilities for Modeling of Capacitor Derating

Shoji Tsubota, Murata

SPEAKER

Shoji Tsubota

General Manager (Capacitor, Div. 1), Murata Manufacturing

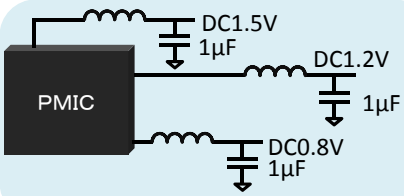
s_tsubota@murata.com

He has 30 years experience of MLCC Sales and Product Engineering, and his global marketing experience includes communication as well as Automotive/Industrial applications.

Currently, his focus is new business development for MLCC.

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

Current Issues regarding Component Modeling



EDA Users

Time consuming to download MLCC Spice model for specific conditions such as DC Voltage and Temperature.

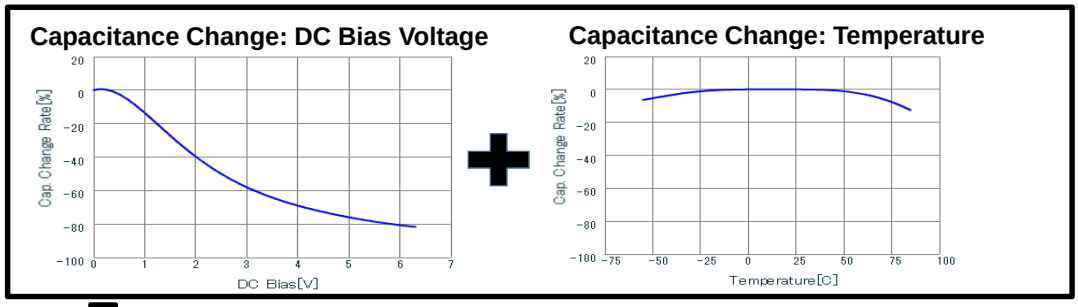
Comp. Vendors

EDA Vendors

Time consuming to develop EDA vendor specific data libraries because required model format is often different by CAD tools.

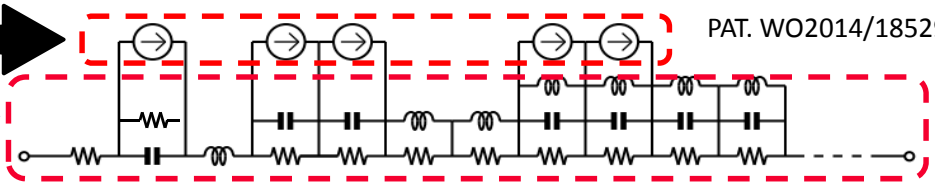
Component model format is often different by Component vendors.

Development of Dynamic Modeling



Dynamic Model

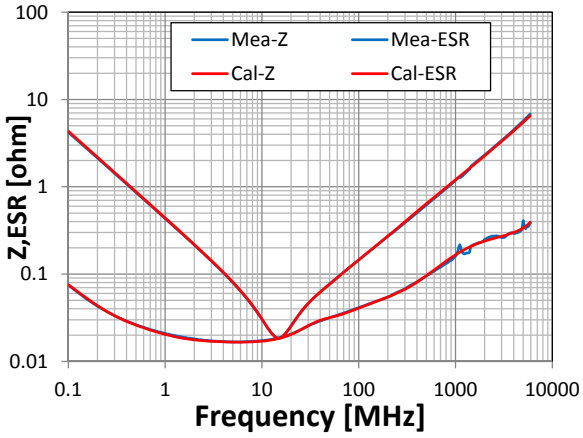
Static Model



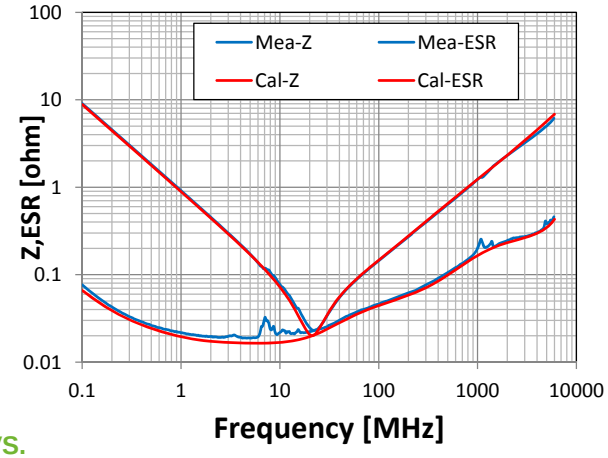
PAT. WO2014/185293

Development of Dynamic Modeling

25degC., DC0V



85degC., DC3.15V



<Static Model> VS. <Dynamic Model>

0603/X5R/0.47uF/6.3V

Modeling Comparison

	Static Model	Dynamic Model	
		Now	Future plan
DC Bias Voltage	O	◎	---
Temperature	O	◎	---
AC Voltage	X	X	Need further study to model accurately.
Initial Capacitance Tolerance	X	X	Simplified model can be done (more accurate model needs further study).
Capacitance Aging	X	Capacitance Aging is minimized when DC Voltage is applied.	

X = Not Available / O = Available with fixed condition / ◎ = Available

Standardization of Dynamic Modeling

- **Key Issues:**
  - Data format of Dynamic Modeling
  - Accuracy of the model (vs. variables to consider, calculation time)
  - Applicability of this modeling method to extend to other product series
  - Need common rules for Dynamic Modeling and future development

MORE INFORMATION

- Cadence® PSpice®
  http://www.murata.com/en-global/tool/library/pspice
- Cadence® Spectre®
  http://www.murata.com/en-global/tool/library/spectre
- Synopsys HSPICE®
  http://www.murata.com/en-global/tool/library/hspice
- Linear Technology LTspice®
  http://www.murata.com/en-global/tool/library/ltspice

[Products]
MLCC Capacitor GRM series
Power Inductor LQM series

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

SPICE Model

Static Model

```
*-----------------------------------------------------------------
* SPICE Model generated by Murata Manufacturing Co., Ltd.
* Copyright(C) Murata Manufacturing Co., Ltd.
* Description :2012/B/47uF/4.0V
* Murata P/N :GRM21BB30G476ME15
* Property : C = 47[uF]
*-----------------------------------------------------------------
* Applicable Conditions:
*   Frequency Range = 100Hz-6000000000Hz
*   Temperature = 20 degC
*   DC Bias Voltage = 0V
*   Small Signal Operation
*-----------------------------------------------------------------
.SUBCKT GRM21BB30G476ME15 port1 port2
C1 port1 11 3.40e-5
L2 11 12 1.27e-10
R3 12 13 1.86e-3
C4 13 14 1.23e-3
R4 13 14 2.61
C5 14 15 2.30e-3
R5 14 15 1.50e-1
C6 15 16 4.07e-3
R6 15 16 2.09e-2
C7 16 17 5.39e-3
R7 16 17 4.23e-3
C8 17 18 3.46e-3
R8 17 18 1.04e-3
L9 18 19 2.87e-11
R9 18 19 6.94e-2
L10 19 20 7.34e-11
R10 19 20 1.73e-2
L11 20 21 4.06e-10
R11 21 8.53e-3
```

Dynamic Model (Encrypted)

```
**$ENCRYPTED_LIB
**$PARTIAL
*-----------------------------------------------------------------
* PSPICE Model generated by Murata Manufacturing Co., Ltd.
* Copyright(C) Murata Manufacturing Co., Ltd.
* Description : 2012/B/47uF/4V (Capacitor)
* MURATA P/N : GRM21BB30G476ME15
* Property : C = 47 [uF]
*-----------------------------------------------------------------
* Applicable Conditions:
*   Frequency Range = 100Hz - 6GHz
*   Temperature = -25 degC - 85 degC
*   DC Bias Voltage = 0V - 4V
*   Small Signal Operation
*-----------------------------------------------------------------
* Encrypted Netlist
*-----------------------------------------------------------------
.subckt GRM21BB30G476ME15 Port1 Port2 PARAMS:temperature=25
$CDNENCSTART
eee8c5c7a2bc4b01f045f303678664e7916da0bae22e8cb0bba041dd67c69ce448ea7014
3b33857aaa06aa9619c3e837a21e9923a241a839a9452a9dc61c6388821d59298e4f1d0d
e47652bdde991f48d6085d4ffa1a7c79c61c6388821d59298e4f1d0dab4ab31a8aea7acf
bd92b7ac246cc3c14fc392e13cf1f65f9bbd027d10818dcd47c6b1555096167c801ed24c
b6df740f908333a34fc392e13cf1f65f5d33d2c20c2dc32247c6b1555096167c801ed24c
71332ed7870e2aea4fc392e13cf1f65f2adcaccfcbabb2fd47c6b1555096167c801ed24c
4660120ca6f3cd834fc392e13cf1f65fa73f8e85335d981947c6b15550961
533280b9926b49794fc392e13cf1f65fbf071e27ea116e4247
042c32d9e38627d432831e5a03a8f78140ad722fe7fa
cd0d5bb3c913bba35ff773029427e8686597d27
2b89cef1ae448caf41bf0cf5fae977ff1
```


Thank you!

QUESTIONS?

UBM

Panel discussion: Needs and Capabilities for Modeling of Capacitor Derating

An EDA Perspective

Sam Chitwood (Cadence)

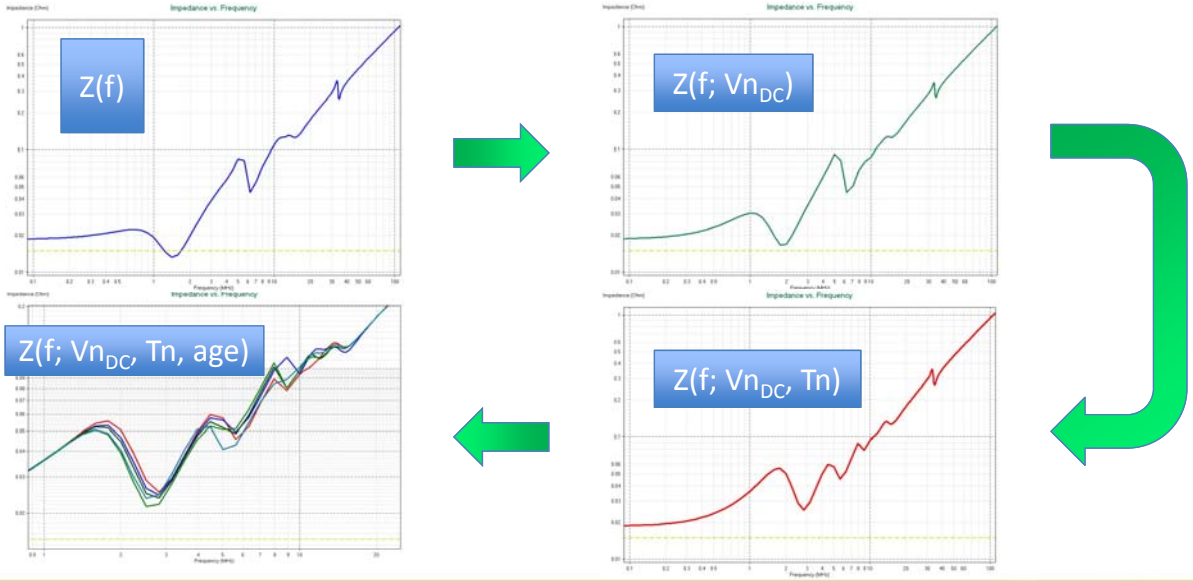
Speaker

Sam Chitwood
Product Engineer, Cadence Design Systems
chitwood@cadence.com

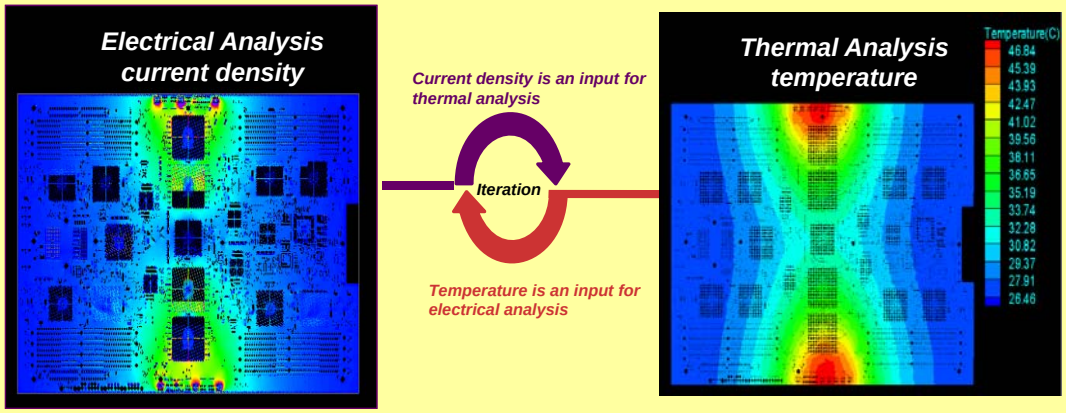
Sam Chitwood has been a Product Engineer for the past three years. His focus areas include PDN optimization and IC package / PCB model extraction. His duties involve product planning, assisting with customer evaluations, AE support and training. Before Cadence, he was an application engineer at Sigrity for ten years. He has BSEE and MSEE degrees from Georgia Institute of Technology.

DESIGNCON 2016 WHERE THE CHIP MEETS THE BOARD JANUARY 19-21, 2016 #DC16

Vision for Analysis PDN Capability



Existing Electro-Thermal Co-Analysis Flow



Both electrical resistance and leakage power increase at higher temperatures

Both Joule and component heating change temperature distribution

Present Analysis Flows

(*3 rails, same 4 cap types each rail, 10 instances of each cap type each rail*)

- Encrypted Models
  A. Assign parametric component models (four models)
  B. Perform electro-thermal analysis to determine Vn_{DC} and Tn.
  C. Manually assign instance-local parameter values for Vn_{DC} and Tn. (120 operations)
  D. Define a global parameter value for age. (1 operation)
  E. Perform PDN AC analysis

NOTE:
- Step (C) is tedious.

Present Analysis Flows

(*3 rails, same 4 cap types each rail, 10 instances of each cap type each rail*)

- Instance Models
  a. Assign nominal component models (four models)
  b. Perform electro-thermal analysis to determine Vn_{DC} and Tn.
  c. Query component vendor tool for instance models with (Vn_{DC},Tn,age). (120 operations)
  d. Assign each model to the corresponding component instance. (120 operations)
  e. Perform PDN AC analysis

NOTE:
- Step (c) is tedious and it is in the component vendor's tool.
- Step (d) is back to the EDA tool and very tedious and error prone.
- Significant chance for error in these two steps, especially (d).

Automation Enablement

- For both model types
  - Electro-thermal analysis is already fully automated.
  - EDA tool needs to add default local parameters for voltage and temperature and update Vn_{DC} and Tn instance-local parameters as well as apply global parameter for age.
- In addition, for instance models
  - The sequence of an automated flow must change vs. a manual flow.
  - Component vendor tool needs to provide programmatic API for EDA tool to query for models from within a PDN AC simulation.

Automated Analysis Flows

- Encrypted Models
  A. Assign global parameter for age.
  B. Assign parametric component models (four models)
  C. Perform PDN combined DC-thermal-AC analysis
- Instance Models
  a. Assign global parameter for age.
  b. Assign instance component models (four models)
  c. Perform PDN combined DC-thermal-AC analysis

NOTE: Exactly the same flow to an OEM, just assign different models.

Component Model Types

- Encrypted Models
  - Huge component vendor effort, tool support issues, not all EDA tools support encryption
- Instance Models
  - Large effort for component and EDA vendors to automate, no standard models or API
- Compiled models (*a new type of model envisioned*)
  - Analogous to IBIS-AMI models
  - One component vendor compiled model would support all EDA tools
  - Some component vendor effort to support 32/64 bit and Windows/Linux
  - Significant effort for each EDA tool to support (*months*, not *weeks*)
  - Effort for EDA, component vendor and OEM to define the model and API
  - Eventual standardization efforts?
  - Easily extensible to other component types

How Broad are the Requirements?

- Parameters
  - Bias, temperature, age, …
- Analyses
  - PDN, SI, electromagnetic, analog, digital, RF, …
  - PCB, package, chip/package/PCB system, circuit, …
- Component types
  - C, R, L, EMI, …
- EDA tools
  - These domains and applications will require at least 20 tools to be supported.
  - This will be perceived by some OEMs as an issue.
  - Is broad EDA tool support a requirement or a desire?

Thank you!

QUESTIONS?

Status of Discussion

- The expressed PDN analysis need of OEMs can be addressed with presently available component vendor models and EDA analysis tools.
- HOWEVER …
  - The solution is extremely tedious for OEMs.
  - At this time EDA tools have not automated links among all the analyses involved.
  - Models are either not available for many EDA tools or if they are available they are not amenable to automation with present EDA tools.
- To enable a reasonable solution, effort is required from component and EDA vendors with guidance from OEMs.

Meeting the Requirements

	General Effects	Non-Disclosure	Many EDA Tools	Automation	Other Components	Effort
Encryption	+	+	-	+	+	comp ++ eda
Instance	+	+	+	0	+	comp eda
Compiled	+	+	+	+	+	comp eda + oem -

Next Steps

1. Discuss high-speed community feedback
2. Choose a path forward
3. Investigate details
4. Review (and iterate?)
5. Prototype
6. Publish
7. Standardize?

Audience Participation

- Survey
- Seed Questions?
- Q&A

Seed Questions

- How much difference in performance do the parameters such as bias, temperature and age really make for PDN designs?
- Is the underlying performance data for components known and readily available to generate parametric models for all of the important effects?
- For which effects would you consider parametric model access the most critical?
- What EDA tools now support the available models? And for what applications?
- Parameter-value-specific models are already available. So, what's the issue? Why aren't OEMs applying the models and/or why aren't EDA companies providing the automation to use them?
- Encrypted parametric SPICE models are now available for a handful of EDA tools. What more do we need?
- Is it difficult for an EDA tool to automate application of parameter-value-specific models? Or for encrypted models?
- Is it really a big deal for a component vendor to support a large number of EDA tools with encrypted models?
- A new type of compiled model was mentioned. Isn't that a lot of effort and complexity for everyone involved without a lot of benefit?
- Would it be useful to create standard measurement conditions for component characterization?

Thank you!

QUESTIONS?