PCB Design 007 *QuietPower* column

Do bypass capacitors change plane resonances?

Istvan Novak, Oracle, January 2012

The other day my friend Greg asked: "If I add surface-mount capacitors to a bare pare of planes, I am told that the resonant frequency will drop. On the other hand I have someone with expertise who is saying that is not the case. What would you expect to see?" As happens many times, both observations have elements of the truth in them. Moreover a third scenario is also possible, so stay tuned.

This was my answer to Greg: "As usual, both statements are correct within their context. People who say that the resonance frequency will drop may refer to the fact that as soon as you add a capacitor to the planes, a new resonance will be created, which is always lower in frequency than any of the modal resonances on the plane. People who say that the resonance frequencies do not change usually refer to the natural (modal) resonance frequencies of the planes; those are hardly changed by the capacitors attached to the surface of the board."

As we explored it earlier in the column "Resonances in power planes," plane pairs have various standing wave patterns at high frequencies. When the plane shapes are rectangular, it is easy to calculate the modal resonance frequencies: we fit half sine-waves, one over the longer side and one over the shorter side. These will represent the lowest possible resonance frequencies in the structure. Any integer multiple of these frequencies can occur as parallel resonance in the impedance profile. Dependent on where we are on the planes, some of these resonances may cancel and at those harmonics at that particular location we may not see a resonance. For odd shapes we can't calculate the resonance frequencies so easily and it is best to rely on numerical simulations or measurements.

To illustrate my explanation, I show here measured data from a large VXI backplane; I used to work on it a number of years ago.

Figure 1 shows the impedance profile of one of the power plane shapes on the backplane with no component attached. Note the low-frequency capacitive down-slope, where the phase is approximately -90 degrees, indicating that at low frequencies the plane pair behaves like a static capacitance. Around 100 MHz we see an impedance minimum; this highlights the series resonance of the plane's static capacitance and inductance. Above the series resonance frequency the impedance magnitude has an up-slope trend with multiple resonances. We can also see that here the phase is mostly positive, around 90 degrees, which corresponds to the equivalent inductance of the plane pair. The plane shape's outline was not perfectly rectangular, and it had multiple cutouts and various size and shape holes for screw attachments and plug-in slots. While the odd shape does not allow us to do simple hand calculations, based on the measured impedance profile we can derive a few important parameters.

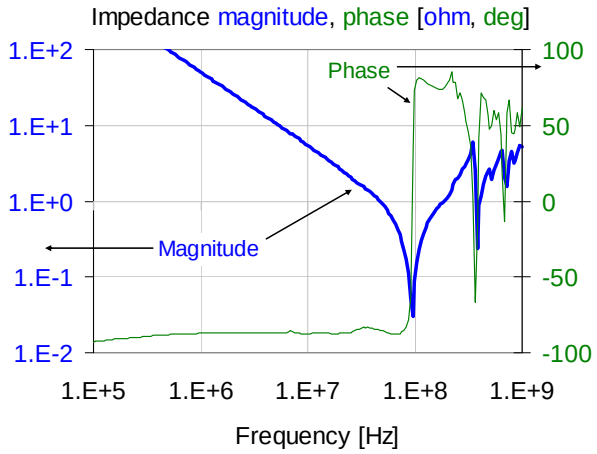

Figure 1: *Impedance magnitude and phase measured on a power-ground plane pair of a VXI backplane.*

Figure 2 shows the same data, but now we plot only the impedance magnitude, together with a few markers. The red straight line shows the impedance magnitude of a 3nF ideal capacitance. Up to about 50 MHz the red trace and the measured blue trace line up very well, telling us that the low-frequency static capacitance of the plane pair should be close to 3 nF. The green straight line represents the impedance magnitude of a 660 pH ideal inductor. At high frequencies this lines up well with the average measured impedance, telling us that the equivalent plane inductance is around 660 pH.

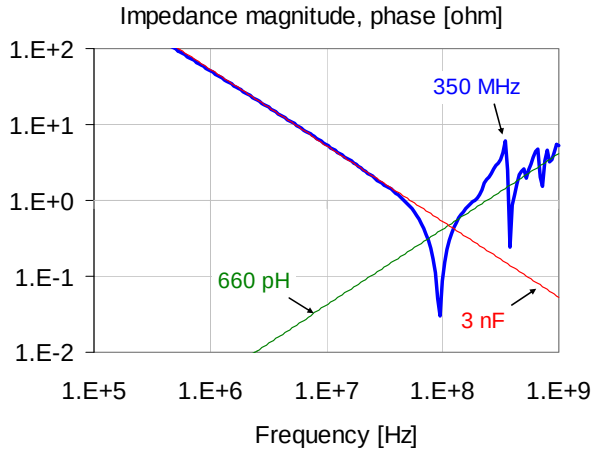

Figure 2*: Impedance magnitude of the same VXI backplane plane pair with the static capacitance (red line), equivalent inductance (green line) and first parallel resonance (blue label) identified.*

As we showed in the column "Simulating planes with SPICE," the plane pair's equivalent inductance is proportional to the dielectric separation, and each miliinch (mil) spacing represents approximately 33 pH inductance. From these numbers we can conclude that the power-ground separation of this plane pair is approximately 20 mils, or 0.5 mm. This is a reasonable assumption, since this was an old, thick backplane, designed –in today's standards- for low-frequency operation. It was also known about this backplane that the PCB laminate was regular FR4 dielectric, with a low-frequency dielectric constant of about 4.5.

For a parallel plane pair of area *A*, with a plane separation of *s* and dielectric constant of D_k, the static capacitance can be calculated as

$$C = \varepsilon_0 D_k \frac{A}{s} \tag{1}$$

where ε_0 is the permittivity of free space. If we plug in numbers in the MSVA system, we get the capacitance in Farads. If we prefer the inch system, there is a simple formula to remember. With Dk~4.5 and 1-mil plane separation, each square inch represents approximately 1 nF capacitance. Of course the capacitance scales inversely with the plane separation: for instance one square inch of dielectric with 2 mils of FR4 plane separation has 0.5 nF capacitance. With our 20-mil plane separation we can expect 0.05 nF for each square inch, so the 3 nF plane capacitance comes from a 60 square inch area.

The last item marked on *Figure 2* is the first F_{res} parallel resonance at 350 MHz. If this was a rectangular shape with a longer dimension of *X*, this resonance frequency could be calculated from

$$F_{res} = \frac{c}{2X\sqrt{D_k}} \tag{2}$$

where *c* is the speed of light or $3*10^8$ m/s. By equating *Eq (2)* to 350 MHz, we get approximately an 8-inch length for *X*. To get a total area of 60 square inches, an equivalent rectangular shape would then have a size of 8" x 7.5".

Next we add a capacitor to this plane. *Figure 3* shows the measured complex impedance of an electrolytic capacitor. The thick blue line is the measured data. The thin red horizontal line is at 0.25 Ohms, which matches well the measured impedance in the 100 kHz to 5 MHz frequency range. The particular Vector Network Analyzer I used for this measurement did not go lower than 100 kHz, so we do not see the capacitive behavior of this electrolytic capacitor. The label on the capacitor stated a nominal capacitance of 220 uF. This capacitance has a 2.9 kHz R-C corner frequency with the 0.25 Ohms ESR value, so unless we go below 1 kHz with the impedance measurement, we can not expect to see a clear capacitive slope. The thin green straight line represents the impedance magnitude of a 4 nH inductance, which matches well the measured impedance everywhere above 2 MHz.

Now if we add this capacitor to the plane shown in *Figures 1* and *2*, we get the measured impedance magnitude plot shown in *Figure 4*.

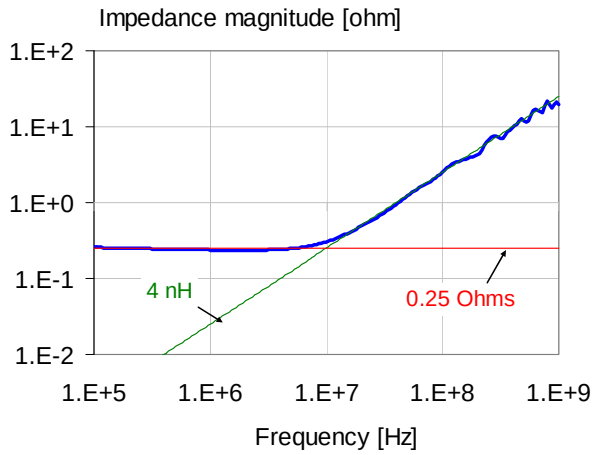

Figure 3: Measured impedance magnitude of a 220 uF electrolytic capacitor with solid lines marking ESR = 0.25 Ohms and ESL = 4 nH.

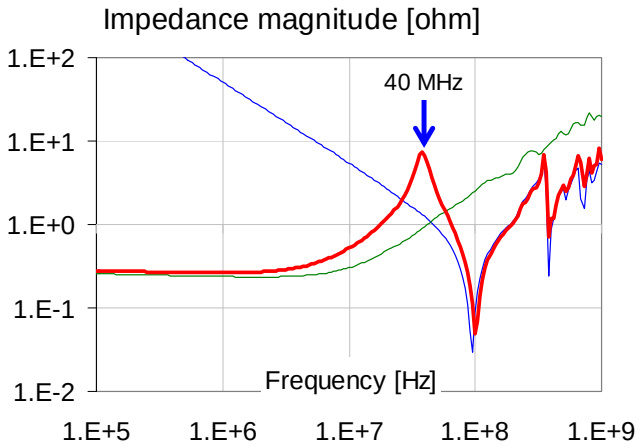

Figure 4: Impedance magnitude of the VXI backplane and the 220 uF electrolytic capacitor.

For sake of easy comparison, *Figure 4* shows all three impedance curves: the thin blue line shows the impedance of the bare board, the thin green line shows the impedance of the stand-alone capacitor, and the red line shows the impedance of the board with the capacitor attached. Note the large new peak at 40 MHz, but note also that at higher frequencies the impedance plot and the resonances do not change as we add the capacitor.

The 40 MHz peak occurs where the impedance of the plane is still capacitive but the attached capacitor already became inductive. We can calculate this frequency approximately from the 3 nF plane capacitance and the 4 nH ESL of the capacitor, and we get 46 MHz. Considering the crude approximations we use here, this is a reasonably good agreement.

The photo of *Figure 5* shows a small portion of the VXI backplane. The capacitor was attached to the board at the C4 location, the measurement was done at the near-by C3 location.

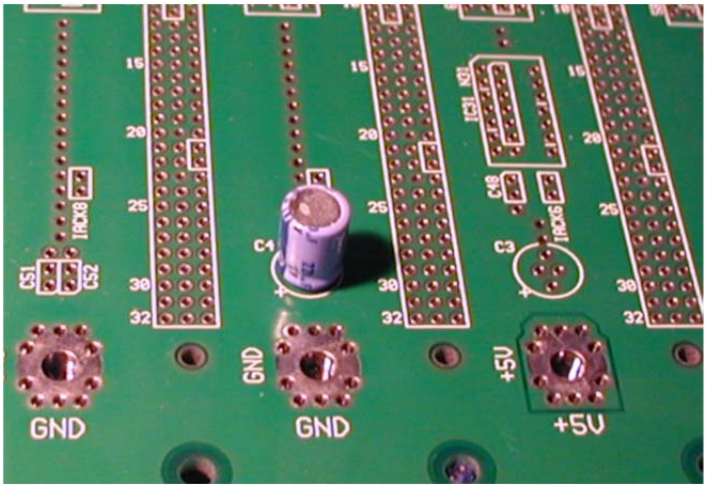

Figure 5*: Part of the VXI backplane, where the capacitor was attached.*

Finally we can ask ourselves: is it really true that the frequency of this capacitor-plane inter-resonance is always lower than any of the modal resonances? The answer will also bring us to the third possible case, mentioned at the very beginning.

The capacitor-plane inter-resonance is created by the static capacitance of the planes and the ESL of the bypass capacitor. For a given geometry and dielectric material the static plane capacitance is fixed and we can change only the ESL of the attached capacitor. In a real multi-layer printed circuit board we always need vertical vias to connect the capacitor on the surface to the planes below. Even if we had the power-ground plane pair assigned to the top two layers so that the capacitor could be laid down flat on the outside plane and one of its terminals connects directly on the surface without a via, we still need a via to connect the other terminal to the plane below and we also have the additional inductance associated with the horizontal distance through the capacitor body. If we assume a very short wide capacitor body with very-very low inductance, we are still left with the inductance of the via connecting the second terminal to the plane below. So speculatively we can conclude (and we can also do detailed 3D simulations to prove it) that attaching a single capacitor to a plane pair will always create a capacitor-plane anti-resonance ***lower*** than any of the modal resonances.

However, if we attach multiple bypass capacitors to the planes, and their cumulative inductance is much lower than the equivalent inductance of the planes, all modal resonances and the capacitor-plane inter-resonance will be highly suppressed. This is a clear benefit of the old-fashioned brute-force capacitor sprinkling.

To get good resonance suppression, the cumulative inductance of the attached capacitors has to be less than approximately 10% of the plane inductance. And here comes another interesting twist: as we said in the column "How thin laminates suppress resonances," thin laminates will inherently suppress modal resonances, but they also have low plane inductance. While low plane inductance helps to keep the power distribution impedance low at high frequencies, at the same time it also makes it harder for us to eliminate the capacitor-plane inter-resonance.