Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals

Laura Kocubinski, Gustavo Blando, and Istvan Novak
Oracle Corporation

Speaker

Laura Kocubinski

Hardware Engineer, Oracle

laura.kocubinski@oracle.com

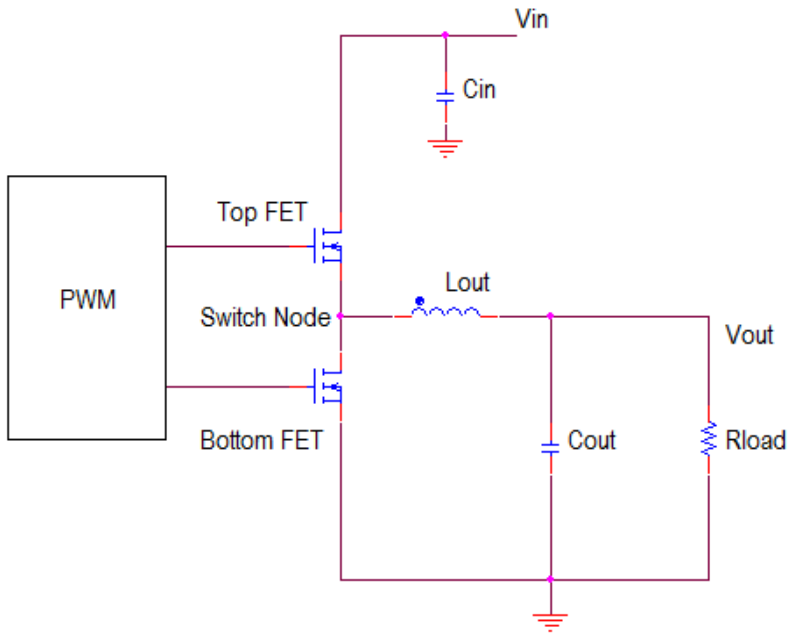
Laura Kocubinski is a Hardware Engineer at Oracle Corp. She currently works on signal and power integrity within Oracle's SPARC server division. She received her BSEE from Rensselaer Polytechnic Institute.

Outline

- Introduction
- Background: Problem Discovery
- Debugging a Solution
- Proof of Solution
- Understanding the Noise Source
- Conclusion

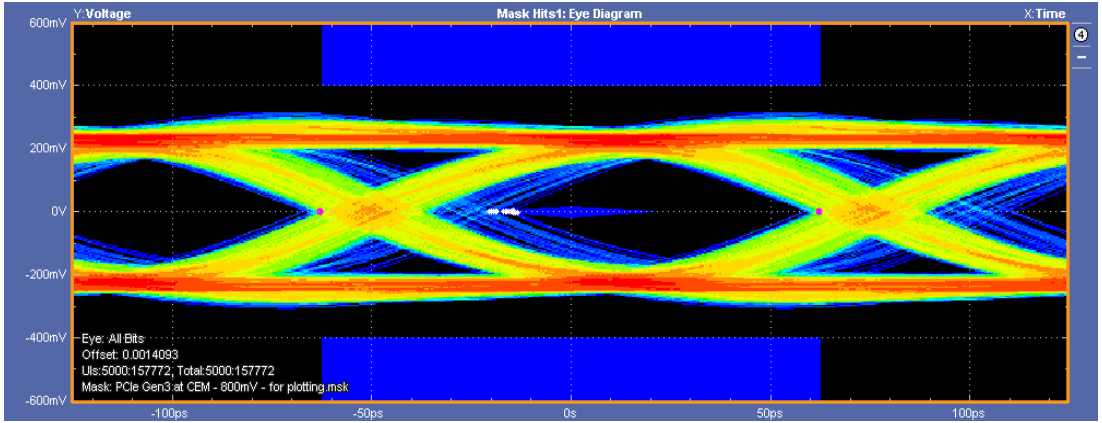
Introduction

- Mid-frequency noise (~100 MHz) associated with the fast switching of a switching regulator may couple onto nearby signal traces
- A case of this noise coupling in a practical server system will be explored
- → Mid-frequency noise may be difficult to contain and understand



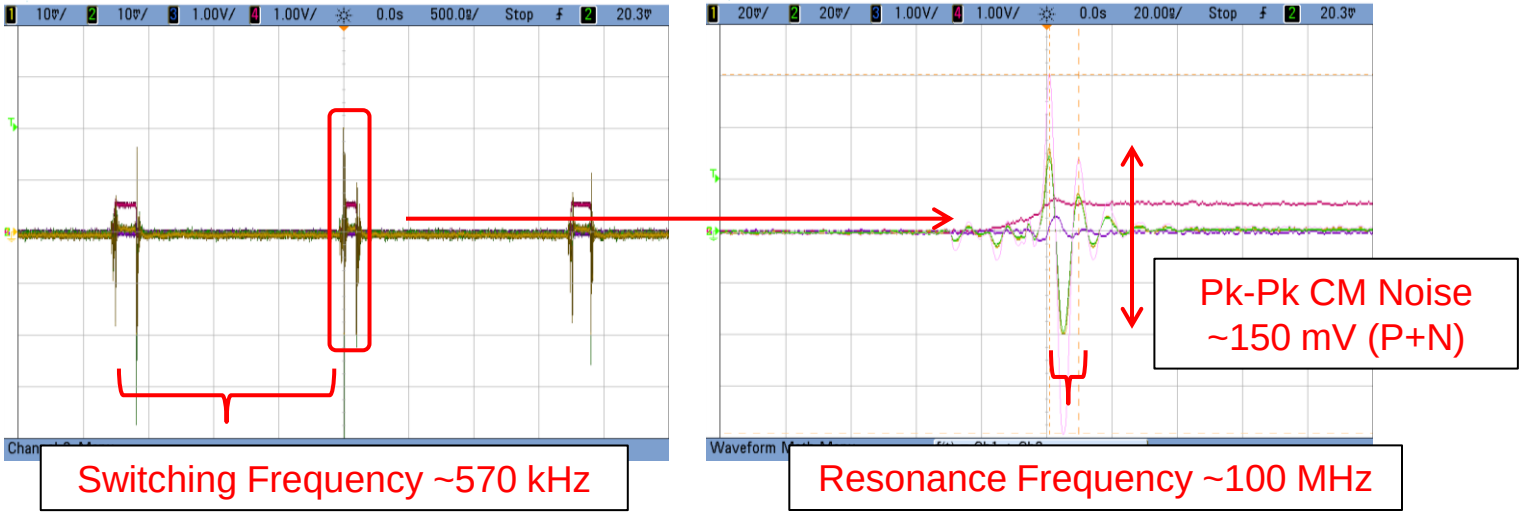
Problem Discovery: Compliance

- In a multi-processor server system, one downstream PCIe (Gen3) lane failed badly during compliance testing, but…
- Only occurred with one particular option card, in one particular slot



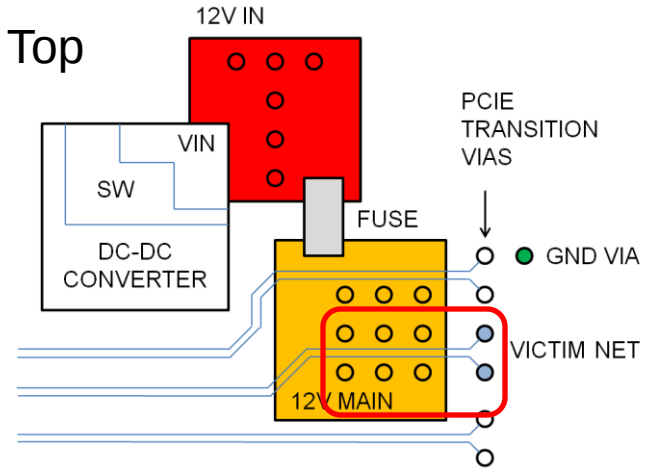
Common-Mode Noise

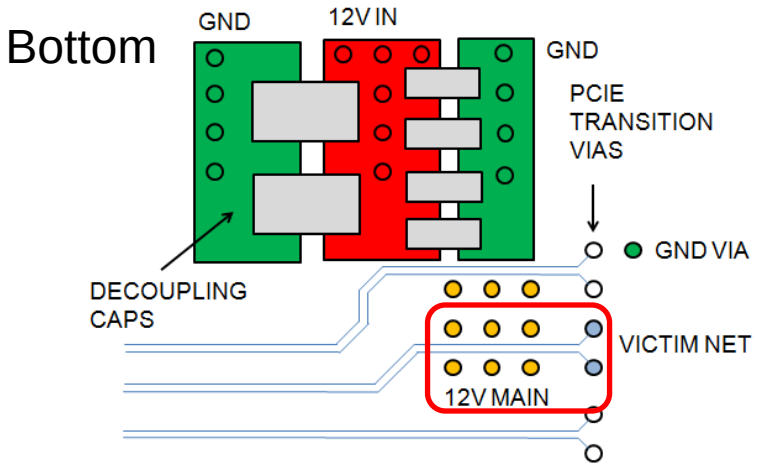
- When victim lane was measured on an oscilloscope, periodic common-mode noise observed during rising edge of a nearby switching regulator



Review of Layout: Problem Area

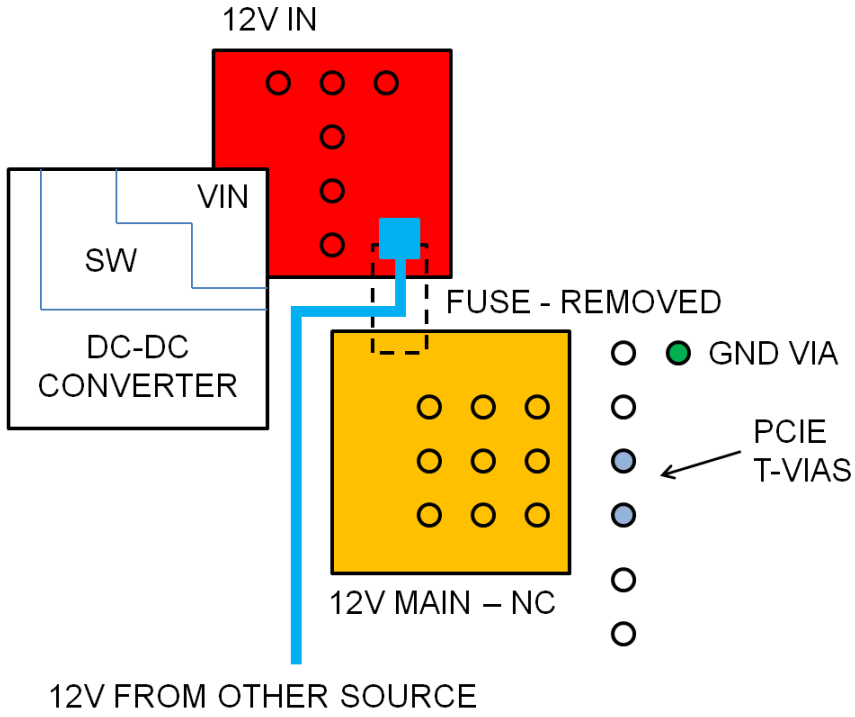
- Victim lane routed through 12V vias input to regulator
- Reasonable to think electrical coupling from 12V vias could be causing CM noise on low-swing, high-speed signal





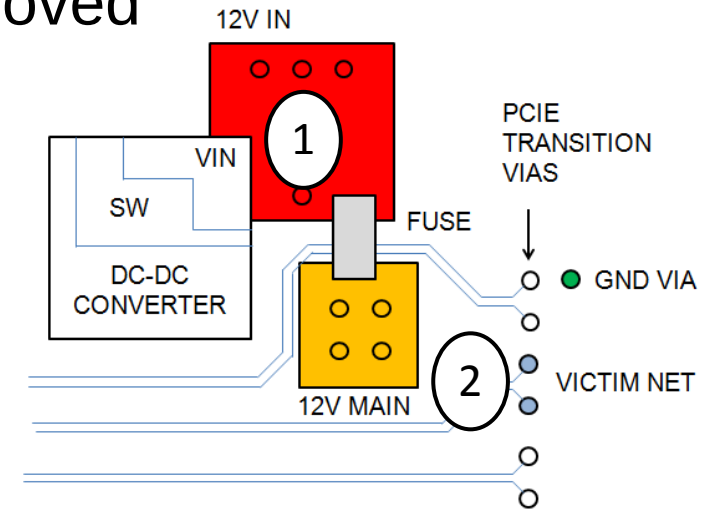
Debugging a Solution

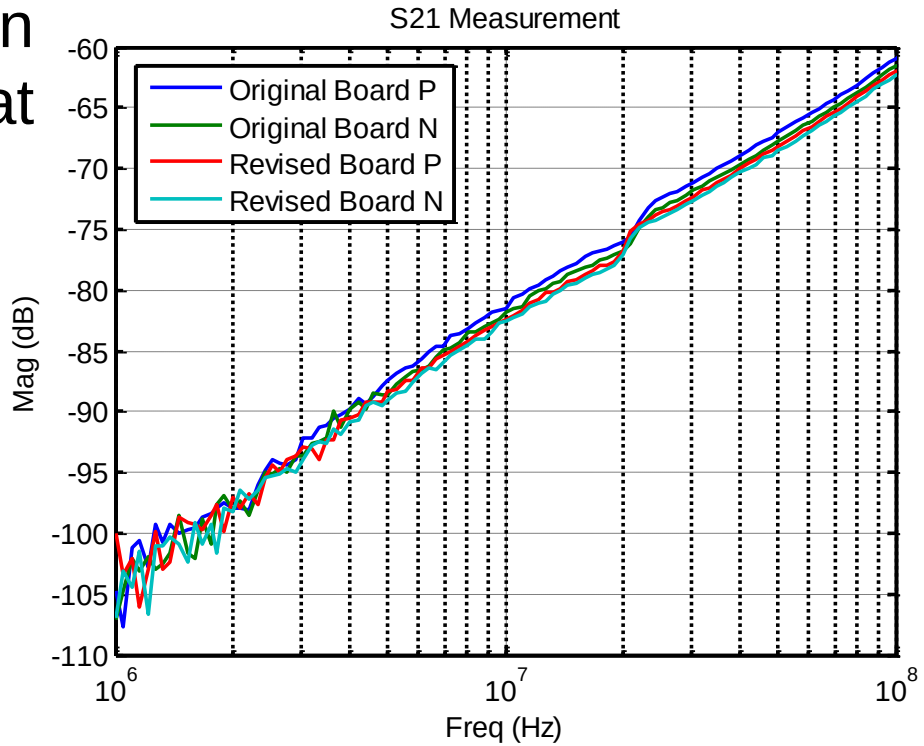
- Bypassing fuse and supplying 12V from another source (avoiding current circulation in vias) eliminated CM noise on victim lane
- → Proved CM noise caused by routing signal traces in close proximity to 12V vias
- Implemented on next spin of board



Follow-up Crosstalk Measurements

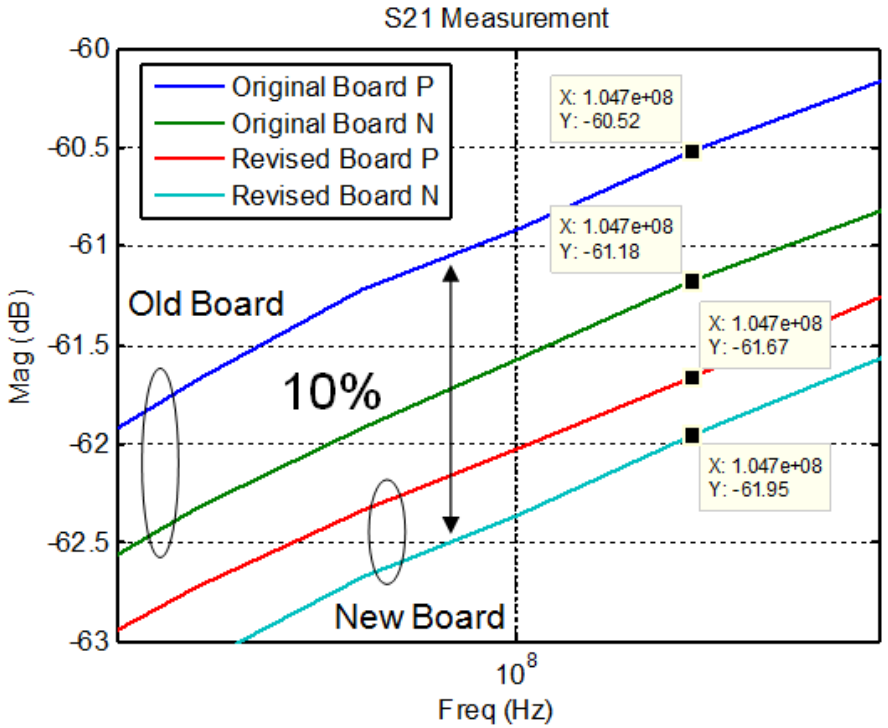
- Crosstalk measurements taken on next revision to validate that coupling mechanism was removed





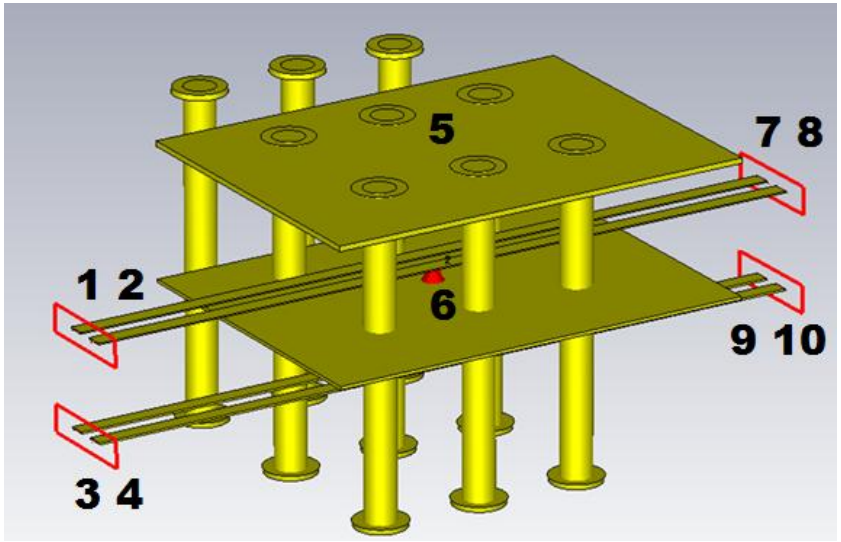
Follow-up Crosstalk Measurements

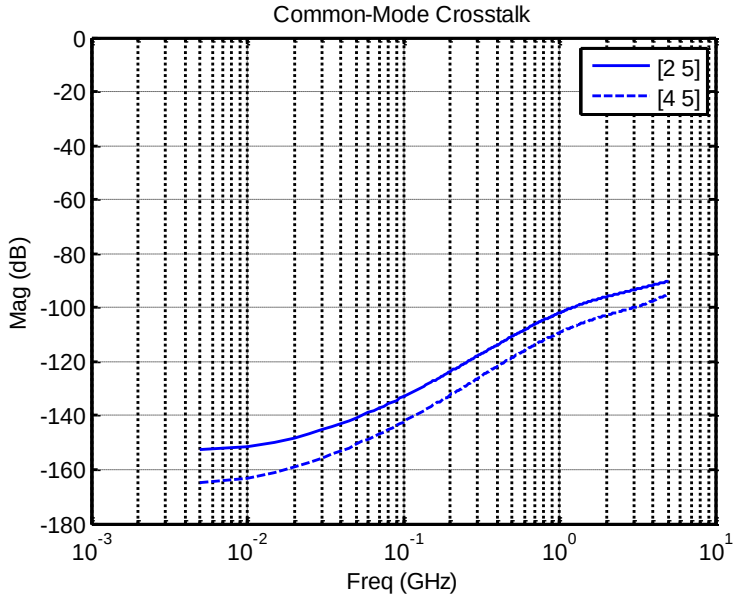
- Only a 10% improvement in crosstalk magnitude
- Coupling mechanism was not removed with layout changes!!!



3D Field Solver Simulation

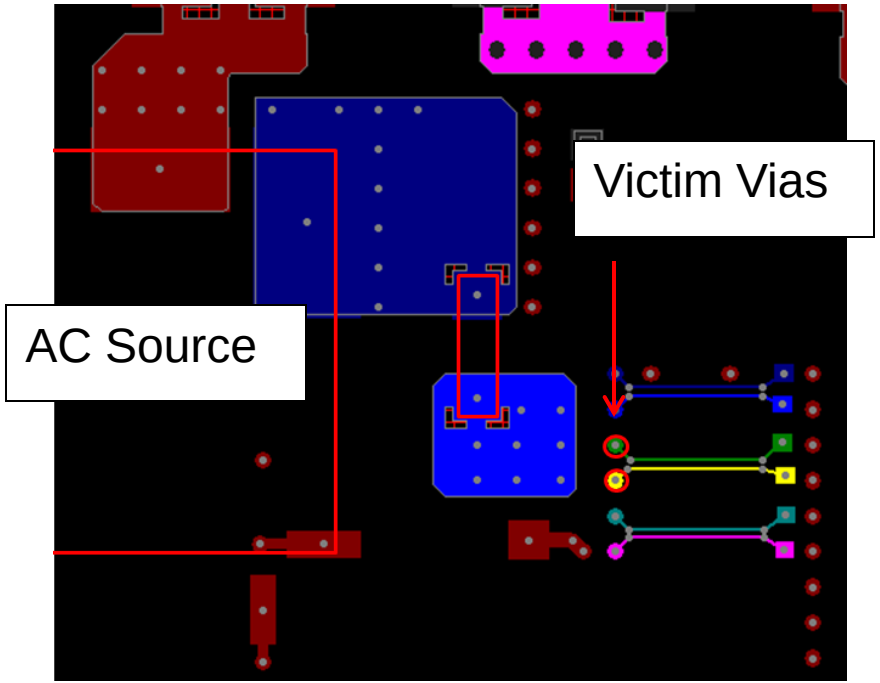
- Coupling is not capacitive (trace-to-via) but must be magnetic (loop-to-loop)





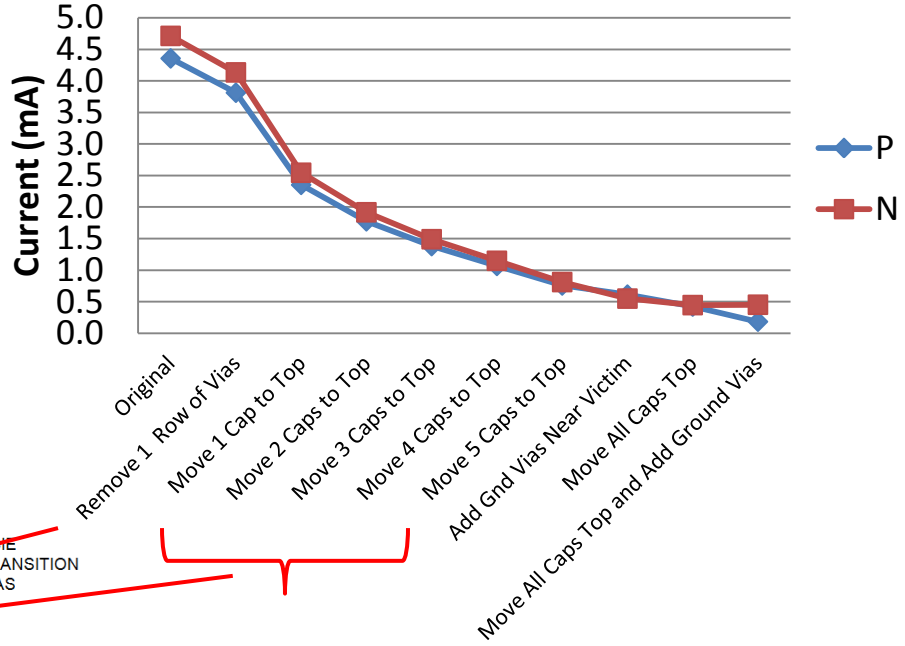
Larger Plane Simulation

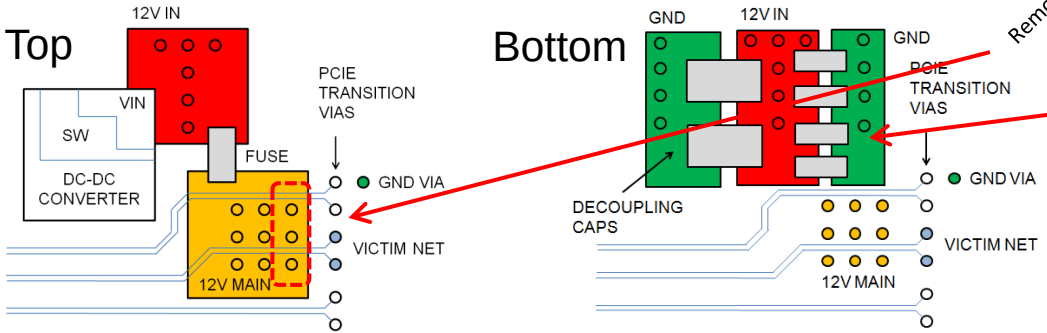
- Hybrid solver set up to simulate current induced in victim vias
  - AC source with constant amplitude (17A) setup at 12V input vias of switching regulator and swept from 10 MHz – 500 MHz



Larger Plane Simulation

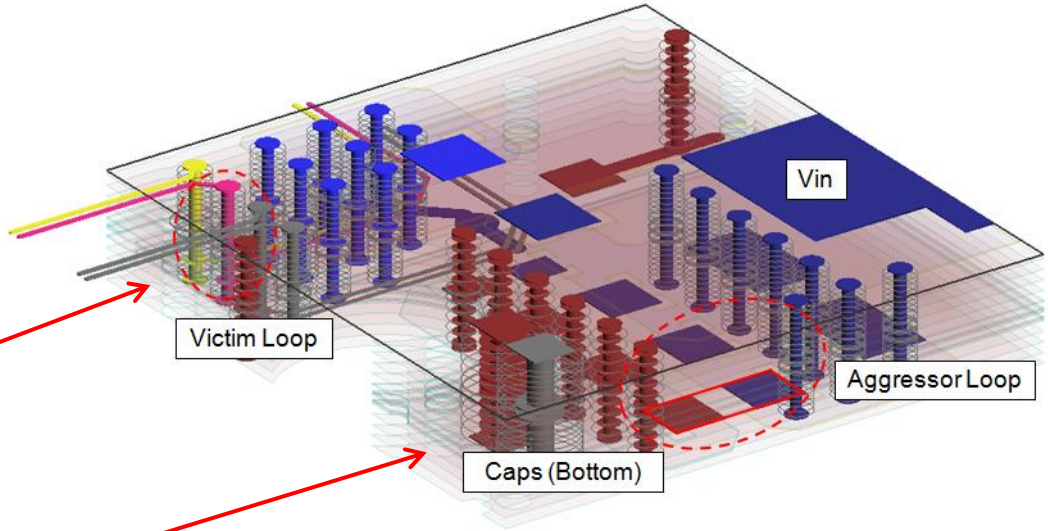
- Simulation run with number of layout changes
- Results (taken at 100 MHz)
- *CAPACITORS ON THE BOTTOM*

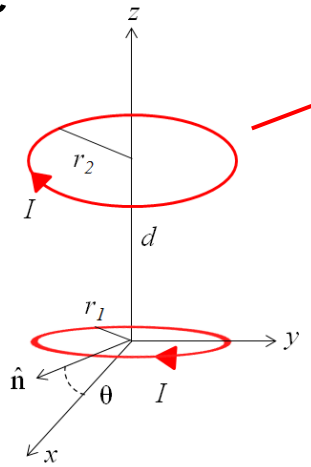




Placing Input Capacitors on Bottom

- Caps are on the bottom
- This creates loop that is the aggressor noise source

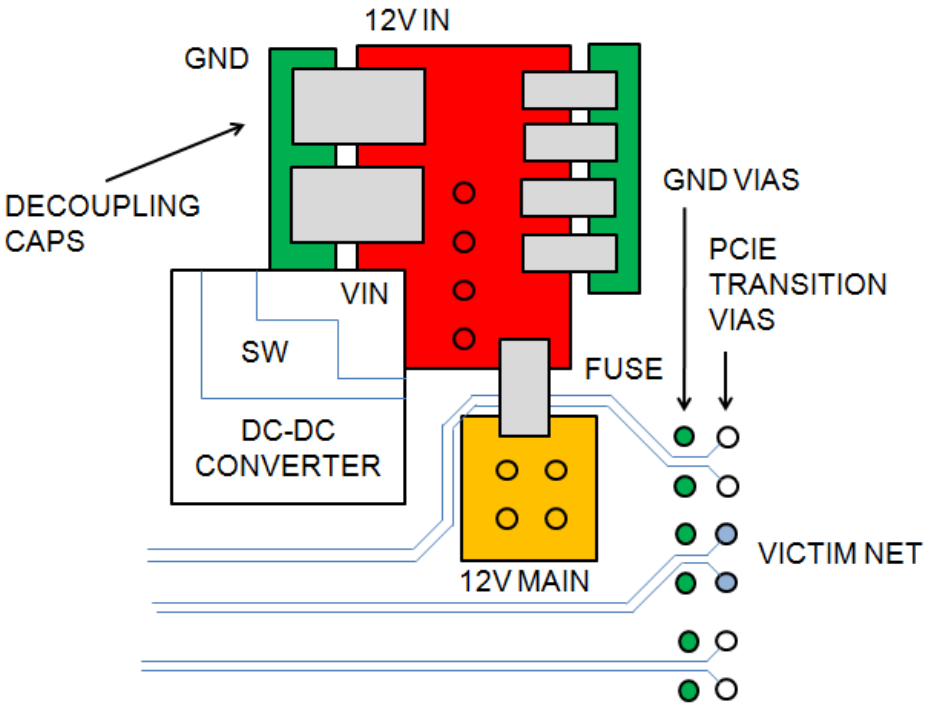




- Size of aggressor loop (r1)
- Size of victim loop (r2)
- Distance between the loops (d)
- Relative loop orientation (θ)

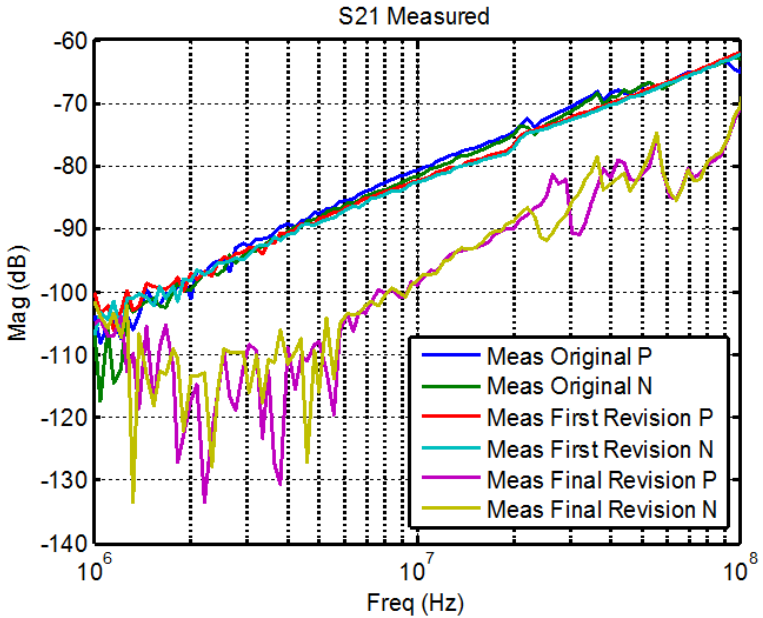
Final Revision of Board

- On final board revision, added ground shielding vias and moved decoupling capacitors to the top of the board
- We threw everything at it!!!!!!!!!!!!!!!!!!



Proof is in the Pudding: Crosstalk Measurements

- Crosstalk measurements of final board shows significant improvement in crosstalk!!!

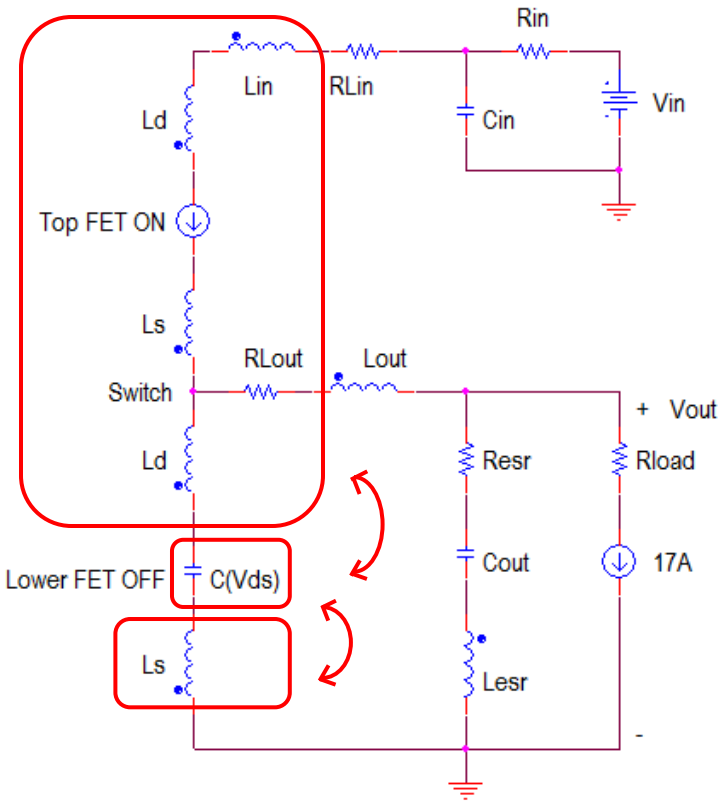


Case closed

But wait, why 100MHz???

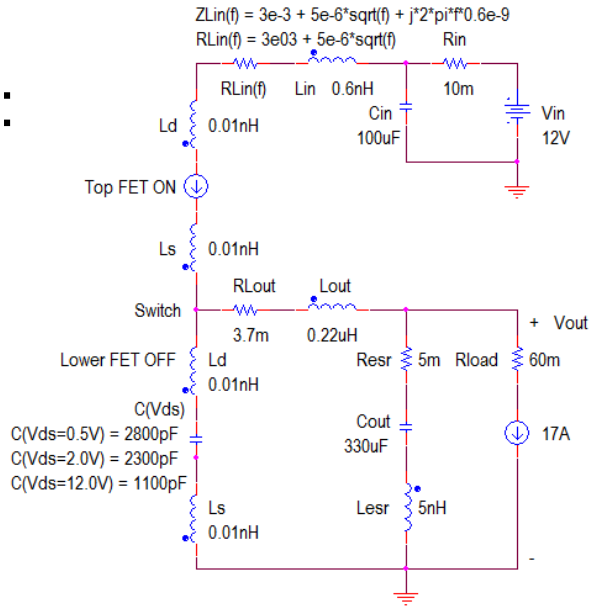
Understanding the Noise Source

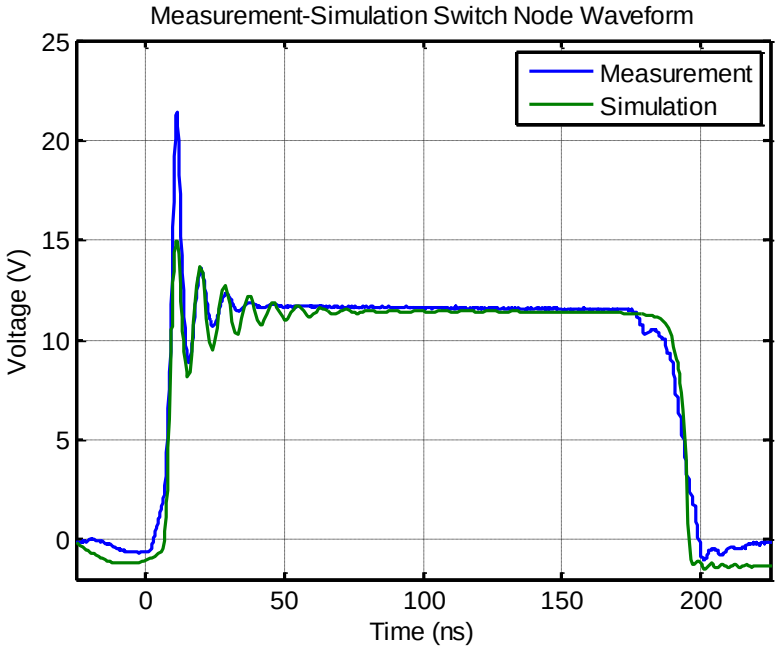
- SPICE model created to simulate ringing on the rising switching waveform
- Ringing frequency (100 MHz) is a result of resonance between inductance of power path, package inductances and parasitic capacitance of low-side FET



Understanding the Noise Source

- SPICE simulation correlated to measurement taken at switch node
- Values:





Conclusion

- The source of noise in this layout was fast slew rate associated with high di/dt of switch node waveform
- On the rising edge of the switch node voltage, the resonance frequency (100 MHz) was set by the capacitance of the low-side FET, the parasitic inductance of the FETs packages, and the inductance of the supply rail feeding the DC-DC converter input
- Placing the input decoupling capacitors and the converter on opposite sides of the board creates an aggressor magnetic loop for high di/dt
- To mitigate inductive noise coupling at mid-frequencies, place decoupling capacitors and the switching devices on the same side of the board (reduce aggressor loop)
- If this can't be done, place ground vias nearby the victim vias (reduce the victim loop)!!!
- →Be careful placing signal vias near switching regulators – mid-frequency noise may travel farther than you think!!!

Acknowledgements

The authors would like to thank Roger Dame, Eben Kunz, Abe Hartman, Seyla Leng, and Eugene Whitcomb (of Oracle) for their help and support with this project.

Thank you!

QUESTIONS?