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STABILITY ANALYSIS OF CONSTANT-FREQUENCY CURRENT-MODE CONTROLLED POWER CONVERTERS

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ABSTRACT

A stability analysis of current-mode controlled constant-frequency switching power converters is presented. There are three possible types of instability in these circuits: - open--loop oscillation above 50% duty ratio, - closed-loop continuously arising oscillation at the first subharmonic of the clock frequency, - closed-loop, hysteretically arising oscillation at the first or higher order subharmonic of the clock frequency. The paper gives insight into the mechanism of these oscillations and introduces simple models and analytical methods for determining the maximum allowable ac loop gain of the fed-back converters. Calculations and experiments were carried out for the buck and boost regulators. A close correspondence demonstrates the practical usefulness of the proposed methods and verifies the given stability criteria.

1. INTRODUCTION

Current-mode control has been invented in 1967 by T. Froeschle of Bose Corp. [1]. This superior control method was re-invented by Weinberg and O'Sullivan of European Space Agency and was reported in 1977 [2]. Since then it became more and more popular among the designers of switching power converters. Results of investigations on various aspects of current-mode control have been published in a number of papers from [3] to [10].

The basic principle of current-mode control is the inclusion of an extra loop into the regulator circuit in order to control directly the switch current. Turn-off of the switch is determined by a current threshold, rather than by the duty ratio of a traditional pulse-width modulator. The switch can be turned on by using one of the following methods: (a) after a fixed amount of current decrease in the inductive component, (b) after a fixed time interval or (c) by a constant-frequency clock signal. The three different types of switch controllers together with the basic waveforms are shown in Fig.1.

The extra loop should use the inductor current (i_L) in version (a) and either the inductor current or the switch current (i_{sw})

in versions (b) and (c). Versions (a) and (b) provide free running operation.

In all cases the power switch is controlled so as to make the inductor peak current follow the error signal (v_c). This means that the inductor can be substituted by a pure voltage-controlled current source.

The fact that the inductor is practically omitted from the circuit has dramatic effect on the dynamic behavior of the converter. The inductor current becomes the input variable for feedback and the order of the whole circuit decreases by one. So in the case of capacitor filtering at the output the circuit has a single-pole open-loop transfer function. By using properly designed error amplifier the usual unpleasant ringing transient response is eliminated and the loop has a roll-off of -20dB/decade and associated 90^0 phase margin in the whole frequency range of interest [10].

Another desirable feature of the current-mode control is the inherent instantaneous - pulse-by-pulse - overload protection of the power switch. A suitable clamping of the control voltage (v_c) produces a well-defined, sharp current limiting characteristic. Also it makes very easy the operation of identical power stages in parallel, by controlling all circuits with the same error voltage. This automatically results in equal current sharing without any extra circuitry.

At last an interesting property of the current-mode control is the feasibility of applying input voltage/output current feed-forward. In this way transient responses in one or a few cycles of the switch can be easily achieved. Details of the theoretical background and example of practical implementation can be found in [10].

Constant-frequency operation of switching power converters is a desirable feature. Electromagnetic compatibility in a large electronic system often requires external synchronisation of the power supplies. Some commercial applications (e.g. in TV receivers) also need a rigid connection between the frequency of the power supply and the internal clock (e.g. horizontal time base). Design of the input and/or the output filter is also a lot more easier in the case of constant-frequency operation. And at last but not least the case of the already well known and proven design procedures for the inductive components (transformers, chokes) of the power circuit are available mostly for fixed frequency.

It can be seen from the foregoings that the most suitable type of current-mode control for general applications is the constant-frequency one. Unfortunately this version is particularly prone to instability. The possible modes of oscillation are: (a) open--feedback-loop oscillation above 50% duty ratio, (b) closed--feedback-loop oscillation at the first subharmonic of the clock frequency, its amplitude is a monotonous function of the ac loop gain, (c) closed-feedback-loop oscillation at the first or higher order subharmonic of the clock frequency, its appearence is a hysteretic function of the ac loop gain.

The paper is concerned with the explanation of the mechanism of the above mentioned oscillations and their conditions. The first one will be only briefly discussed because it is well understood and documented [5][6][8] and more attention will be paid to the other types of instability. The main goal of the authors is to provide an easy-to-understand picture about these phenomena and introduce analytical methods which are accurate enough for everyday use but do not assume an extensive computational background and detailed knowledge of selected topics of modern control theory.

2. OSCILLATION WITH OPEN FEEDBACK LOOP

If the duty ratio of a constant-frequency current-mode controlled converter is above 50%, any perturbation of the inductor current will increase according to geometric series. The quotient of the geometric series can be determined by the help of the current waveform of Fig.2. The change in the current minimum in one cycle is:

$$\Delta I_{m(n+1)} = - \frac{m_2}{m_1} \Delta I_{mn} \qquad (1)$$

or substituting the steady-state duty ratio (1):

$$\Delta I_{m(n+1)} = - \frac{D}{1-D} \Delta I_{mn} \qquad (2)$$

It is clear from (2) that if the absolute value of the duty ratio is larger than 50% the series of the current minimums will be divergent. The first reference of this fact can likely be found in [11]. It is interesting to note that this type of instability occurs similarly in any type of converters.

Deisch [5] proposed a solution to overcome this severe limitation of the constant-frequency operation. It is obvious from (1) that if the ratio of the slopes of the rising and falling part of inductor current is less than one stability is ensured. If an artificial ramp is added to the rising current so as to meet this condition proper operation can be maintaned above 50% duty ratio, too. The required time function can be derived as follows:

Let the magnitude of the rising current slope be normalised to the magnitude of the falling slope. In this case the condition of stability is:

$$\frac{1}{D} - 1 + m_{norm} = 1 \qquad (3)$$

where (1/D-1) is the normalised slope of the rising current and m_{norm} is the normalised slope of the artificial ramp function. From (3)

$$m_{norm} = 2 - \frac{1}{D}$$

In order to determine the time function itself the D=t/T substitution and solution of the resulting differential equation should be accomplished.

$$\frac{df_c(t)}{dt} = m_{norm}(t) = 2 - \frac{T}{t} \qquad (5)$$

From (5)

$$f_c(t) = 2t - T \ln \frac{t}{T} + C \qquad (6)$$

Taking the $f_c(T/2)=0$ boundary condition results

$$f_c(t) = T(2 \frac{t}{T} - \ln \frac{t}{T} - \ln 2e) \qquad (7)$$

where e is the base of natural logarithm.

Theoretically there is no need for compensation below 50% duty ratio. Substituting $f_c(t)$ by zero in this range provides the Deisch function as shown in [5]. Its waveform can be seen in Fig.3.

The implementation of this ramp function is not very easy. However good results can be achieved by simple approximations (e.g. portion of a sinewave, exponential function with positive exponent, integrated linear ramp or linear ramp, itself). The simplest way is to use linear ramp truncated below 50% [5] or linear ramp from the onset of the current increase [8][9]. This latter solution is a mixture of the traditional PWM control and the current-mode control. Detailed analysis of the dynamic behavior of this dual control can be found in [9].

It is worth to mention that without compensation the transient response to line, load or control signal step changes is oscillatory even below 50% duty ratio. The response can be improved by starting the compensating ramp before half of the period. This results in a better damped ringing in the choke current minimums.

3. CONTINUOUS SUBHARMONIC OSCILLATION

From Eq.2 it is obvious that any perturbation in the inductor current disappears as a damped oscillation at the first subharmonic of the clock frequency. This observation indicates that the converters under discussion are inclined to spurious oscillation at half of the clock frequency even in the stable duty ratio range. The tendency can be easily verified experimentally, too.

The subharmonic oscillation is unwanted for many reasons. Its presence increases the ripple voltage at the output, results in saturation of the push-pull transformers in certain converter topologies, causes electromagnetic compatibility problems, etc.

The beginning of this oscillation is closely related to the magnitude of the amplified and fed-back output ripple. Gradually increasing the ac gain of the error amplifier one can experience an oscillation at the first subharmonic of the clock with a gradually increasing amplitude. Decreasing the loop gain also decr-

eases the amplitude and at a well-defined gain value the oscillation stops.

The gain value where the oscillation starts coincides with the value of ceasing. So there is no hysteresis in the gain at the boundary of instability. This is in contrary to the other type of instability discussed in Section 4.

For the design engineer it is important to know what is the maximum usable ac gain. The higher the gain, the smaller the amplitude of the output transient response to sudden load or line changes. Therefore in order to obtain good transient response high gain should be used.

The main point in the describing function analysis is the following. The nonlinearity of the system (in our case the current-mode controlled power converter) is characterized by its amplitude and phase response to sinewave excitation. This response is the so-called describing function which is a multivariable function being dependent on the amplitude, phase and frequency of the input excitation.

The designer is interested in the gain only at the boundary of instability and at half of the clock frequency, i.e. the frequency and amplitude as input variables can be omitted. So the describing function should be determined at infinitesimal amplitude and at the first subharmonic frequency.

If the describing function is available the maximum usable gain can be calculated e.g. by the help of the widely used and easy-to-apply Bode criterion. The fed-back system is on the verge of oscillation if the phase shift of the loop is 2π and the overall loop gain is unity.

The detailed block schematic of the controller with injected subharmonic perturbation signal is shown in Fig.4. The describing function of the controller can be defined as the limit value of the ratio of the subharmonic current component of the current flowing - or being injected - towards the load (i_i) and the perturbation current (i_p). Infinitesimally small perturbation can be assumed because of the above mentioned reasons. So the magnitude of the describing function is:

$$|F(\varphi)| = \lim_{I_p \to 0} \frac{I_{i\ f/2}}{I_p} \qquad (8)$$

and the phase shift:

$$\text{arc } F(\varphi) = \lim_{I_p \to 0} (\text{arc } i_{i\ f/2} - \varphi) \qquad (9)$$

where

$i_{i\ f/2}$: the first subharmonic component of the injected current

$\varphi = \text{arc } i_p$: phase of the perturbation current

For the buck converter the injected current equals the inductor current (i_L) in the whole period, for the boost and other flyback converters it equals the inductor current during the off state of the period and is zero during the on state.

The conditions of oscillation can be written as:

$$\text{arc } F(\varphi) + \text{arc } Z_L(j\pi f) = \pi \qquad (10)$$

and

$$|F(\varphi)||Z_L(j\pi f)|g = 1 \qquad (11)$$

Here

$Z_L(j\pi f)$: impedance of the load at the first subharmonic of the clock frequency.

$g = \frac{R_2}{R_1 R}$: total transconductance of the current-mode controller (including the ac gain of the error amplifier), frequency independent gain of the error amplifier at f/2 is assumed.

Details of the derivation of $F(\varphi)$ are submitted in the Appendix. In the usual case of capacitive filtering at the output relatively simple expressions can be obtained for the maximum allowable transconductance. These expressions are shown for the buck and boost regulators in Table 1.

TABLE 1. MAXIMUM ALLOWABLE TRANSCONDUCTANCE

Buck $\quad g \leq \dfrac{1-2D}{\frac{4T}{\pi^2 C} - R_c}$

Boost $\quad g \leq \dfrac{1-2D}{\frac{4}{\pi}\sin\frac{\pi}{2}(1-D)\left[R_c \sin\pi(1+\frac{D}{2}) - \frac{T}{\pi C}\cos\pi(1+\frac{D}{2})\right] + \frac{D(1-D)T}{2C} + \frac{LI_0}{V_0 C(1-D)} - DR_c}$

R_c : equivalent series resistance of the output filter capacitor C

D : steady-state duty ratio

T : period time of the clock signal

L : choke inductance

I_0 : load current

V_0 : regulated output voltage

At the derivations second-order effects (transistor or diode forward voltage drops, winding resistance, switching delay in the controller and/or power transistor) were neglected. The accuracy of the expressions is illustrated by the experimental data shown in Section 5.

It is interesting to note that both types of converters are unconditionally stable - at least from the point of view of continuous subharmonic oscillation - above a certain $R_c C$ product.

For the buck regulator this product is independent of all circuit parameters, except the clock frequency and the circuit is stable if

$$R_c C > \frac{4T}{\pi^2} \tag{12}$$

For the boost regulator the value of this product is a function of the duty ratio, choke inductance and output dc voltage/current.

4. HYSTERETIC SUBHARMONIC OSCILLATION

The characteristic waveforms at the input of the current comparator are shown in Fig.5 for the case of the boost converter. If the amplified and fed-back output ripple ($-g\hat{v}_o$) is below the choke current at the end of the period the R-S flip-flop cannot change state and the conduction of the power switch in the next period will be missing. This results in a particular subharmonic oscillation. For the buck converter this type of oscillation is practically impossible because here the fed-back ripple is always above the choke current in normal operation.

Decreasing the gain of the loop stops the oscillation at a lower gain value. The condition of ceasing can be determined by the waveforms of Fig.6. If the instantaneous value of the ripple at the moment of the arrival of the first clock signal in the off state is below the choke current the flip-flop cannot change state. However the oscillation terminates if the ripple crosses the choke current before the next clock pulse.

The starting condition of the oscillation is:

$$g\hat{v}_{op\text{-}p} \geq I_M - I_m \tag{13}$$

The ceasing condition of the oscillation is:

$$g\Delta\hat{v}'_o[(1-2D)T] \leq \Delta i'_L[(1-2D)T] \tag{14}$$

Here the upper comma indicates the state of subharmonic oscillation. Δ refers to the difference from I'_M.

Substituting the known expressions for $\hat{v}_o$ and i_L results in rather simple inequalities (Table 2).

Hysteretic subharmonic oscillation can arise if the difference between the starting and ceasing values of transconductances is positive. This condition is fulfilled almost in the entire duty-ratio range of interest.

It is wortn to note that if the clock pulse is able to trigger the flip-flop even if the comparator output is in the inhibiting state the conditions for the oscillation change. This is not the case for the test circuits introduced in Section 5.

TABLE 2. TRANSCONDUCTANCES FOR STARTING AND CEASING SUBHARMONIC OSCILLATION OF THE BOOST CONVERTER

Starting value of transconductance	$g \geq \dfrac{1}{\dfrac{R_c L I_0}{V_0 T D (1-D)^2} + \dfrac{R_c}{2} + \dfrac{L I_0}{V_0 C (1-D)}}$
Ceasing value of transconductance	$g \leq \dfrac{1}{\dfrac{R_c L I_0}{V_0 T D (1-D)(1-2D)} + \dfrac{R_c (1-D)}{1-2D} + \dfrac{L I_0}{V_0 C (1-D)} + \dfrac{T}{2C}}$

5. EXPERIMENTAL RESULTS

Fig.7 and Fig.8 show the simplified circuit schematics of a buck and a boost regulator. The circuits were built only for test purposes - to measure the boundary of instability at different operating conditions. The clock pulse was 200 nsec wide which was long enough to trigger the R-S flip-flop whenever it was allowed by the current comparator but it was too short to change the state of the power switch. The transconductance was controlled by the potentiometer R_p in the feedback circuit of the operational amplifier. The output capacitor was changed in order to simulate real operating differences.

Results of the measurements and the calculated limits of the transconductances at the verge of continuous subharmonic oscillation are shown for the buck regulator in Fig.9. The measurements were carried out with the same capacitance and with two different ESR values of the filter capacitor. The close correspondence between the experimental and computed data justifies the application of the method of describing function analysis.

Measurements were made for the boost regulator with three different capacitance and ESR combinations. The results are shown in Fig.10. In the diagrams the calculated starting and ceasing values for hysteretic oscillation and limits of continuous subharmonic oscillation are also plotted.

As it can be seen there is a rather good correspondence here, too, but due to the inherent inaccuracies of the describing function analysis method at smaller degree of filtering the deviation between the predicted and experimental data are larger than in the case of the buck regulator.

According to the calculations the C=2200μF and R_c=0.47 ohm combination provides unconditional stability from the viewpoint of continuous oscillation. This was well demonstrated by the test circuit which showed only hysteretic oscillation close to the predicted boundaries.

In the case of C=30 µF and R_C=50 mohm the curve of the starting value of the hysteretic oscillation is not shown completely. This curve lies outside the diagram with a peak value of 1.64 at D=0.12 and declines gradually to 1.06 at D=0.5.

6. REFERENCES

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APPENDIX: CALCULATION OF SUBHARMONIC DESCRIBING FUNCTION WITH FED-BACK OUTPUT RIPPLE

The subharmonic describing function is defined as the ratio of input and output subharmonic current amplitudes of the current-mode controlled converters (see Fig.11).

The following assumptions are made:

- small perturbation: $i_p(t) = I_p \sin(\pi f t - \varphi)$; $I_p \ll I_M$
- ΔI_m, ΔI_M, ΔD have the same magnitude but opposite sign at successive periods
- $i_p(DT) \approx i_p[(D+\Delta D)T]$
- $m_{c1}(DT) \approx m_{c1}[(D+\Delta D)T]$
- $m_{c2}(DT) \approx m_{c2}[(D+\Delta D)T]$

Four basic equations can be derived from Fig.12 which shows a short time interval around the turn-off moment.

$$\Delta I_m + \Delta I_M = m_1 \Delta DT \tag{15}$$

$$\Delta I_m - \Delta I_M = m_2 \Delta DT \tag{16}$$

$$\Delta I_c + i_p(DT) - \Delta I_M = m_{c1} \Delta DT \tag{17}$$

$$\Delta I_c - i_p(DT) + \Delta I_M = m_{c2} \Delta DT \tag{18}$$

Eliminating ΔI_M, ΔDT and ΔI_c from Eqs.15-18 results:

$$\Delta I_m = i_p(DT) \frac{m_1 + m_2}{m_1 - m_2 + m_{c1} - m_{c2}} \tag{19}$$

The subharmonic content of the injected current can be calculated by the help of Fig.13. The peak-to-peak current difference is $2\Delta I_m$ for both types of regulators.

For the buck regulator the first-order subharmonic current component is:

$$i_{f/2} = \frac{2}{\pi} 2\Delta I_m \sin(\frac{\pi}{T} t - \pi D) \qquad (20)$$

Substituting (19) into (20) and taking into account that the phase of $i_{f/2}$ is constant independently of the phase of perturbation:

$$F_{buck} = \frac{4}{\pi} \sin(\pi D-\varphi) \frac{m_1+m_2}{m_1-m_2+m_{c1}-m_{c2}} e^{j(\pi D-\varphi)} \qquad (21)$$

Let the output be filtered by a capacitor with given ESR and C values. In this case the stability conditions can be written in a simplified form as shown subsequently.

The equation of phase condition is:

$$\text{arc } Z_L + \text{arc } F(\varphi) + \pi = 2k\pi \quad (k=0,1,2..) \qquad (22)$$

From (21) and (22):

$$\varphi = \text{arc } Z_L - \pi D + \pi(1-2k) \qquad (23)$$

Let us write (23) into (21). The product of $|Z_L|$ and the term $|\sin(\pi D-\varphi)|$ gives:

$$|Z_L||\sin(\pi D-\varphi)| = \frac{T}{\pi C} \qquad (24)$$

For the boost regulator the first-order subharmonic content of the difference current is:

$$i_{f/2} = \frac{2}{\pi} 2\Delta I_m \sin(\pi D-\varphi)\sin[\frac{\pi}{2}(1-D)]\sin\pi(\frac{t}{T}-\frac{D}{2}) \qquad (25)$$

With the same considerations as in the case of the buck regulator one can obtain the describing function as

$$F_{boost} = \frac{4}{\pi} \sin(\pi D-\varphi)\sin[\frac{\pi}{2}(1-D)] \frac{m_1+m_2}{m_1-m_2-m_{c1}-m_{c2}} e^{j(\pi\frac{D}{2}-\varphi)} \qquad (26)$$

Note that in the denominator m_{c1} is of opposite sign as for the case of the buck regulator because here during the conducting period the output voltage decreases.

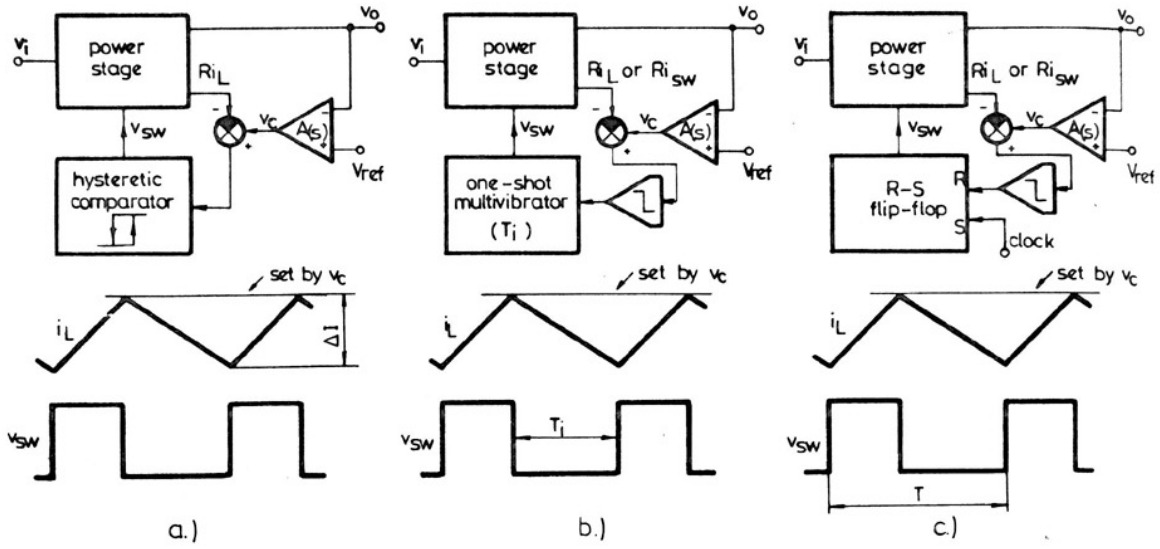

Fig.1 Three current-mode controlling techniques: (a) hysteretic, (b) constant off-time, (c) constant frequency.

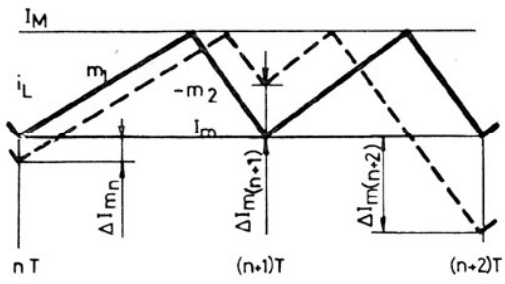

Fig.2 Growth of perturbation above 50% duty ratio.

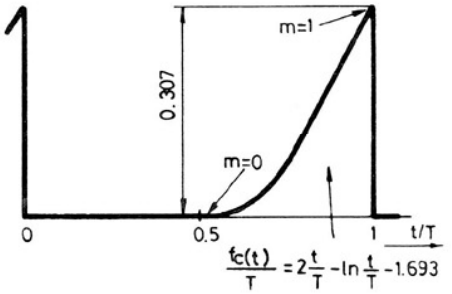

Fig.3 The Deisch-function.

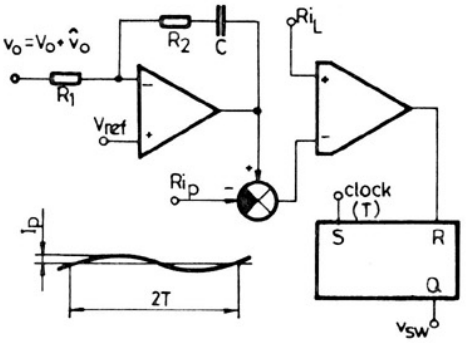

Fig.4 Current-mode controller with first subharmonic perturbation.

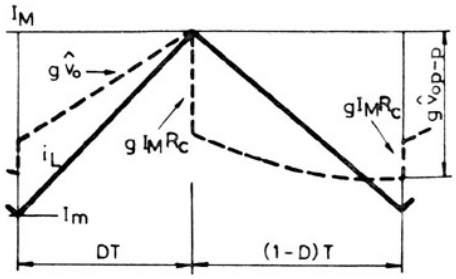

Fig.5 Current comparator waveforms of the boost converter.

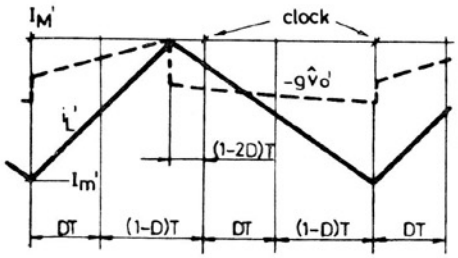

Fig.6 Current comparator waveforms in the state of hysteretic oscillation.

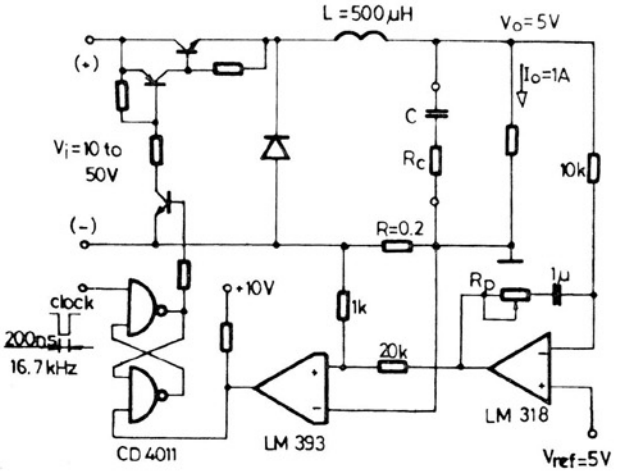

Fig.7 Buck regulator test circuit.

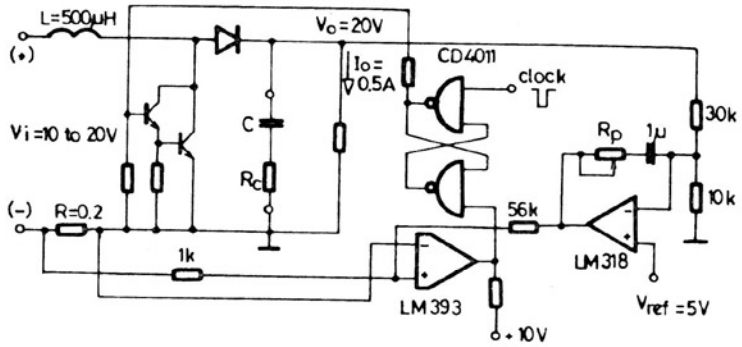

Fig.8 Boost regulator test circuit.

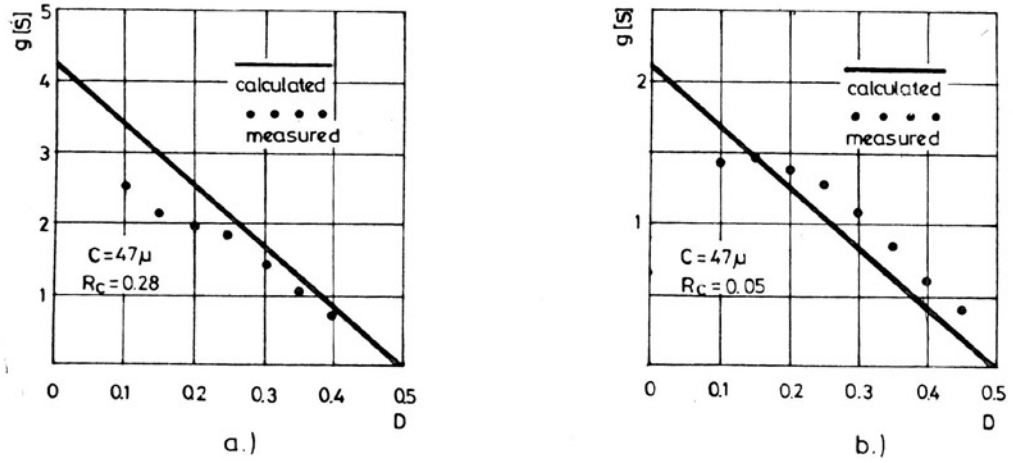

Fig.9 Calculated and measured transconductances of the buck regulator at the boundary of continuous subharmonic oscillation.

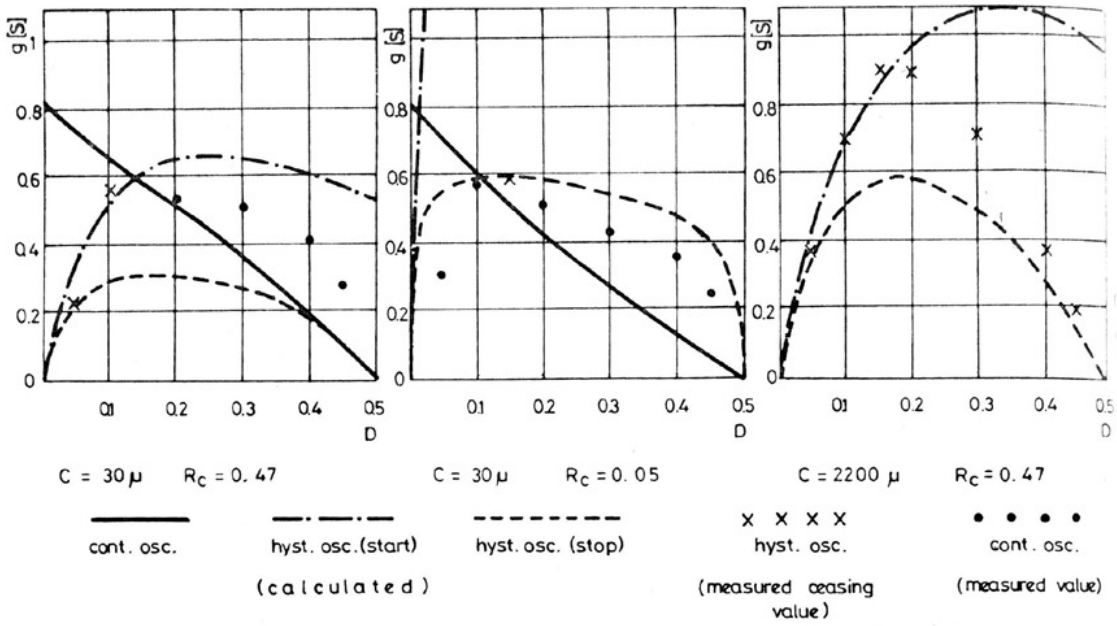

Fig.10 Calculated and measured transconductances for the boost regulator.

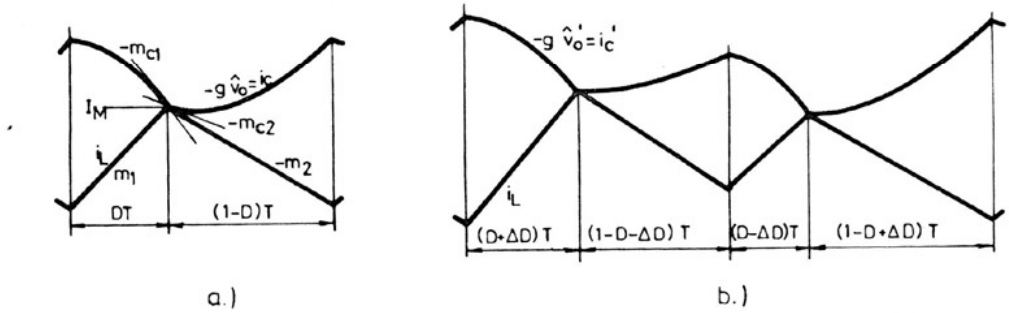

Fig.11 Current waveforms of the buck regulator in stable state (a) and in the state of continuous subharmonic oscillation (b).

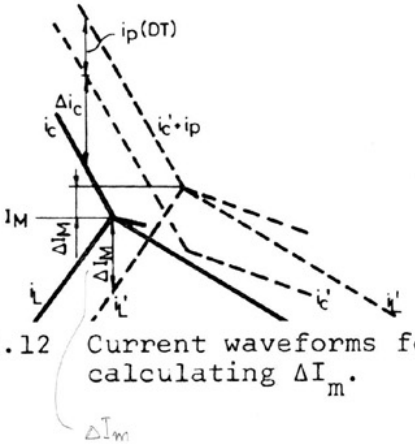

Fig.12 Current waveforms for calculating ΔI_m.

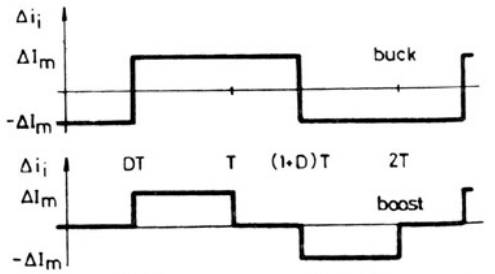

Fig.13 Difference of injected currents between stable state and state of subharmonic oscillation.