DesignCon East 2005

A Black-Box Frequency Dependent Model of Capacitors for Frequency Domain Simulations

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Abstract

There is an ongoing interest in refining the simulation models for passive components in electronic circuits. For simple analyses, bypass capacitors are modeled by a series C-R-L equivalent network. To capture the frequency dependency of the circuit parameters, more complex equivalent circuits can be used: ladder L-R networks to model the frequency dependent inductance and resistance and/or C-R networks to model the frequency dependent capacitance. These equivalent circuits have the advantage of being compatible with both time-domain and frequency domain SPICE simulations, but the optimum topology of the equivalent circuit may depend on the type and construction of capacitor. First, the paper shows the current distributions inside MLCC parts simulated with a bedspring model at various frequencies, which give insight to the expected frequency dependency of resistance and inductance. Second, we show measured data on stacked capacitors, illustrating the vertical resonances in tall MLCC parts. Third, the paper introduces a black-box approach to model the capacitance, resistance and inductance of bypass capacitors separately with a fixed set of approximation functions, where the parameters of the formulas can be obtained semi-automatically from measured data through curve fitting.

Author Biography

Istvan Novak is signal-integrity senior staff engineer at SUN Microsystems, Inc. Besides signal-integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

I. Introduction: Present modeling options

When considering the parasitics of bypass capacitors, a widely used simple model is a series C-R-L network, where C is the capacitance of the part, R is the Equivalent Series Resistance (ESR) and L is the Equivalent Series Inductance (ESL), as shown in Figure 1. In its simple form, C, ESR and ESL are assumed to be frequency independent constants. However, measured data indicates [1] that all three of these parameters are eventually frequency dependent and furthermore may be inter-related through the application geometry.

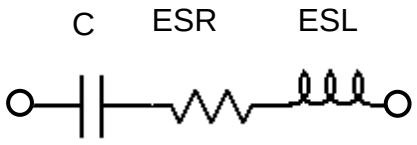


Figure 1. Simple RLC equivalent circuit of a capacitor.

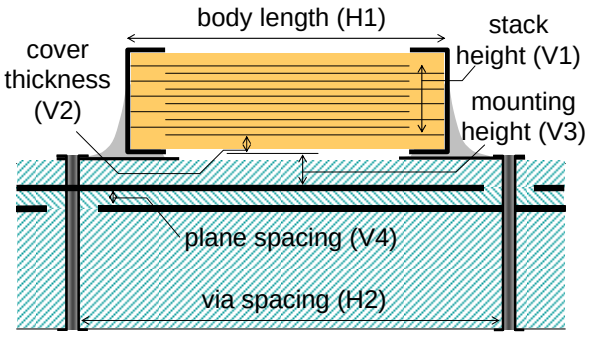


Figure 2. Vertical cross section of an MLCC mounted to PCB planes.

The capacitance may be frequency dependent, primarily because of dielectric losses [2].

ESR is the result of transforming the parallel dielectric losses and series conductive losses into a single series resistance value. As long as tangent delta of the dielectric material is constant, the parallel loss resistance drops inversely with frequency. The series resistance of the part comes from the terminals and conductive layers on the dielectric sheet(s). Apart of bulk constructions, like tantalum brick capacitors and alike, the conductive material and terminals are thin enough that in the frequency range of interest their thickness is less than the skin depth, and therefore the AC resistance contributions of the plates themselves do not vary much with frequency. Overall ESR still varies at high frequencies, due to non-uniform current distribution in the plates [4]

Inductance depends both on the internal construction of the part and the external geometry forming the closed current loop. As illustrated in Figure 3 for the case of a Multi-Layer Ceramic Capacitor (MLCC) attached to a pair of planes on a PCB, the low-frequency inductance loop spreads vertically through the vertical stack of capacitor plates, whereas at high frequencies the loop shrinks to the lower capacitor plates and upper PCB plane. In this simplistic high-frequency current-loop model we usually neglect the small opening on the top PCB plane around the via connection.

When extracting capacitor parameters from measured data, we face a further complication: ESR is simply the real part of the measured impedance (after the proper calibration and/or deembedding process), but the capacitive and inductive reactances show up in a superimposed way in the imaginary part of the measured impedance. If capacitance and inductance were frequency independent, extracting them from the imaginary part of measured impedance would be easy. Because the capacitive and inductive reactances change with frequency in the opposite way, we know that at frequencies much below the Series Resonance Frequency (SRF) the inductive reactance is negligible and from the measured reactance we can calculate the capacitance. Similarly from a measured reactance value at a frequency much above SRF we could calculate the inductance. This approach is assumed for instance in

[3] and [4]. With relatively strong frequency dependency of capacitance and/or inductance, which is the case of tall capacitor stacks with lossy dielectrics and aggressive mounting, using a low-frequency capacitance and a high-frequency inductance can not uniquely resolve the frequency dependent capacitance and inductance values around SRF. One step further is to iteratively approximate the capacitance and inductance close to SRF and use those (constant) values to extract the frequency dependent capacitance and inductance curves [5]. This improves accuracy and the range of validity for the extracted capacitance and inductance curves, but unless we have further data points or constraints, we cannot uniquely resolve the two unknowns, C(f) and ESL(f), from one data point of Im{Z(f)}.

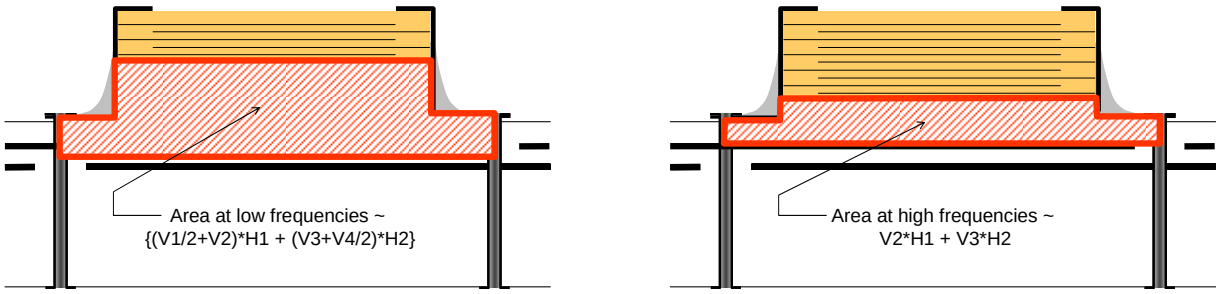


Figure 3. Illustration of approximate current-loop shapes and cross-section areas. On the left: low-frequency model; on the right; high-frequency model.

Instead of trying to blindly extract the parameters from measured data, more sophisticated equivalent circuits can also be used to fit the measured data on the model. Equivalent circuits composed of frequency independent resistors, capacitors and inductors unconditionally guarantee causality and easy compatibility to circuit simulators. For frequency dependent capacitance and ESR of bulk capacitors, [6] suggests a composite RLC network. To capture the frequency dependent ESR and ESL of MLCCs, [7] uses a resonant ladder network, while [8] proposes a transmission-line model.

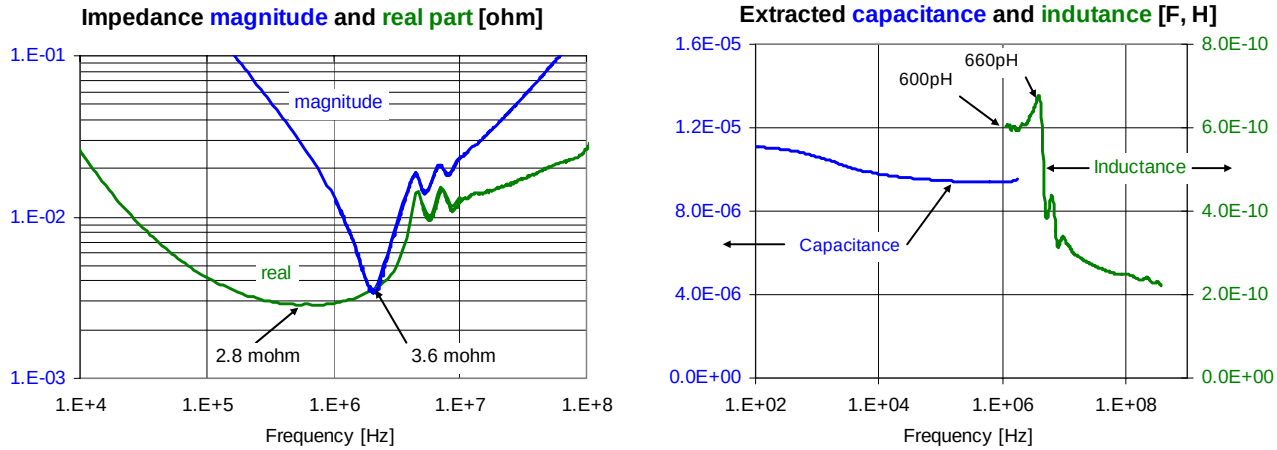


Figure 4. Measured impedance magnitude of a 10uF 0508 MLCC with the real part of the impedance (on the left), and extracted capacitance and inductance versus frequency (on the right).

For MLCC parts, it is customary to assume that the capacitive and inductive currents balance themselves at SRF and therefore at that frequency the current uniformly penetrates all plates and for this reason the lowest ESR value occurs at SRF. Similarly, it is usually assumed that inductance monotonically drops from its low-frequency value towards the high-frequency inductance.

Figure 4 shows the measured impedance and the extracted C(f), ESR(f) and ESL(f) values for a 10uF 0508 reverse-geometry MLCC part mounted on a small fixture.

In contrast to usual expectations, the minimum of the impedance real part is not at SRF: at 600kHz ESR is 2.8 milliohms; whereas at the 2.1MHz SRF the ESR reading is 3.6 milliohms. Moreover, the ESL(f) value extracted according to the procedure in [5] results in 600pH at SRF, but the inductance first increases with frequency, reaching a 660pH peak at 4.2MHz before it starts decreasing. Is this due to measurement errors or a deficiency in the extraction procedure, or really ESR and ESL behave contrary to common assumptions? This will be looked at in the next section.

II. Bedspring capacitor model

To look into the frequency dependency of the parameters of an MLCC part, a simplified two-dimensional bedspring model was constructed with ten capacitor plates and ten sections of each capacitor plates and dielectrics. Figure 5 shows the partial schematics of the bedspring model.

If in the physical design we assume N capacitor plates, they are grouped into ten horizontal equivalent circuits, each representing N/10 plates. The conductive plates are modeled by their series resistances and inductances. To capture the resonances both vertically and horizontally, each model of capacitor-plate group is further divided horizontally into ten segments. Each segment is represented by an Rp resistance and Lp inductance. The Rp resistor represents the physical resistance of the plate, but it was also used to ‘sense’ and measure the current in SPICE. Half of the plates connect to the left capacitor terminal, the other half of plates connect to the right terminal. The last sections of plates, which connect to the terminals, do not have facing counterparts of opposite-polarity plates. These end sections are modeled by using one more horizontal segment of Rp resistance and Lp inductance, though if geometry warrants it, these parameters can easily be adjusted to reflect the actual percentages of plates in the open dielectric region. The capacitance of the dielectric material between the plates is represented by a uniform network of capacitors with values of C, connecting each adjacent vertical node of the plates. In the SPICE sub circuits these capacitors had two additional elements. Each capacitor had a parallel resistor to represent optional dielectric losses and a very small series resistance to ‘sense’ and measure current (though since not necessarily needed to represent series losses, which we usually neglect in the dielectrics, for this purpose independent voltage sources could also be used). To increase clarity, these additional two elements are omitted from the partial schematics of Figure 5. The vertical end terminals are modeled by series Rt resistances and Lt inductances between every other plates, which connect to the terminal. The external connections, pads and vias are modeled by the series Rc and Lc elements. Note that the internal construction of MLCC parts is nominally symmetrical, and therefore what becomes ‘lower’ capacitor plate, being close to the return-path plane in the PCB, is determined solely where the Rc Lc elements are connected in the model.

SPICE AC simulations were run on the model with various parameter combinations, and the current was printed in each horizontal and vertical segment. The current magnitudes on the plates and in the dielectrics were plotted at various frequencies. Note that with the bedspring model we can achieve arbitrary geometrical resolution of the capacitor construction. One could construct a model where each

capacitor plate had its own entry, and each plate could be divided up along its length to many more segments. To understand the current distribution versus frequency behavior of the part, this ultimate level of detail is not necessary, nor is it practical when the number of plates is possibly many hundreds. Even this simplified model of Figure 5 is too complex to use for Power Distribution Network simulations, where we may need many of these models hooked up to the PCB. The bedspring model, however, provides a good insight into the variations of current distribution at different frequencies.

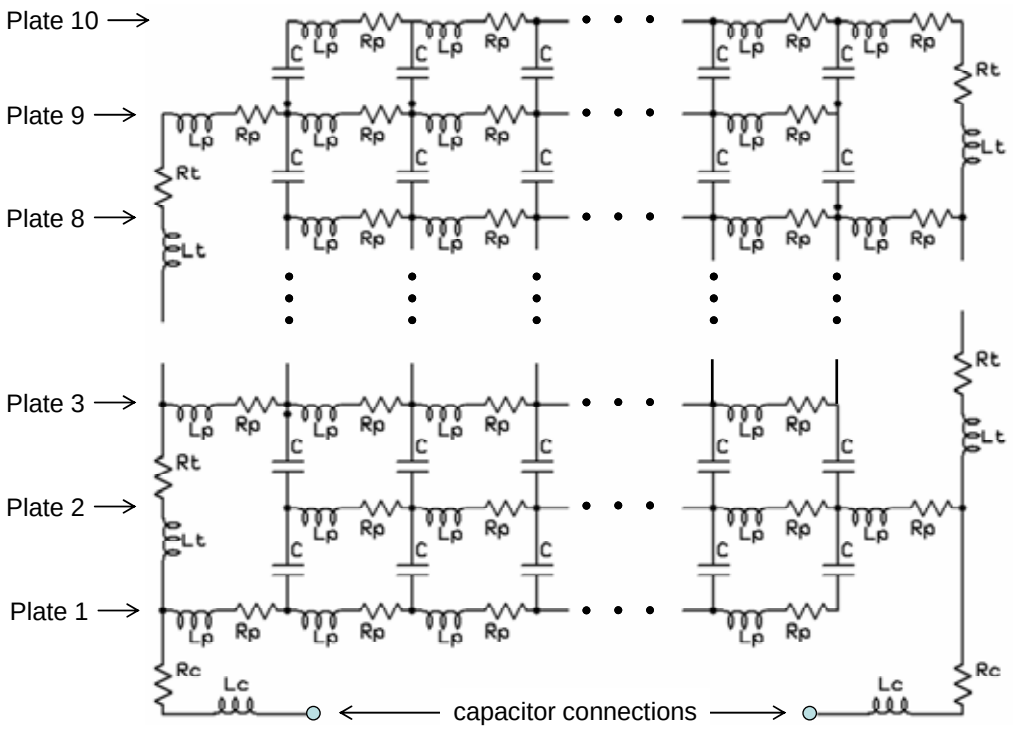


Figure 5. Partial schematics of the bedspring capacitor model. The model consists of ten capacitor plates, 1 through 10. The lowest capacitor plate, connecting to the PCB, is Plate 1. Plates 1, 3, 5, 7 and 9 are connected to the left terminal. Plates 2, 4, 6, 8 and 10 are connected to the right terminal. Each capacitor plate is divided into ten equal segments (plus an end piece), represented by series RL networks. At each internal plate node, a capacitor represents the dielectric material.

For sake of simplicity and clarity, the simulation results shown here do not assume any dielectric losses, and (therefore) the capacitance of the insulating material is assumed to be frequency independent.

Figure 6 shows the simulated impedance magnitude and impedance real part of the bedspring model with the particular parameter values shown on the right. Note that the purpose of this model and series of simulations was not to correlate to any particular measured results. Though it could have been done, it was clear that regardless of the correlation result, this model is too complex to be used in actual simulations of PDNs. Since the sole purpose of the model was to study horizontal and vertical resonances in the structure, a series of one-dimensional parameter sweeps were performed: the Rp, Lp, Rt, Lt, Rc and Lc values were stepped through a large range to see their effects on the impedance curve and current distribution (note that C only scales the frequency axis). Of the many simulated parameter combinations, the one shown in Figure 6 represents a case, where across the one decade below and above SRF, we can follow the gradual build-up of both vertical and horizontal resonances and can identify and follow key trends of current distribution variations.

With the selected parameters, the impedance magnitude curve shows the familiar V shape, and it also shows strong secondary resonances, characteristic to tall stacks of MLCCs mounted with low-inductance via geometry. SRF is approximately 10MHz, and the first parallel resonance occurs at 22MHz. The impedance real part already confirms the measured trend shown in Figure 4: there is a visible (though small) increase of the resistance by the time we get to SRF. Note that at lower frequencies, unlike in Figure 4, the impedance real part flattens out instead of increasing again; this is due to the fact that we assumed lossless dielectrics for this simulation.

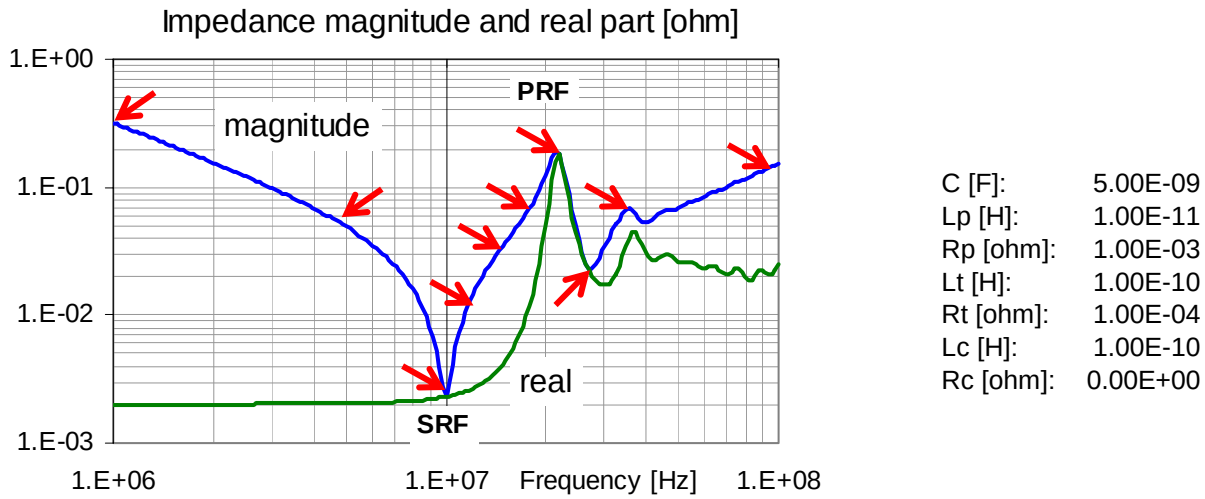


Figure 6. Simulated impedance magnitude and impedance real part at the capacitor connections terminals of the circuit shown in Figure 5. Circuit parameter values for Figure 5 are shown on the right.

Figure 6 has ten arrows placed along the magnitude curve. These arrows show the frequency points, where Figures 8 through 17 illustrate the current distributions along the capacitor plates and in the dielectrics. The selected frequencies were:

- 1MHz, SRF/10
- 5MHz, one octave below SRF
- 10MHz, SRF
- 12.3MHz, slightly above SRF
- 15.5MHz, halfway between SRF and PRF
- 17.4MHz, slightly below PRF
- 22MHz, PRF
- 27.5MHz; frequency of the second minimum
- 35MHz, frequency of second maximum
- 100MHz, ten times SRF

To help to interpret the current-distribution charts, Figure 7 shows the footprints of the capacitor-plate charts and dielectric-current charts together with a sketch of a PCB, which defines the orientation of the capacitor plates. The PCB is shown only to define where on the current-distribution charts the lower and upper capacitor plates are, otherwise the board was not included in the simulation. Figures 8 through 17 show the current distributions with the same orientation as shown in Figure 7. In these

figures, the lower-plate to right-terminal joint is at the front corner, the upper-plate to left-terminal joint is at the top corner. The current magnitudes along the conductive capacitor plates are shown on the left graphs; the current magnitudes in the dielectric cells are shown on the right graphs. Note the size difference between the left and right graphs. The left graphs plot 10 x 10 arrays, representing the ten capacitor plates, with ten segments on each plate. The right graphs plot 11 x 9 arrays, representing the nine layers of eleven dielectric columns between the adjacent capacitor plates. The unit for all vertical axes on these plots is Ampere.

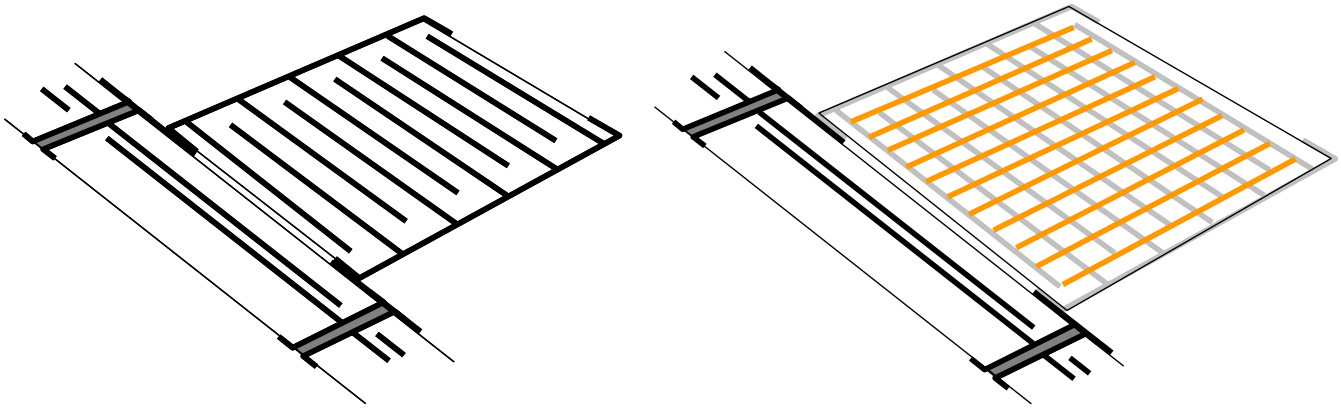


Figure 7. Sketches showing the capacitor plates and dielectric sections together with the PCB connection. The orientation of plates and dielectric segments is the same as the orientation on the following current-distribution plots.

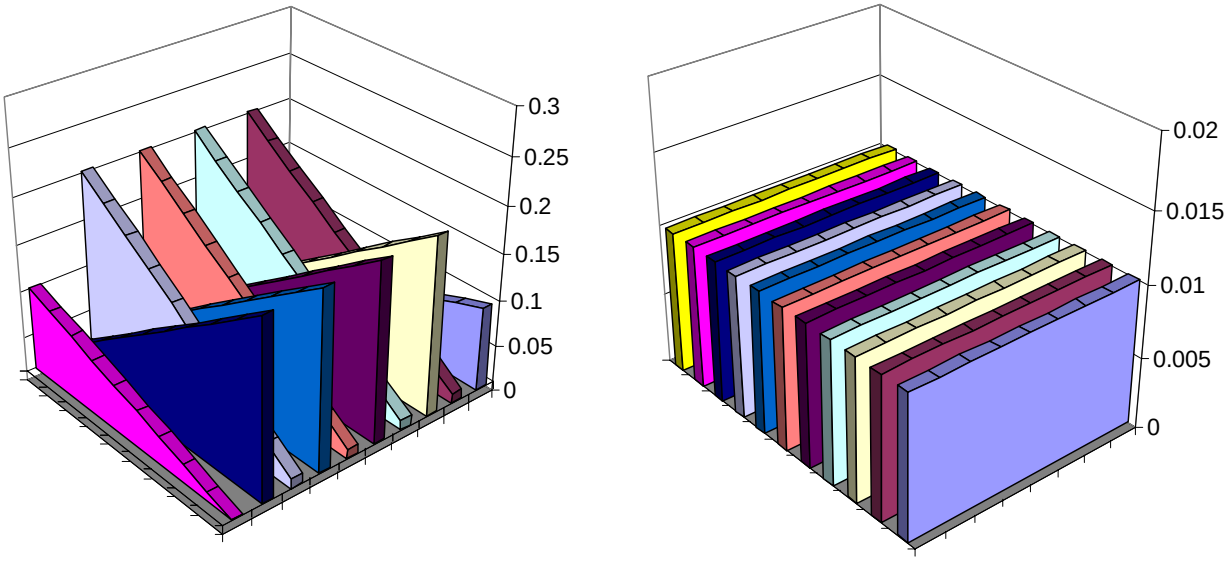


Figure 8. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 1MHz.

Figure 8 shows the current distribution at 1MHz, ten times below SRF. The current distribution in the dielectrics on the right shows a uniform distribution. We have a total of 99 dielectric cells in the model, and the 1A test current is evenly distributed, each dielectric cell carrying 1/99A at low frequencies. The

current distribution on the left is also uniform, but on the capacitor plates this shows up differently. We have five capacitor plates in the model connected to the left terminal, and five plates connected to the right terminal. The current enters the plates from the terminals, and it decreases linearly with distance as we move along the plate toward its open end, where the current becomes zero. In each horizontal segment the current becomes smaller due to displacement current 'leaking' into the dielectric cells. This creates the interleaved triangle-shaped current profiles shown on this figure. Note also that in a symmetrical-plate stack, the bottom and top plates carry only half the current compared to plates inside the stack, because the outside plates have dielectric only on one of their sides where current could enter or exit the plates. If we sum up the currents in the five plates at the left or at the right of the plot, this adds up still just to 0.91A. This is because the plot does not include the currents in the end pieces of the plates; the first segment where the current is shown along the plate is already after the first of the eleven capacitors. Each capacitor carries 1/11 part or 9% of the current entering the plate.

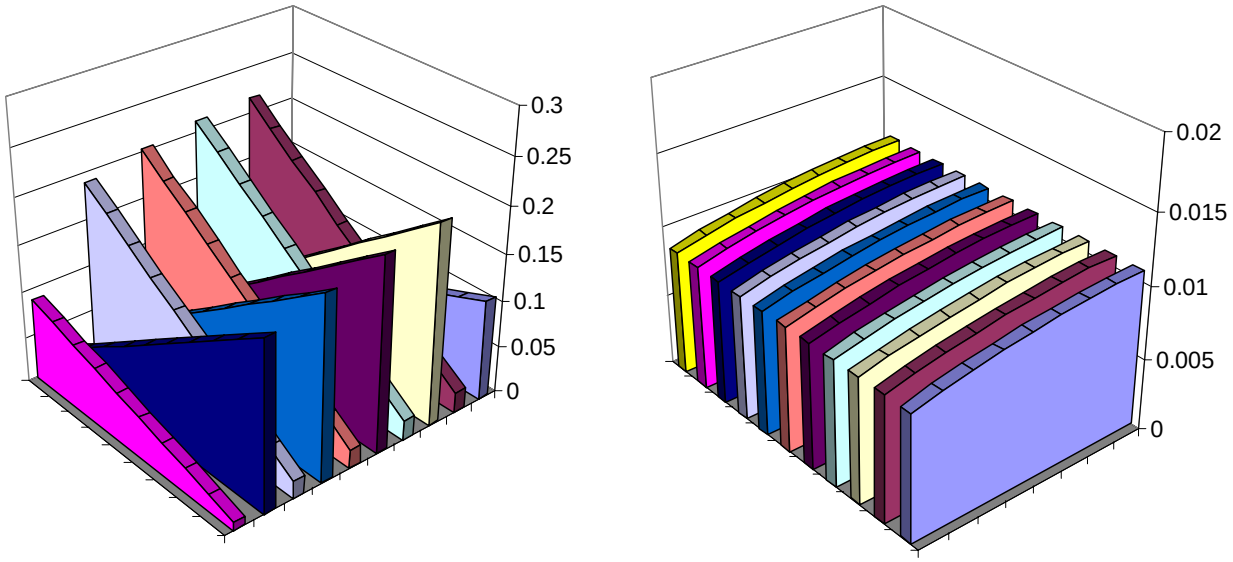


Figure 9. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 5MHz frequency.

Figure 9 shows the current distribution at 5MHz, one octave below SRF. At this frequency the distribution of the dielectric current is already not uniform. The sum of current magnitudes over the dielectric cells is still 1.0000 A, but there is clearly more current in the dielectrics towards the top plates and less current towards the lower plates. This is also visible if we compare closely the left-hand charts of Figures 8 and 9; current entering/exiting the lower plates is slightly less at 5MHz. This changing current distribution starting way below SRF tells us that the inductance corresponding to the particular current distribution already may start to change; in fact it may increase, since more current flows further away from the return path. The current distribution varies close to linear with elevation within the stack, and therefore ESR does not yet increase noticeably: the fact that less current flows on the lower plates gets balanced by the higher current in the upper plates.

Figure 10 shows the current distribution at SRF. At this frequency the current magnitude around the bottom plates is already four times lower than the current around the upper plates. This clearly defies the conventional assumption that at SRF the capacitive and inductive currents balance in a way that

current fills the capacitor plates and dielectrics uniformly. The current variation with elevation within the plate stack starts showing signs of nonlinearity; the center of gravity of current flow moved upwards. This explains that at the series resonance frequency ESR is already higher (2.36 milliohms) than the low-frequency value (2 milliohms). The sum of current magnitudes in the 99 dielectric cells starts rising; the sum at this frequency is 1.0006 A.

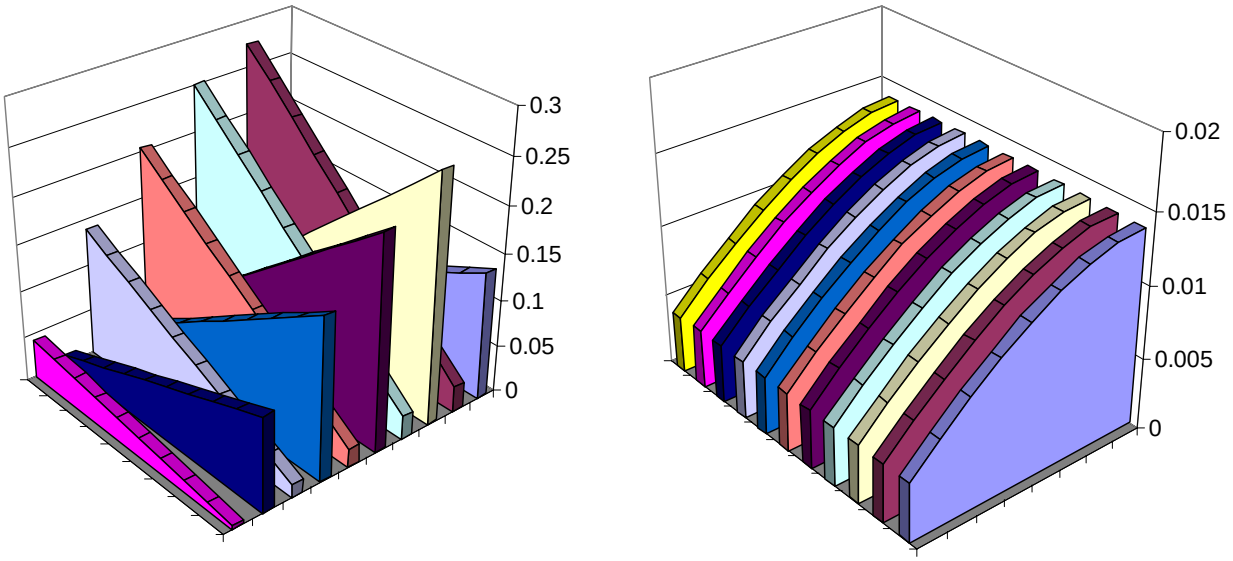


Figure 10. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at the 10MHz Series Resonance Frequency.

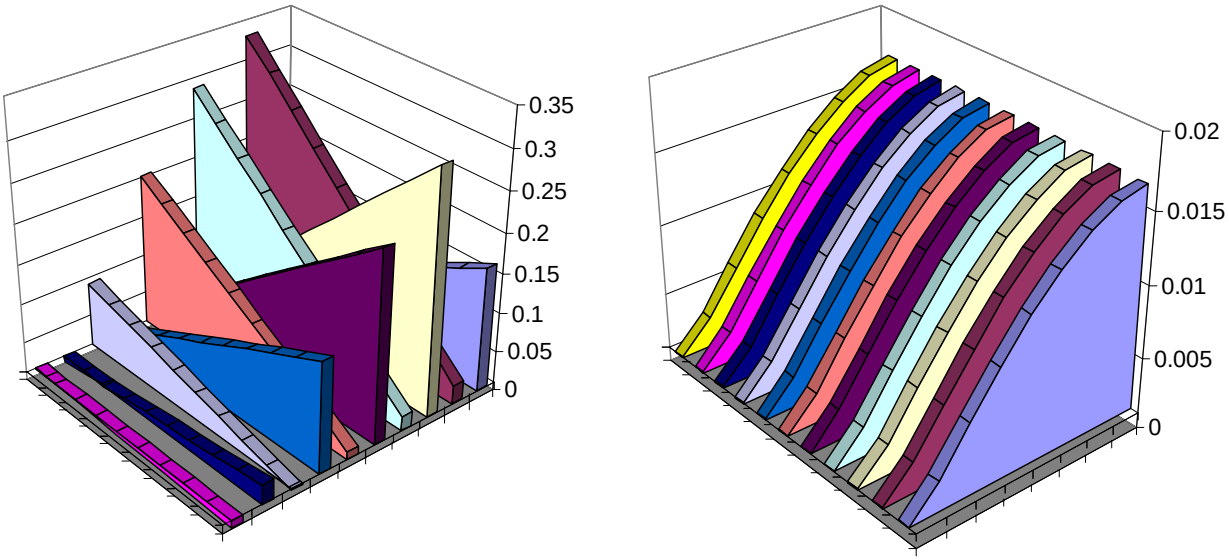


Figure 11. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 12.3MHz frequency.

Figure 11 shows the current distribution at 12.3MHz, one third on the way between the series resonance frequency and first parallel resonance frequency. At this frequency we can observe the build-up of a full

vertical resonance: current on the lower plates (close to the return path) is practically zero, and we see the characteristic one-quarter sine wave current-distribution shape vertically in the dielectrics. The vertical distribution of current also becomes strongly nonlinear, which explains the start of the sharp rise in ESR (see Figure 6). The sum of current magnitudes in the dielectric cells is 1.0147 A.

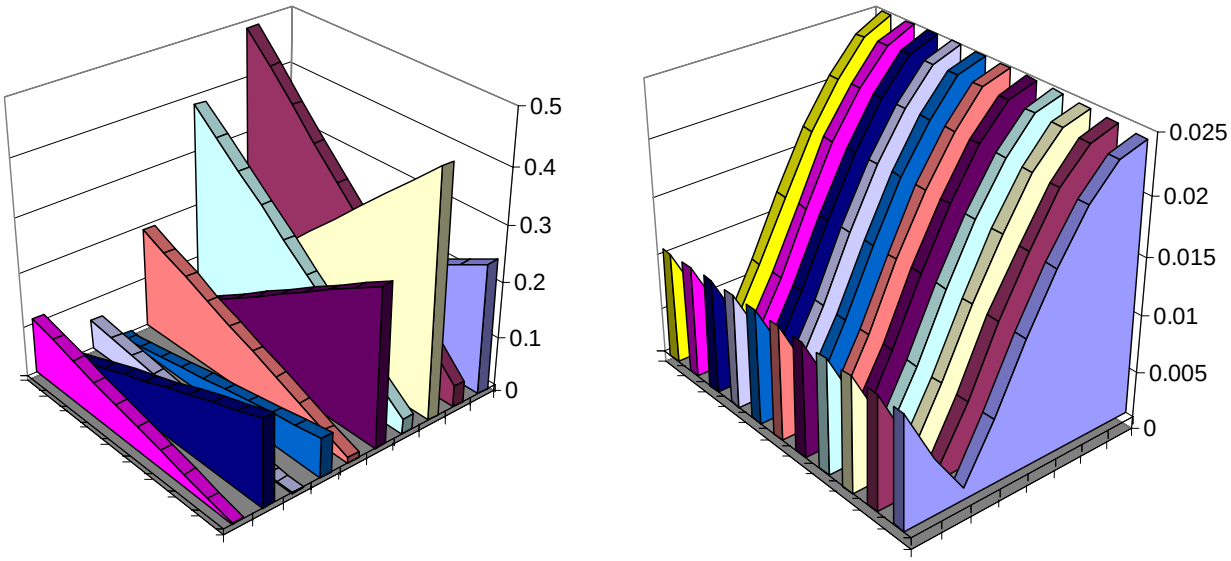


Figure 12. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 15.5MHz frequency.

Figure 12 shows the current distribution at 15.5MHz, approximately halfway between SRF and PRF. The minimum line in the current distribution in the dielectrics has moved from the bottom plates further upwards in the stack. Note also that the resonance in the distributed LC circuit amplifies the current magnitude: the sum of current magnitudes over the 99 dielectric cells rose to 1.3754 A, and therefore the vertical scales of both charts had to be increased (compared to earlier figures) to fit the data.

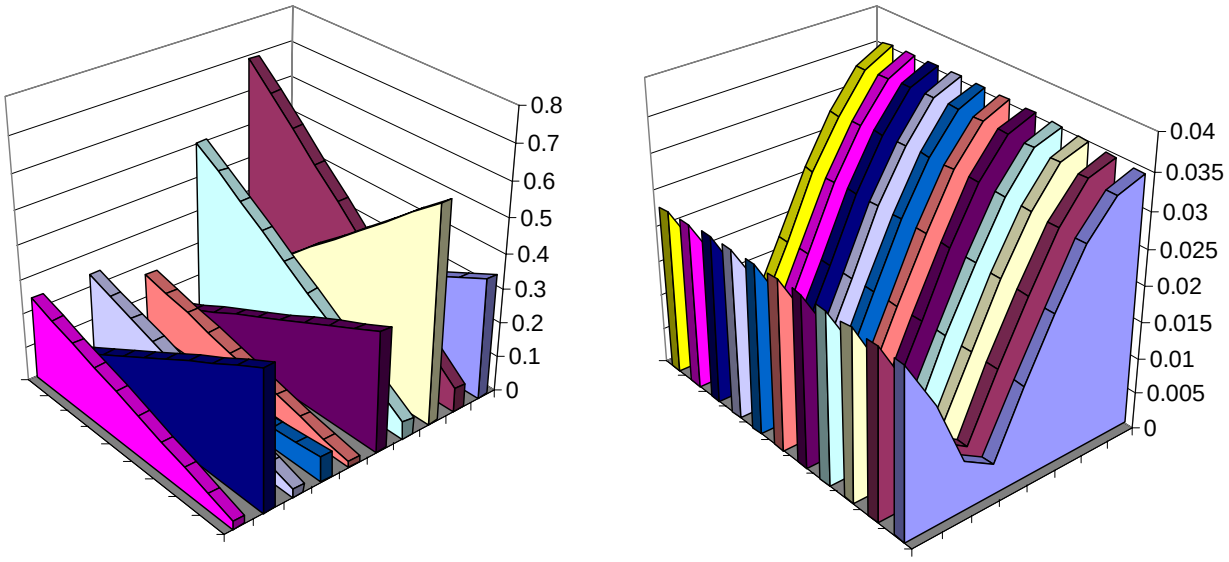


Figure 13. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 17.4MHz frequency.

Figure 13 shows the current distribution at 17.4MHz, slightly below the first parallel resonance frequency (PRF). The current minimum has moved further upwards in the stack of plates, and the current got further amplified. The sum of current magnitudes rose to 2.0291 A, necessitating a further change of vertical scales. On the left chart we clearly see the asymmetrical current distribution; the resonance pushes the current upwards in the stack and as a result, much more current flows on the upper plates. This also means that not only ESR rises, but contrary to conventional assumptions, inductance gets also bigger compared to its low-frequency value.

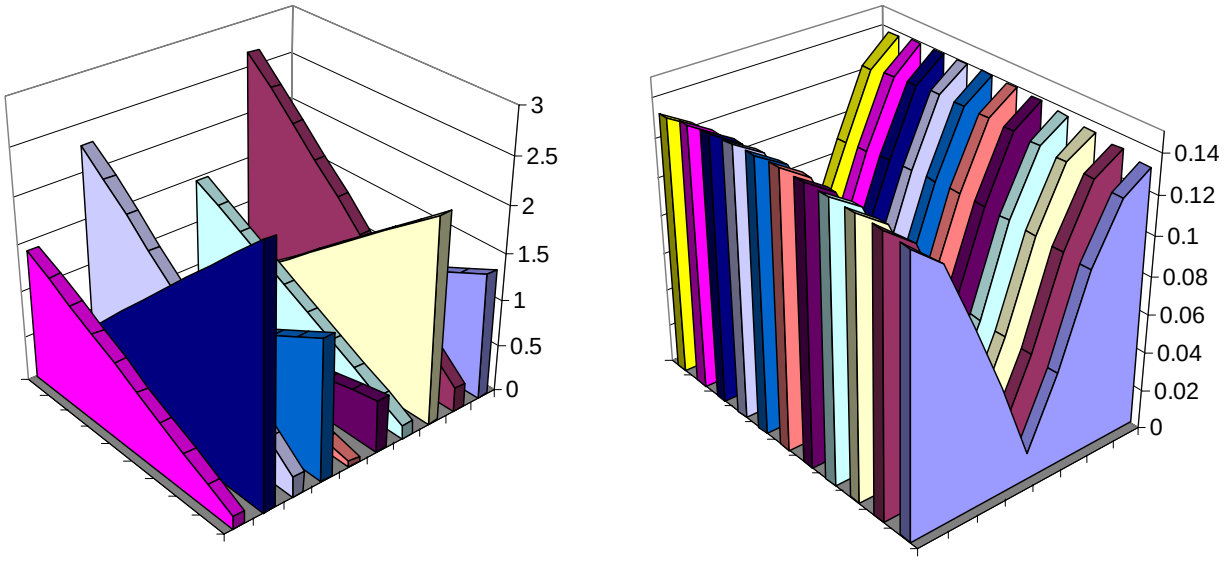


Figure 14. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 22MHz frequency.

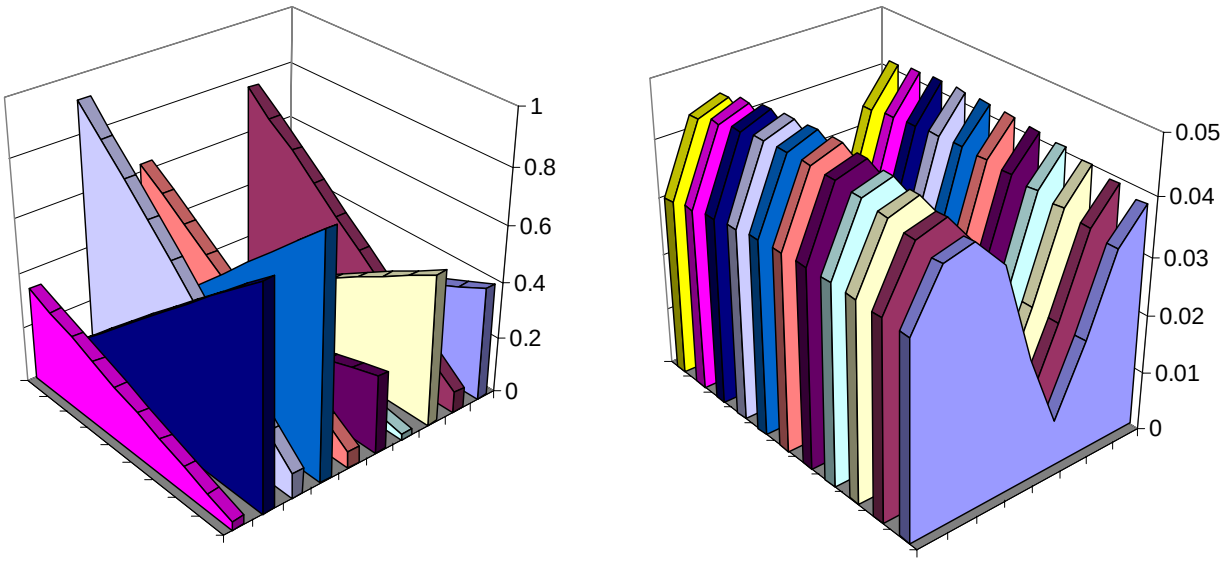


Figure 15. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 27.5MHz frequency (second impedance minimum).

Figure 14 captures the current distribution at 22MHz, which is the first impedance maximum (PRF). The vertical resonance builds up in a way that the current is minimal halfway inside the stack, and maximum both on the bottom and at the top of the capacitor stack. The resonance increased the currents further; the sum of current magnitudes is 9.3278 A, and the vertical scales had to be increased again. This is also the frequency, where ESR in Figure 6 peaks.

Figure 15 refers to 27.5MHz, which is the frequency of the second minimum. The vertical current distribution in the dielectrics develops a broader peak towards the bottom plates, and the resonance now throws the broad maximum towards the return path. This is eventually responsible for the sudden drop of the extracted inductance. At the same time the sum of current magnitudes also dropped to 3.1836 A.

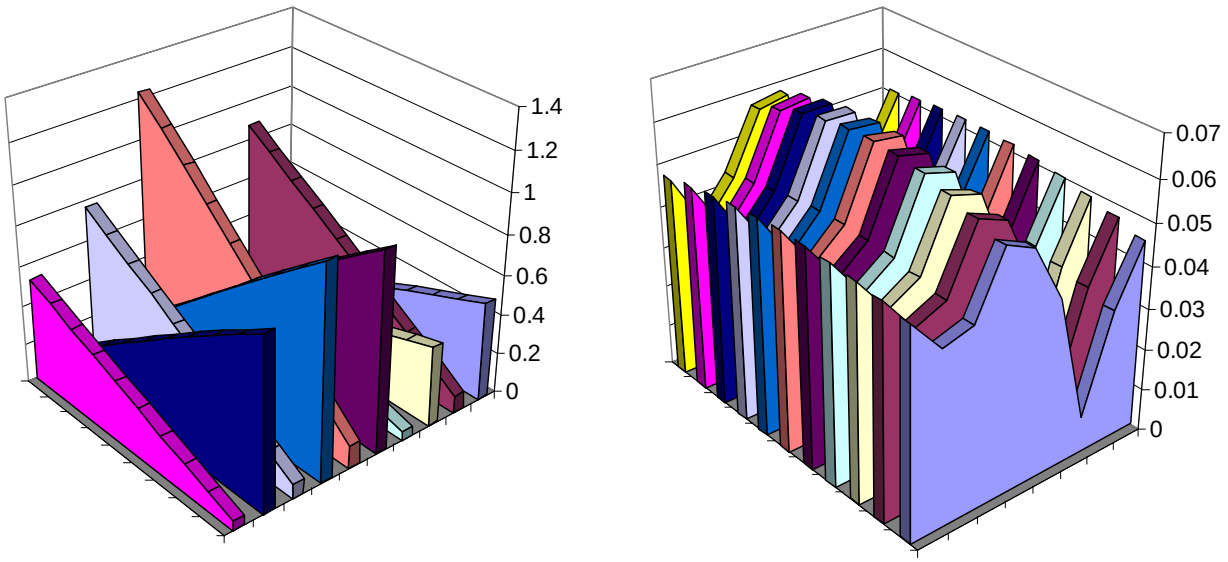


Figure 16. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 34.7MHz frequency (second impedance maximum).

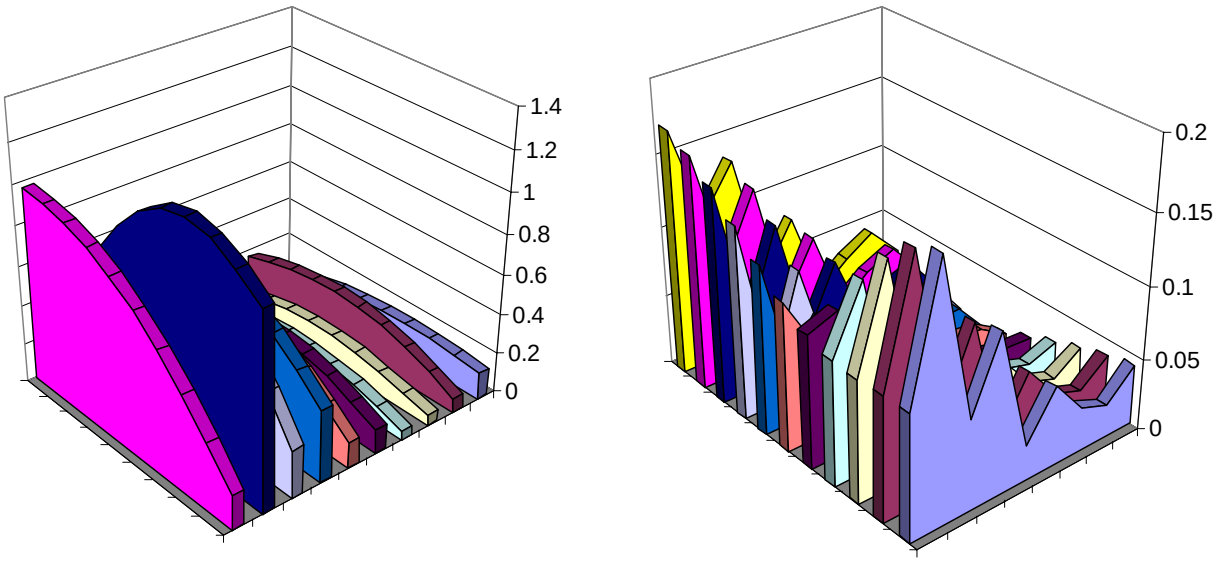


Figure 17. Current distribution along the capacitor plates (on the left) and inside the dielectrics (on the right) at 100MHz frequency.

Figure 16 shows the current distribution at 34.7MHz, at the second maximum frequency. By now, more periods built up vertically, but also more current stays towards the bottom plates; the sudden fall of inductance has already finished. At this frequency the current distribution in the capacitor plates starts showing signs of nonlinearities horizontally; in the middle of the plate, current is slightly above the linear estimate.

Figure 17 shows the current distribution at 100MHz, ten times above SRF. The current distribution in the dielectrics has multiple resonances, and both in the horizontal and vertical distributions the current crowding towards the bottom plates is strong. Horizontal spatial resonance becomes strong.

III. Empirical study of vertical resonances

The simulation-based study in Section 2 focused on the internal current distribution of MLCC parts. The results confirmed that the current distribution in the dielectrics and capacitor plates starts to deviate from uniform distribution already well below SRF. In particular, the current first tends to flow more towards the upper capacitor plates, which starts to increase ESR and later also ESL. With the numbers chosen for the simulations shown here, the increase of ESR at SRF was noticeable by simulation, an 18% increase. This effect was also clearly visible on the measured data of Figure 4: 3.6 milliohms instead of 2.8 milliohms. Altogether, the increase of ESR at SRF is attributed to the vertical resonance inside the part, which resonance starts to build up gradually and distorts the linear current distribution already below SRF. This opens up the question: is the ESR increase around SRF always limited to a small percentage, or could it be much bigger under some other circumstances? We can find the answer either by simulations or by measuring dedicated structures.

Changing the bedspring capacitor model to represent different geometries is easy. On the other hand, to visualize the internal current distribution on capacitor plates and inside the dielectric material, there is no easy way to do it other than by simulations. In contrast, the ESR of a part is only interesting as it is seen from outside, which is easy to measure. Therefore the following figures show the results of a study based on measurements.

The study was conducted with the same kind of capacitors that was used for Figure 4: 10uF 0508 reverse-geometry MLCC parts. Ten parts were selected. The parts were marked individually and their two sides (‘top’ and ‘bottom’) were also identified. All ten parts were measured in the same fixture, in both configurations: ‘bottom’ facing the fixture and ‘top’ facing the fixture. The parts were hand soldered to the fixture by pushing them in the melted solder all the way to the fixture pad. This way, it was possible to eliminate the uncertainty of unknown solder height between the fixture pads and capacitor terminals. Though eliminating the solder fillet in this manner cannot be done in volume manufacturing, in this study we were interested in capacitor characteristics originated from their internal geometry and construction, which justifies the exclusion of external variables. The part-to-part and ‘top’ versus ‘bottom’ variability was found to be almost non measurable among the selected ten parts.

With this consistent set of ten parts, different horizontal and vertical combinations were built. Horizontal configurations (with a different part) have been already studied and shown in [9]. Here we show one of the vertical configuration studies, where the parts were stacked on top of each other, starting with one, gradually adding parts one by one, up to a stack height of ten. The construction is shown in Figure 18.

It was made sure that when a part was added to the top of the stack, all of the parts already on the fixture were left in the same exact position and location (by making sure that the solder melted only around the part added to the top, but not anywhere below). At each phase, the impedance of the fixture was measured, and the parameters extracted. The measurements were done with two separate VNA setups; one covering the 100Hz – 10MHz range, the other covering the 100kHz – 1.8GHz range. The two independent set of curves were merged, and the impedance magnitudes and impedance real parts were plotted.

Figure 19 shows the impedance magnitude with 1, 2, 3, 4, 6 and 10 parts stacked. Traces for 5, 7, 8 and 9 stacked parts followed the same trends and those traces were left out to increase the clarity of graphs. First we can verify that as we add more capacitors, the impedance magnitude below SRF moves to the left in accordance with the increased total capacitance. We can also notice on the full-range plot on the left that above 10MHz all traces run on top of each other. In other words, this again confirms the empirical findings reported earlier that the capacitor height does not degrade (nor does it improve) the inductance associated with the part at high frequencies.

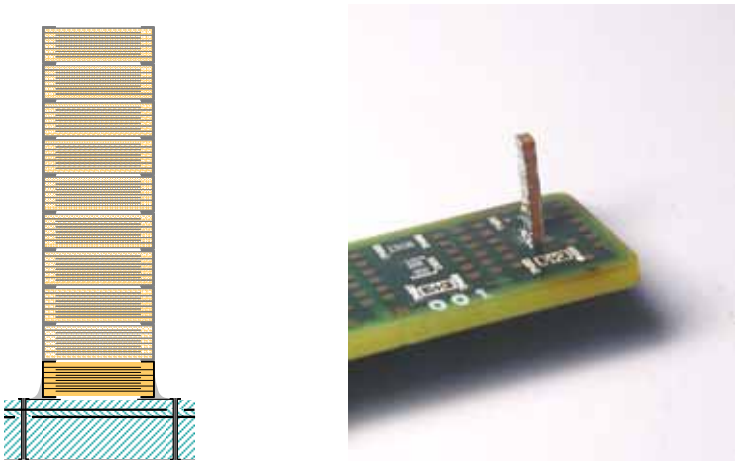


Figure 18. Side-view sketch and photo of stacked 10uF 0508 reverse-geometry capacitors mounted on a small test fixture. The plane pair was 400mil x 600mil of size. The 2-mil dielectric laminate was 4-mil below the surface. The nine grayed-out capacitors in the sketch indicate that these were optional, and were added one-by-one to the stack.

Regarding the plots around SRF, one would expect that as we add capacitors on top of the stack, the impedance minimum continues to go down, maybe saturating beyond a certain height (certain number of parts stacked). Note, however, that the measured data shows something strikingly different: as we add parts, the impedance minimum monotonically keeps going up. This happens in spite of the fact that we only add parts to the top of the stack, without changing the geometry of the parts already on the fixture. The impedance minimum with one part on the fixture is 3.5 milliohms. It goes up to 4.3 milliohms and 5.1 milliohms as soon as we stack a second and third part on top of the first, respectively. With four parts stacked, the impedance minimum is 5.9 milliohms. By the time we have a stack height of six and ten parts, the impedance minimum rises to 7.6 milliohms and 11 milliohms, respectively.

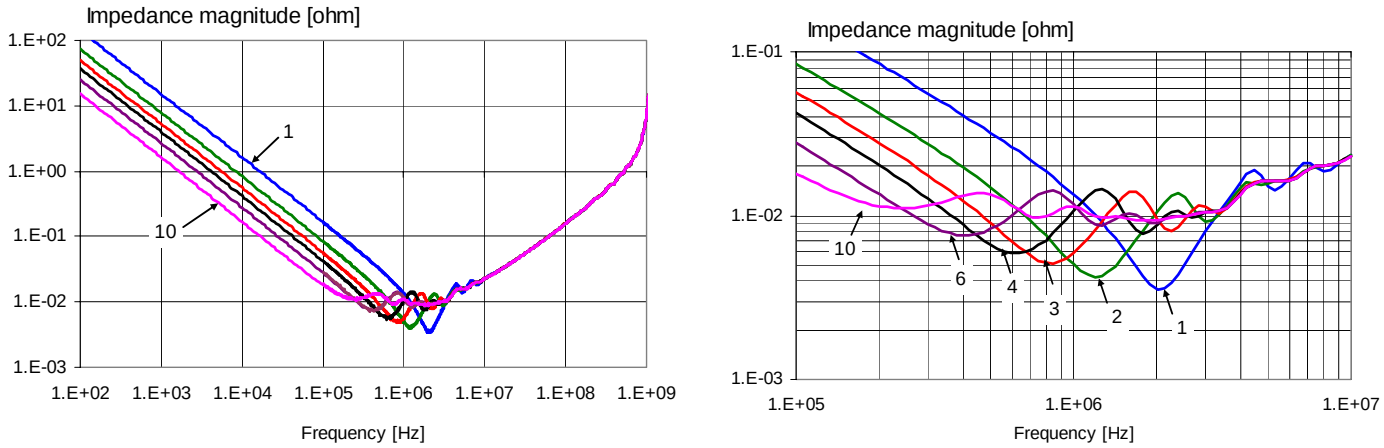


Figure 19. Impedance magnitude of 1-10 stacked 10uF 0508 MLCC parts. Full frequency range on the left, zoomed portion around SRF on the right. The labels show the number of parts stacked.

We can capture the same thing more clearly when we plot the real part of measured impedance. Figure 20 shows the real part of the impedance traces for the same configurations: 1, 2, 3, 4, 6 and 10 stacked parts. Data in Figure 20 confirms that ESR in fact does rise as we add components vertically (which is equivalent of increasing the height of a single component). Also, both Figure 19 and 20 suggest that increasing the capacitor height not only increases ESR, but it also creates a wider frequency band over which the higher ESR is maintained with less fluctuation. The impedance-magnitude and ESR numbers are summarized in Table 1.

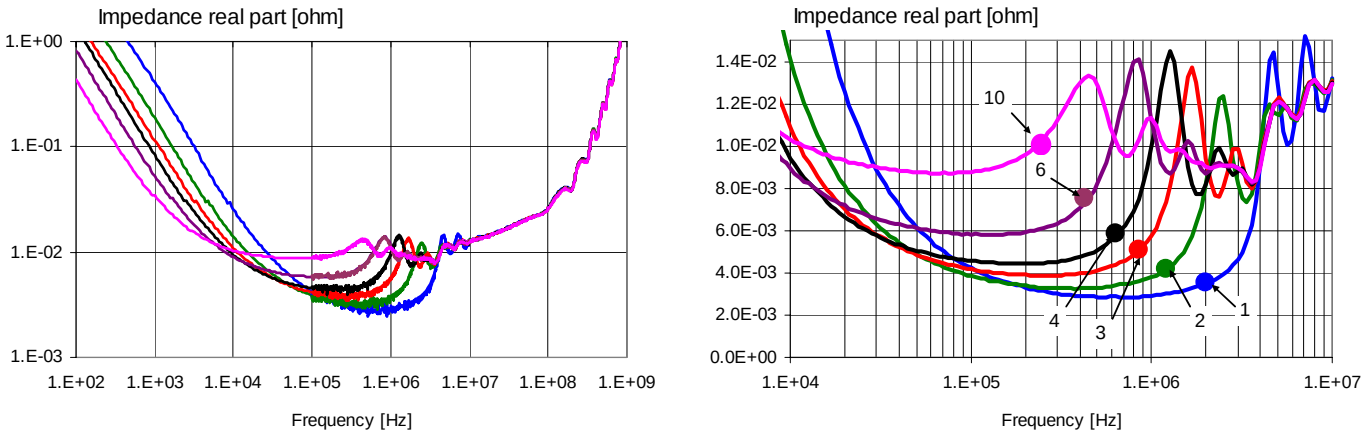


Figure 20. Impedance real part of 1-10 stacked 10uF 0508 MLCC parts. Full frequency range on the left, zoomed portion around SRF on the right. The dots on each trace show the frequency point, where the impedance-magnitude minimum occurs. The labels show the number of parts stacked.

Number of stacked parts:	Impedance minimum [milliohms]	Frequency of impedance minimum [MHz]	ESR minimum [milliohms]	Frequency of ESR minimum [MHz]
1	3.5	2.1	2.8	0.8
2	4.3	1.2	3.3	0.36
3	5.1	0.85	3.9	0.24
4	5.9	0.63	4.4	0.19
6	7.6	0.4	5.8	0.12
10	11	0.2	8.7	0.07

Table 1. Summary of impedance minimum and frequency of impedance minimum values (from Figure 19), ESR minimum (minimum of real part of impedance) and frequency of ESR minimum values (from Figure 20) as a function of parts stacked.

Figure 21 shows the extracted inductance. Note that with ten parts stacked, the inductance stabilizes at about 1.5MHz, from which point it rises, which is, again, counter intuitive. In the 1.5MHz to 5MHz range, the inductance rises by a factor of two. At 5MHz, it joins the slowly decreasing inductance curves of shorter capacitor stacks. The temporary rise of inductance is attributed to the fact that taller capacitor stacks show more pronounced resonances, and with stronger resonances, when the standing-wave pattern rolls towards the lower plates, it pushes more current over a wider frequency band towards the bottom. In the frequency range of stronger resonances the overall inductance gets lower than what we have at higher frequencies. As initial resonances die out at higher frequencies, inductance rises.

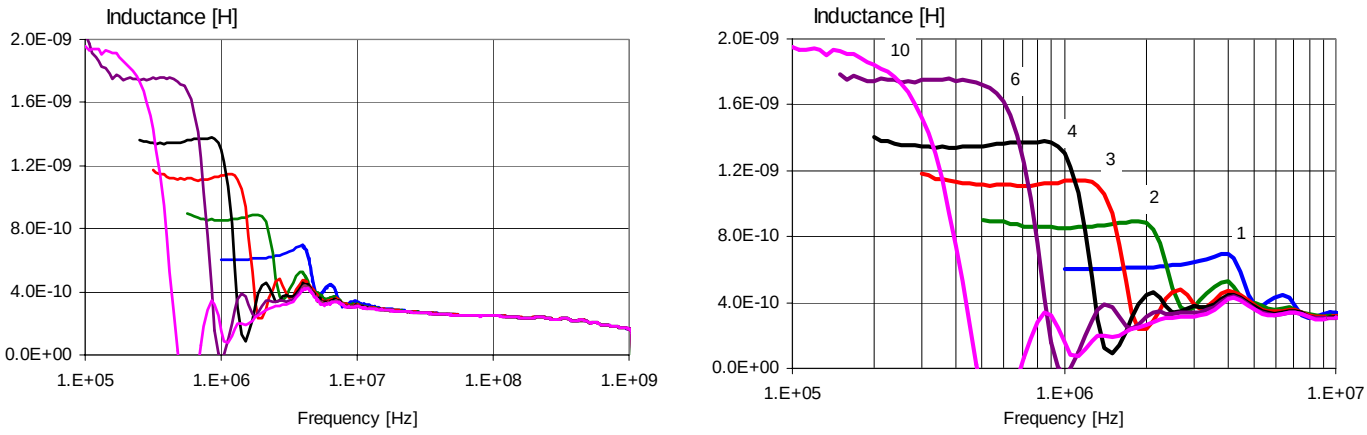


Figure 21. Extracted inductance of 1-10 stacked 10uF 0508 MLCC parts. Full frequency range on the left, zoomed portion around SRF on the right. The labels show the number of parts stacked.

Finally, it was empirically verified that this vertical resonance behavior is primarily the property of the capacitor itself, and the external connecting geometry has little (but clearly more than zero) influence on it. The stack of ten capacitors was carefully lifted from the fixture pads, making sure that solder holding the ten capacitors together did not melt. Two solid copper spacers with rectangular cross sections were soldered on the fixture pads, and the stack of ten capacitors was soldered on top of these spacers. The height of the spacers was approximately the height of a single capacitor in the stack. Figure 22 shows the photo of stacked capacitors on the riser and the impedance magnitude curves for ten stacked parts

with and without the riser. Note that with and without spacers there is no difference in the impedance magnitude below 100kHz. In the 100kHz to 1MHz range the impedance magnitude is slightly higher without spacer. Above 1MHz, the extra inductance of the spacers gradually shows up. Note that both with and without the spacers; the low-ripple bottom portion of the impedance magnitude curves is more than a decade wide.

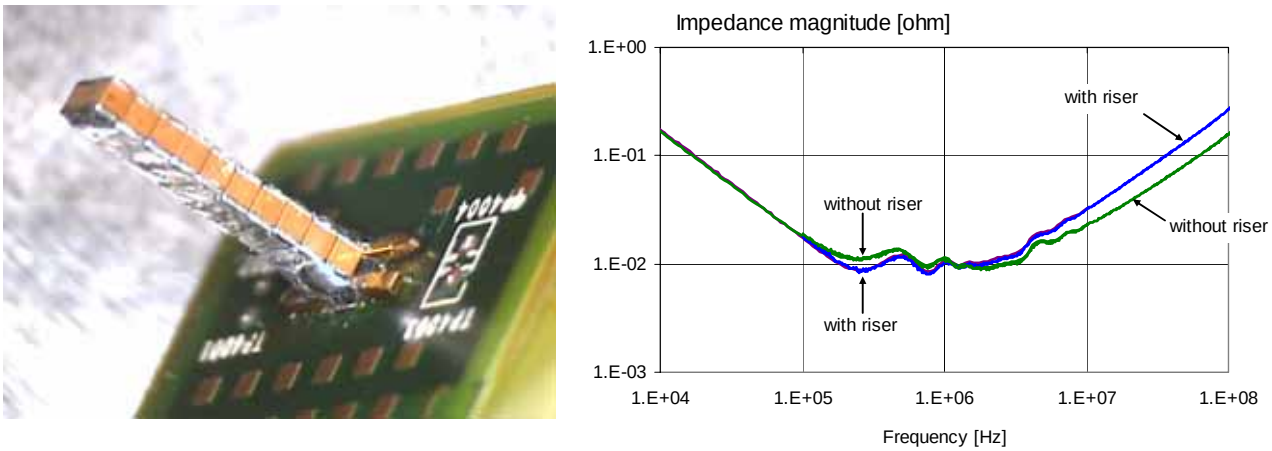


Figure 22. Left: Photo of stacked capacitors on riser bars. Right: impedance magnitude versus frequency curves of ten stacked capacitors with and without riser.

IV. Developing a black-box model

Instead of a complex multi-element lumped models, we can return to the simple equivalent circuit of Figure 1. The complex frequency dependency of C, ESR and ESL can, in general, be taken into account by turning the three elements frequency dependent. This will prevent us from using the models in most time-domain simulations, but the model fits well frequency-domain simulators and spreadsheet-like solutions. This approach follows the widely used standard solution to describe the complex propagation features of traces and transmission lines with frequency-dependent R-L-C parameters.

IV. 1 Modeling of capacitance versus frequency

To find the proper model, first we have to look at the measured data, how the extracted capacitance of different capacitors varies over a wide range of frequencies.

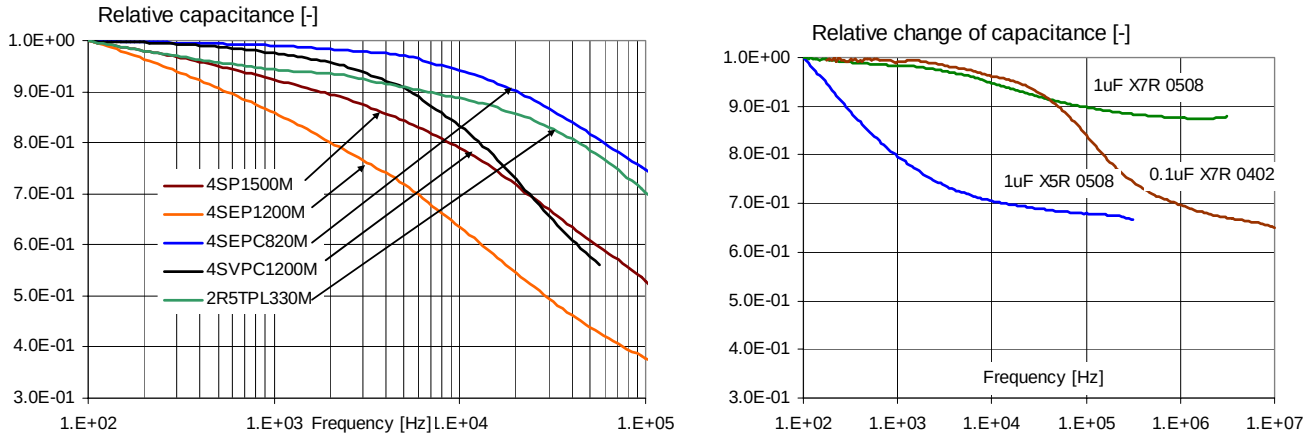


Figure 23. Left: extracted relative capacitance versus frequency of five bulk capacitors. Right: three multi-layer ceramic capacitors.

Figure 23 show the extracted capacitance of various bulk and ceramic capacitors measured from 100Hz upwards. The first four capacitors on the left graph are radial type organic polymer parts in different sizes (diameter and height) of cans. The fifth capacitor is a D-footprint face-down low-height part. The curve for each capacitor is truncated at SRF, since beyond that point the extraction algorithm has increasing errors. The right graph shows three MLCC parts, exhibiting various degrees of capacitance drop as frequency increases..

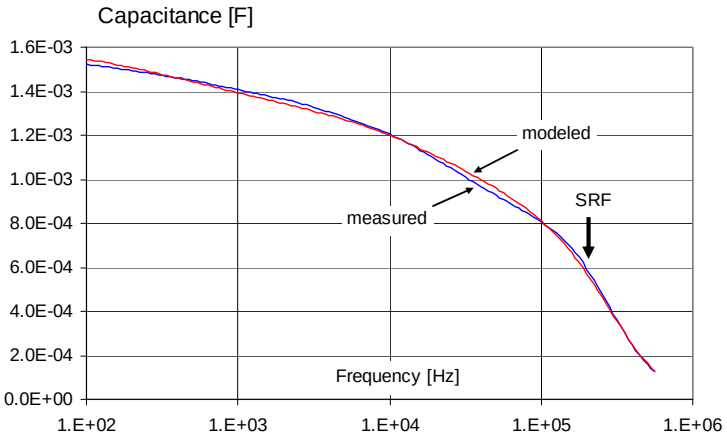
The measured data suggests that the capacitance follows a constant-percentage drop model segment by segment, with varying slopes, which is characteristic of having constant loss tangent for each segment. Empirical data also suggests that the capacitance drops monotonically with frequency, in other words the slope only increases as frequency increases. It may be reasonable to assume that when we reach an inflection point, beyond which the slope is increased, we have a new physical phenomenon that adds to the slope, and eventually in the last (highest-frequency) segment we have the sum of all of the slopes. However, in this paper we are not interested in identifying the physical reasons for the parameter changes, and therefore it is easier and simpler to curve fit the measured data with generic formulas.

It was found that three segments (terms) and seven parameters altogether can model the frequency dependency of capacitance of all parts measured so far.

The approximation formula has three building blocks with seven parameters: a low-frequency asymptotical capacitance (C_0), and three exponential one-pole terms (f_{C1}, m_{C1}, f_{C2}, m_{C2}, f_{C3}, m_{C3}).

$$C_a = \frac{C_o}{\{1+(\frac{f}{f_{C1}})^2\}^{m_{C1}} \ \{1+(\frac{f}{f_{C2}})^2\}^{m_{C2}} \ \{1+(\frac{f}{f_{C3}})^2\}^{m_{C3}}} \qquad (1)$$

In the one-pole terms, the f_{Ci} corner frequencies set the approximate corner frequency: below this frequency the term approaches one; above this frequency the term falls with increasing frequency. Larger m_{Ci} values result in steeper drop.



C_0 [F]:	1.58E-03
m_{C1} [-]:	0.025489932
f_{C1} [Hz]:	9.00E+01
m_{C2} [-]:	0.045950875
f_{C2} [Hz}:	1.00E+04
m_{C3} [-]:	1.548530745
f_{C3} [Hz]:	4.00E+05

Figure 24. Curve fit of the extracted capacitance of a 1500uF organic polymer capacitor.

The result of the process is illustrated in Figure 24. The complex impedance of a 1500uF organic polymer radial-can bulk capacitor was used as a starting point, since this capacitor 'made use' of all three segments in the modeler. The extracted capacitance was automatically curve fitted by varying the parameters shown on the right of the figure. The squares of the relative differences between measured and modeled capacitances were summed over the frequency range of interest; in this case from the lowest measured frequency, which was 100Hz, up to SRF, which for this part was around 100kHz. The Solver function of a spreadsheet software can be used to do the curve fitting automatically. Alternately, a simple macro was written to step systematically each parameter and find the best fit.

IV. 2 Modeling of inductance versus frequency

As it was shown in earlier sections, the inductance of capacitors may vary in a very complex way with frequency. In bulk capacitors, the variation of inductance with frequency was found to be less pronounced and less strong: usually it follows a one-pole exponential roll off. In tall MLCCs, the vertical resonance creates a sudden drop of inductance somewhere two-to-three times above SRF, beyond which frequency the inductance drops smoothly, and it can be approximated with a one-pole exponential roll off. The sudden drop is not monotonic; as we saw above, inductance first rises before it starts to drop sharply. Immediately after the sudden drop, there may be further non-monotonic sections. We have to remember though that unless we bring the causality constraints into the equations, we do not have enough data points to uniquely separate capacitance and inductance at frequencies where none of the two could be rightfully neglected. The assumption of having non-monotonic inductance versus frequency curve in tall MLCCs is qualitatively supported by the current-density plots obtained with the bedspring capacitor model, but the extracted inductance curve, which serves as the basis for curve fitting, works with a frequency-independent capacitance estimate, extracted at SRF.

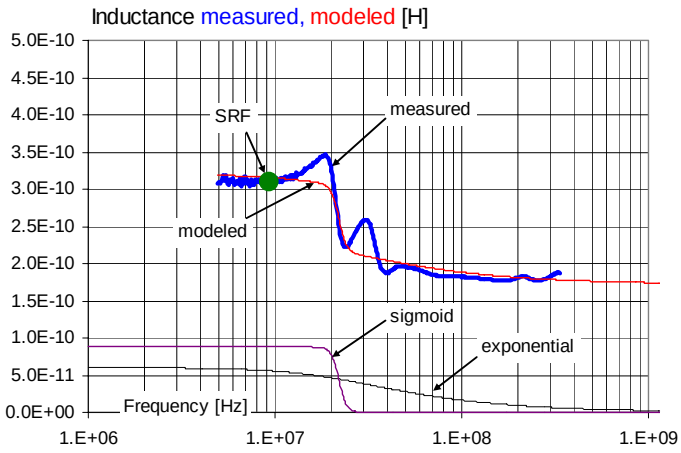
Causality conditions could be included in the curve-fit procedure, but for PDN applications, the actual waveforms of noise has less importance, hence small violations of causality are acceptable in the overall network.

Based on the above considerations, the curve-fit model shown here has three building blocks with seven parameters: an infinite-frequency asymptotical inductance (L_{inf}), a one-pole exponential roll-off term (L_1, f_{L1}, and m_{L1}), and a sigmoidal term (L_2, f_{L2} and m_{L2}) to model the steep step. With the notation of terms on the right-hand side of Figure 25, the approximation formula is:

$$L_a = L_{\inf} + \frac{L_1}{(1+(\frac{f}{f_{L1}})^2)^{m_{L1}}} + \frac{L_2}{1+\exp\{\frac{\log(f)-\log(f_{L2})}{m_{L2}}\}} \qquad (2)$$

Figure 25 shows the extracted and approximated inductance versus frequency traces. To illustrate the curve-fit process, the one-pole exponential and sigmoidal terms in the approximation formula are plotted separately. The one-pole exponential term is similar to the one used for capacitance estimation. The sigmoidal term has its f_{L2} center frequency, which should be set to the frequency of steep inductance drop. The m_{L2} parameter sets the steepness of the sigmoidal transition: smaller values result in steeper transitions. The curve fitting can be done either manually or semi-automatically. In manual fitting, the parameters can be changed in the spreadsheet, and the result can be iterated quickly based on the visual feedback. In semi-automated curve fitting, we can use a macro, for instance, to step the parameters until

the error function gets minimized. The table on the right in Figure 25 shows the minimum and maximum values, which were used by the macro to minimize the error function.



		min	max
L_{inf} [H]:	1.72E-10	1.00E-10	2.50E-10
L_1 [H]:	6.00E-11	3.00E-11	1.50E-10
f_{L1} [Hz]:	2.18E+07	1.00E+06	1.00E+08
m_{L1} [-]:	4.20E-01	0.00E+00	1.00E+00
L_2 [H]:	8.78E-11	3.00E-11	2.00E-10
f_{L2} [Hz]:	2.20E+07	5.00E+06	5.00E+07
m_{L2} [-]:	2.00E-02	1.00E-02	1.00E+00

Figure 25. Inductance modeling. Left: extracted inductance from the measured impedance of a 10uF 0508 reverse-geometry MLCC part, together with the approximation using (2). For the approximation, the values from the first column of the table on the right were used.

The only non-automated part of the curve-fitting is to select reasonable minimum and maximum values to guide and bound the fitting procedure. Note that without any user-supplied limits, the Solver function of spreadsheets may fail to find the correct solution, because the parameters of the sigmoidal term have high sensitivity.

IV. 3 Modeling of resistance (ESR) versus frequency

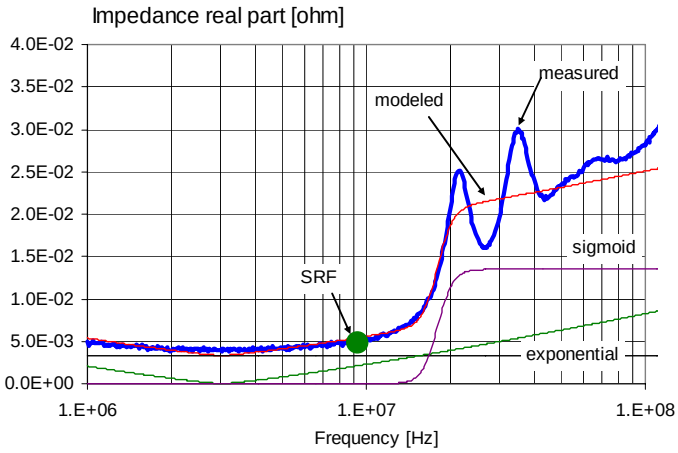
When capacitor losses are transformed into a single series equivalent resistance value, the frequency dependency tends to follow a bath-tub curve. At very low frequencies, the parallel dielectric losses increase the series resistance. At high frequencies, similar to skin and proximity effects in conductors, the current loop reassigns itself to minimize inductance, filling only portion of the capacitor body, hence resistance also increases at high frequencies.

Measured and simulated data shows that in tall MLCCs, at frequencies where inductance drops steeply, ESR increases similarly sharply. As with inductance, this sudden increase of ESR is not seen in most bulk capacitors.

All of the above effects can be captured with three terms and seven parameters: a minimum resistance (R_{min}), a first-order exponential term squared around a minimum frequency (R_1, f_{R1}, and m_{R1}), and a sigmoidal term (R_2, f_{R2} and m_{R2}) to model the steep step. With the notation of terms on the right-hand side of Figure 26, the approximation formula is:

$$R_a = R_{\min} + R_1 \left| \log(f) - \log(f_{R1}) \right|^{m_{R1}} + \frac{R_2}{1 + \exp\{\frac{\log(f_{R2}) - \log(f)}{m_{R2}}\}} \qquad (3)$$

The illustration for ESR curve fitting uses the same MLCC part that was used for the inductance fitting. The fitting of ESR data can also be automated. Either the Solver function of spreadsheet software, or a macro, can be used to do the curve fitting. Figure 26 shows the extracted inductance and the curve-fit result. The first column in the table on the right shows the results of the curve-fit procedure. The second and third columns show the selected minimum and maximum values, which were used in the semi-automated curve fit with a macro. In the semi-automated curve fit solution, the min/max bounds are the only required user inputs; the rest is automated.



		min	max
R_{min} [ohm]:	3.32E-03	2.00E-03	5.00E-03
R_1 [ohm]:	5.00E-03	1.00E-03	5.00E-03
f_{R1} [Hz]:	3.02E+06	2.00E+06	5.00E+06
m_{R1} [-]:	1.2	1.00E+00	5.00E+00
R_2 [ohm]:	1.35E-02	5.00E-03	3.00E-02
f_{R2} [Hz}:	1.80E+07	1.00E+07	2.00E+07
m_{R2} [-]:	2.72E-02	1.00E-02	5.00E-02

Figure 26. Measured and fitted ESR of an MLCC part. The fitting was done with the parameters shown on the right using (3).

Conclusions

It was shown that not only capacitor parameters are sometimes a strong function of frequency, but contrary to popular assumptions, the lowest value of ESR occurs *below* SRF, not at SRF. In tall MLCC parts, vertical resonances push the current upwards, *increasing* ESR and also increasing ESL in a certain frequency range above SRF. A bedspring model visualized the frequency dependent current distribution inside an MLCC part, and illustrated the vertical and horizontal resonances inside the capacitor body. It was further shown by measured data that adding capacitor plates on top of an existing MLCC part eventually will monotonically *increase* ESR. The higher value of ESR has also less fluctuation with frequency. In very tall constructions, inductance can have pronounced frequency bands with opposite slope of change: above SRF first the inductance rises smoothly before it starts to drop. Based on the simulated and empirical parameters of bypass capacitors, black-box models were created to model separately the capacitance, resistance and inductance of parts with a set of consistent building blocks. Manual or automated fitting of extracted data to the selected approximation functions yield good agreement over several decades of frequencies.

Acknowledgement

The author wishes to express his thanks to Gustavo Blando (SUN Microsystems) for his valuable comments on the topic.

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