# Test Floor Management Software

# Using Process Step Verification (PSV) to Ensure Wafers Have Completed All Process Steps

White Paper

Jeffrey C. Quinton
DELPHI ELECTRONICS & SAFETY

F. B. Lynch III
ELECTROGLAS, INC.

## Using Process Step Verification (PSV) to Ensure Wafers Have Completed All Process Steps

This reference guide presents a methodology, using wafer mapping, to validate a wafer has been through the previous test or visual inspection process step prior to continuing to the next process step. This methodology is referred to as Process Step Verification or (PSV).

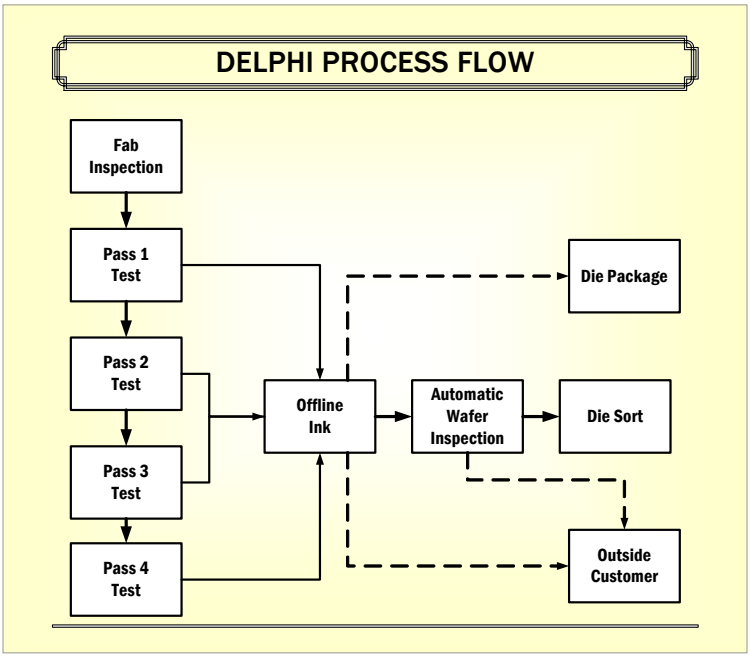
PSV provides a method to assure that wafer/lots will accurately flow through a pre-defined set of process steps. Wafers/Lots at any step in a process will not be tested or processed until they have completed the previous step in the process. The system has been designed to be flexible such that it can be adapted to accommodate virtually any process, and can be integrated with equipment from third party vendors.

## Processing Without Process Step Verification

In a time when the customer expects Known Good Die (KGD) and 0 ppm failures we must make every effort to ensure all wafers are fully processed through the test and die sort area. Process Step Verification (PSV) provides a level of assurance guaranteeing the customer receives good product.

Wafer processing through test, sort and inspection can involve several steps. If any of the steps are missed bad die will be shipped to the customer. Use of a Lot Flow Sheet is not a guarantee that a wafer has been through the previous process step due to the potential of human error. Inventory tracking systems, such as Workstream, do not prevent a lot from moving on if it has not seen a process step. See example flow below.

Figure 1: Delphi Process Flow



When a wafer or wafers miss a process step and get shipped to the customer several things happen, charge backs for scrap, loss of customer confidence, material scrap, increased production to make up for what was lost, engineering investigation, overtime and premium shipments expenses due to impacts to the end customers scheduling. Below are examples of process flow violations and the resultant impact on the end customer.

Example One: Device ABCD is a flip chip IC used in a safety critical application in the vehicle.

- It is tested functionally at first pass. The last step of first pass test is to program some memory cells.
- The device then goes in to a 24 hour retention bake and is tested a second time.
- The second pass test is to make sure the memory cells retain programming.
- The memory cells are then erased using UV light and a third test is performed to make sure devices were erased properly.
- The last step is an automatic visual inspection to check for mechanical or bump damage.

The wafer map created at first pass is updated at each test or inspection pass with additional reject die. The final map is used by the die sorter to put good die in tape and reel.

If any of the above mentioned process steps are missed there could be one of two results. A module level failure at final assembly or latent failure after the module is placed in a vehicle.

- A module level failure would result in lost dollars due to scrap and replacement.
- A latent failure in the vehicle could result in an end customer "walk home" event. PSV ensures that all process have been completed before the IC leaves the test and sort department.

Example Two: Device XYZ is a flip chip used in an automotive application.

- This part is tested functionally before bumps are put on. No inking is done to the device after this step. The only thing that tells you the part has been tested is the wafer map and data file.
- The part then leaves the test area for the bump process and comes back for test after bump. The part may not come back to test for several days.
- Second pass test follows the first pass map and updates it with any additional rejects; however, second pass is not a full functional test.
- The part is then sent to automatic visual inspect and on to die sort.
- This part goes in to a module but at module level the full functionality of the specific IC cannot be tested due to it being a part of a circuit.

If the first/second pass test or automatic visual steps were missed the result would be a failed module and the associated cost – a vehicle assembly plant return with the associated cost and loss of credibility or a "walk home" event with the end customer.

The other potential cost comes from the investment of engineering hours spent trying to salvage the material. Typically, there will only be a few bad die in the reel. In one instance there were 17 bad modules in a lot of 8000. Is there some way to sort out the 17 and ship the rest or do we have to scrap all 8000 units?

From these two examples one can see the absolute criticality of ensuring, beyond human dependence, that all process steps are completed on every lot/wafer. The use of PSV has proven to give us and our customers the assurance that we are providing them with KGD and that they are providing their customer with known good components. One person said it well, "Quality is when our customers come back but our parts do not."

## Cost of a Process Step Violation Event

Figure 2: Example of Costs Associated with Process Step Violations

**Assumptions:**

25 wafers per lot @ $1000/wafer (material and processing) per violation event
Engineering time to investigate cause of spill $125/hr per violation event

**Cost to replace product:**

| | |
|---|---|
| 25 X $1000 | = $25,000 |
| 4 hours X $250 | = $ 1,000 |
| Replacement cost | = $25,000 |
| OT/Premium Ship | = $ 9,000 |
| Total Material/Labor Cost | = $60,000 |
| Total Cost | = ?? (Loss of customer Confidence) |

Supplier has seven (7) PSV violation events per year. This results in substantial revenue loss and major impact to the end customer.

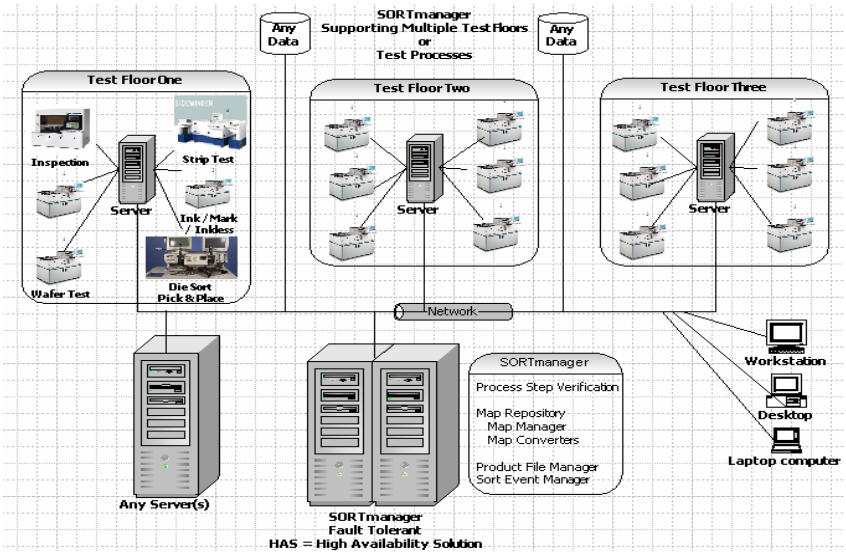
Supplier Annual loss = 7 X $60,000 = $420,000.00.

End customer loss is difficult to compute due to unknown impact on customer confidence and impacts to their scheduling and their downstream end users customers.

## How Does Process Step Work?

Process Step Verification is based on the use of wafer maps at each process step. Process result maps are generated at the first test or visual inspection step. All subsequent processes steps utilize this result map and follow it, processing only good die. If the good die test bad at the next process step the result map is updated to reflect the failure. If a process step is missed the subsequent process step will not follow or process a wafer map that does not have the correct information. PSV involves putting flag(s) in the wafer map file that tracks what process step(s) the wafer has been through. The wafer mapping system has a database/wafer map repository that monitors and validates all process steps for each product type.

Figure 3: Electroglas' SORTmanager Process Step |Verification Process




The overall function:

- Wafer begins the test process at pass 1. A wafer map containing X/Y coordinate and bin information is created and stored in a wafer map repository. The wafer map is named according to the laser scribe on the wafer.
- Wafer is ready for the next process step, pass 2. A zero-bin wafer map is sent to the wafer map repository. This map contains a process step flag specific to the process flow of this product /device. The wafer maps repository checks to see if a map is available and if it is the correct process step. If this passes the validation a map is sent to the machine and processing continues. If validation fails a message is sent to the machine informing the operator to check the wafer for correct processing.
- This validation process continues for all wafers within a lot and all process steps for the product /device.

## Other Considerations for Implementation of PSV

Successful implementation of PSV requires a program to ensure first die integrity at every process step. Garbage in = garbage out. If the first or subsequent wafer maps are not correct, if the die sorters or automatic visual inspection machines cannot get to the correct first die, all the PSV will be of no benefit.

A test floor dependent on wafer mapping and PSV requires the computer hardware and networking infrastructure to be 99.9%+ dependable. PSV is an automated process. If one goes back to a manual process they can no longer guarantee a device has seen all of the process steps and that the resultant IC is a KGD.

A company must decide on a standard wafer map format to use. This format will be specified to any equipment vendor that will be providing test or inspection equipment that will be a part of the wafer mapping/PSV process flow. One must also consider compatibility with equipment used by offshore assembly houses.

Lastly, a robust wafer laser scribe is required to correctly identify wafer maps throughout the process. We convert to a barcode label, which matches the laser scribe, when the wafers are mounted on to a frame for saw and sort.

## Conclusions

As process geometries continue to shrink and process steps become more complicated, semiconductor manufacturers are finding that the ability to quickly ramp up to an acceptable level of yield is a defining characteristic of market leaders. However, just meeting time-to-market goals isn't enough. Customers are demanding 0 ppm defect rates. Throughput and overall equipment effectiveness in these multi-billion dollar facilities must be continuously optimized to keep manufacturing costs in line with the competition. Management and optimization of processes have never been more crucial to the success of the semiconductor manufacturer.

Effective process management requires the ability to take corrective action quickly when an out-of control process condition occurs. In turn, prompt corrective action requires obtaining and managing data from a variety of sources and presenting those data in a manner that facilitates quick decision-making. Since every manufacturing environment is different, any solution must support extensible and unique customization. Also, since users tend to be widely dispersed geographically– from corporate headquarters to remote locations, customer sites, and supplier facilities – collaboration requires a solution with both local and remote access via the Internet. Process Step Verification is that solution for us at Delphi.

Since the implementation of Process Step Verification at Delphi we have not had a missed process step or experienced any quality spills to any of our customers. Our ROI (return on investment) for (PSV) is 0.5 years (6 months) based on investment, throughput optimization and scrap savings.