Using Process Step Verification (PSV) to Ensure Wafers Have Completed All Process Steps

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Abstract

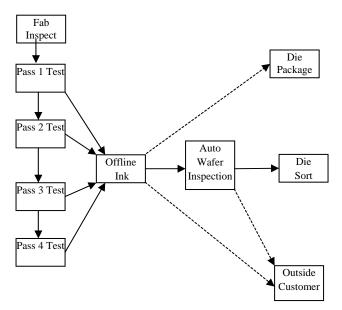
This paper presents a methodology, using wafer mapping, to ensure a wafer has been through the previous test or visual inspection process step before it can run at the next process step. This methodology is referred to as Process Step Verification or (PSV).

Process Step Verification (PSV)... provides a method to assure that wafers / lots will accurately flow through a predefined set of process steps. Wafers / Lots at any step in a process will not be tested / processed until they have completed the previous step in the process. The system has been designed to be flexible such that it can be adapted to accommodate virtually any process, and can be integrated with equipment from third party vendors

In a time when the customer expects Known Good Die (KGD) and 0 ppm failures we must make every effort to ensure all wafers are fully processed through the test and die sort area. Process Step Verification (PSV) provides a level of assurance guaranteeing the customer receives good product.

Processing Without Process Step Verification

Wafer processing through test, sort and inspection can involve several steps. If any of the steps are missed bad die will be shipped to the customer. Use of a Lot Flow Sheet is not a guarantee that a wafer has been through the previous process step due to the potential of human error. Inventory tracking systems, such as Workstream, do not prevent a lot from moving on if it has not seen a process step. See example flow below.



When a wafer or wafers miss a process step and get shipped to the customer several things happen, charge backs for scrap, loss of customer confidence, material scrap, the need to make more material to make up for what was lost, engineering investigation, overtime and premium ships due to customer schedule impact.

Cost of a Process Step Violation Event

25 wafers per lot

\$1000 cost per wafer (material and processing)

Engineering time to investigate cause of spill 125/hr

Cost to replace product.

25 X \$1000 = \$25,000 4 hr X \$250 = \$1,000 Replacement cost = \$25,000 OT/Premium Ship = \$9,000

Total Material/Labor Cost = \$60,000

Total Cost = ??

Due to unknown impact on customer confidence.

7 Process Step Violation Events per Year

7 X \$60,000 = \$420,000.00

How Does Prior Step Work?

Prior Step is based on the use of wafer maps at each process step. A wafer map of the good and bad die is generated at the first test or visual inspection step. All subsequent processes call up this map and follow it, only going to good die. If the good die test bad at the next step the map is updated to reflect the failure. If a process step is skipped the subsequent process will not follow a wafer map that does not have the correct information. PSV involves putting flag(s) in the wafer map file that tracks what process step the wafer has been through. The wafer mapping system has a database that keeps track of what steps a specific product should go through.

The overall function:

- Wafer begins the test process at pass 1. A wafer map containing X/Y coordinate and bin information is created and stored on a wafer map server. The wafer map is named according to the laser scribe on the wafer.
- Wafer is ready for the next process step, pass 2. A dummy wafer map is sent to the wafer map server. This map contains a prior step flag specific to the process flow of this device. The wafer maps server checks to see if a map is available and if it is the correct process step. It everything is ok a map is sent to the machine and processing continues. If everything is not ok a message is sent to the operator, telling them to check the wafer for correct processing.
- The scenario presented above continues for all wafers within a lot and all process steps for the device.

Conclusions

Since the implementation of Process Step Verification we have not had a missed process step or quality spill to any customer. The ROI for PSV is 0.5 years (6 months) based on investment and scrap savings.

Acknowledgments

References