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JULY 12, 2016
TUESDAY

IC Innovation at Heart of Decade of Disruption

BY PETE SINGER

On Monday, imec – the Leuven Belgium-based research consortium – hosted its annual imec Technology Forum (ITF) USA, a half-day conference at the Marriott Marquis. With the theme 'Towards the Ultimate System', imec's speakers and industrial keynote speakers looked at the co-optimization of design and new technology, and how technology innovation can deliver the right building blocks to build these systems.

Luc Van den hove, President and CEO of imec

Delivering the keynote address at the event was Luc Van den hove, President and CEO of imec. He talked about how the world was in the middle of a decade of digital disruption brought about by integrated circuit innovation. He then provided an outlook of how the industry could continue to stay on the path defined by Moore's Law by moving to nanowires and the 3rd dimension.

Van den hove noted what he said were obvious examples of disruption today: Uber, the world's largest taxi company that doesn't own any taxis. Airbnb, the world's largest accommodation provider that doesn't own any real estate.

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DON'T MISS

9:00 am – 9:45 am
OPENING KEYNOTE: There's Never Been a Better Time to Connect
John Kern, Cisco Systems
Keynote Stage

10:35 am – 11:15 am
Silicon Innovation Forum Keynote
Conor Madigan, PhD
President and COO, Kateeva
Innovation and IoT Theater

10:30 am - 12:30 pm
ADVANCED MANUFACTURING FORUM: Pathfinding Beyond 5nm
TechXPOT South

10:30 am - 12:30 pm
ADVANCED PACKAGING FORUM: Packaging Photonics for Speed & Bandwidth
TechXPOT North

10:30–12:30pm
Test Forum
TEST EXECUTIVE PANEL: Economics Perspectives at Test

10:30 – 5:00 pm
FLEXIBLE HYBRID ELECTRONICS: Flex Hybrid Electronics Processing and Packaging

5:00pm – 9:00pm
Leti Workshop
W Hotel - 181 3rd St., San Francisco

Global Economics Limiting Semiconductor Business Growth

BY ED KORCZYNSKI

The near-term outlook for semiconductor manufacturing is challenging, with revenues down slightly but equipment spending up a bit, as reported by experts during the SEMI/Gartner Market Symposium held yesterday afternoon. The global economy is facing extreme uncertainty and is still recovering from the 2008/2009 financial crisis. Duncan Meldrum, Chief Economist with Hilltop Economics, explained why the after-shocks of the 2008/2009 global financial crisis combined with current political uncertainties result in a difficult investment environment. Compared to the 1993-2007 era when world real GDP was +3.2%, there are many indicators that the current ~2.3% GDP growth is the 'new normal.'

"Rolling recessions in different regions have been pulling down global growth," explained Meldrum. "Before the financial crisis, all the

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SEMI Gartner Dataquest *continued from p. 1*

growth rates tended to be together in a coordinated global market. We're actually seeing potential growth cut in half compared to what it was before the recession. That will create a new speed limit on the global economy, so it'll be a tougher world than we're used to." These are high level macro-economic global investment numbers, but there's a high correlation between these numbers and semiconductor industry silicon wafer processing in Millions of Square Inches (MSI).

Capital Equipment Forecast

Bob Johnson, Gartner Research vice president, presented the outlook for semiconductor capital equipment, based on Garner's economic model assumptions:

- Consumer demand will remain weak,
- High inventory of chips in all channels,
- NAND and DRAM in oversupply for the rest of 2016,
- Demand weakness continues longer term,
- No new significant demand driver, and
- Uncertain global economic climate post-Brexit.

Gartner is not bullish on the Internet-of-Things (IoT) to provide a next wave of demand. Premium smart-phones are expected to soon saturate global markets, and PC markets see weak consumer demand. In emerging markets, smartphones will take the majority of disposable income, which lowers new PC and tablet purchases by 10% through 2020.

NAND Flash is the long-term bright spot in the industry, with most of the growth driven by solid-state drives (SSD). However short-term oversupply in the second-half of 2016 is expected due to weak end markets, and increased output of planar 3bit/cell products. 3D-NAND represents 19% of the PetaBytes (PB) of total demand in 2016, increasing dramatically to 70% by 2020. SSDs are not just for PCs and mobile devices, but are moving into the enterprise segment and data centers, and 84% of SSDS will use 3D-NAND by 2020.

Above: Bob Johnson, Gartner Research vice president
Left: Sam Wang, Gartner Research vice president

"3D-NAND manufacturing represents a major shift from litho-centric to etch-centric processing," reminded Johnson. "The cost structures is still not competitive with 2D-NAND, but there will still be ~300k wafer-starts-per-month in the fourths quarter of 2016. By 2018, 3D-NAND will be half of the total NAND bits produced." In response to 3D-NAND competition, 2D-NAND suppliers will likely do another shrink using their fully depreciated fabs, which will contribute to short-term oversupply.

Chinese Foundry Plans

Sam Wang, Gartner research vice president, discussed challenges of the foundry market related to China's plans to develop domestic IC fab capability that is globally competitive. "Believe that China is really serious this time, with $140B investment," said Wang. "The SOC capability of China is world-standard."

For foundry markets in general, with increases in the number of mask layers with successive nodes the selling prices for finished wafers has to continue increasing. Wafer costs for fabless customers buying from foundries are now <$4K for 28nm-node, and <$7K for 14nm-node. TSMC ramped 14nm in one-half-year, and reports unprecedentedly low defects per mask layer to allow them to produce large Apple chips with high yield.

Packaging Trends and China

Jim Walker, Gartner vice president of research, presented on "Semiconductor Packaging: the crucial growth component in China's electronics supply chain." IC manufacturing is critical to the economic growth and national security of China, and it is part of the 'made in China 2015' plan issued by China's State Council.

China today has already invested sufficient resources to now have ~1/3 of the global floor-space in Outsourced Semiconductor Assembly and Test (OSAT) facilities, while the percent of global revenue taken by Chinese companies is still much less. Since China has updated investment plans earlier this year, both South Korea and Taiwan industry organizations issued public statements of the need for strategic counter-investments. The semiconductor industry production in Taiwan represents ~13% of its total GDP, so China's investment into this market is seen as a major threat.

Show Daily Staff

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EXTENSION MEDIA

Vince Ridley
Publisher
vridley@extensionmedia.com

Ed Korczynski
Contributing Editor
edk@extensionmedia.com

Pete Singer
Editor
psinger@extensionmedia.com

Shannon Davis
Contributing Editor
sdavis@extensionmedia.com

Dave Lammers
Contributing Editor
dlammers@austin.rr.com

Kerry Hoffman
Advertising Sales
khoffman@extensionmedia.com

TRADESHOW MEDIA PARTNERS

Mark Larson
Production and Printing
mark@tsmpartners.com

Kevin Clarke
Layout and Design
kevin@tsmpartners.com

Luc Van den hove *continued from p. 1*

Facebook, the world's largest media provider, that doesn't generate any media content.

"These are just a few examples, but we will see this kind of disruption everywhere, in every market and every segment," he said. "Companies will have to adapt. They will have to reposition themselves in the value chain and come up with new business models. This is just the beginning."

What's made this disruption possible is IC technology and ubiquitous mobile computing. What's been particularly beneficial over the last 50 years is that, in addition to the increased functionality that comes with scaling, there were advantages of faster operation at lower power. "This combination of effects that occurs simultaneously with scaling has resulted in the phenomenal evolution," he said.

After a short video clip of Gordon Moore talking about the benefits of microprocessors, Van den hove give a realistic view of the future.

"Today, there is a lot of debate about the continuity of Moore's Law. Yes, we're faced with several tradeoffs. It's getting harder and harder (to scale) and when we scale down our transistors we do not automatically the performance improvement that we used to with previous generations," he said. "But we are sure there are sufficient solutions out there that will allow us to continue Moore's legacy for several more decades. I am convinced that scaling will not only continue, it *has* to continue. If you want to enable the IoT wave, we will have to succeed in extending Moore's law to generate the required compute power and storage capacity."

Van den hove added that Moore's Law is on the verge of morphing. "We will need other techniques in order to realize this complexity increase," he said. "We will continue 2D scaling. It will evolve from the FinFET that is in mass production today towards horizontal nanowires, towards most likely vertical nanowires. This will bring us to at least the 3nm generation if not one or two generations more. This will keep us busy for the next 10-15 years."

"If you want to enable the IoT wave, we will have to succeed in extending Moore's law to generate the required compute power and storage capacity."
—LUC VAN DEN HOVE, IMEC

Luc Van den hove, president and CEO of imec, tipped his hat to Gordon Moore, showing a short video clip and describing a future where Moore's Law will live on through 3D integration.

He stood by his past comments on the production-worth status of EUV. "To enable this, we will need a cost-effective lithography. We absolutely need EUV lithography to make this happen. I'm sure, based on the progress I've seen over the last 12 months, that EUV is ready to enter manufacturing. But we have to be realistic. Eventually, 2D scaling will slow down. I'm not saying it's going to stop. But it's getting harder and harder and hence it will require more time to transition from one geometry-based node to the next geometry node. We will need other ways to compensate for this gradual slowdown. One of the obvious ways to do so is to start using more extensively the third dimension, as the memory guys have started to do already," he said.

Van den hove presented a future where devices are stacked on top of one another like Lego blocks. "Once we are using these vertical nanowires, it's not so difficult to imagine that we may be stacking those transistors on top of each other – stack an n-FET on top of a p-FET and realize an SRAM cell. It's obvious that such a 3D version of an SRAM cell has a much smaller footprint than its 2D equivalent. Once we can do that, we can even imagine that we may start stacking some of these building blocks on top of each other," he said.

"It's more straightforward to imagine that this can be done with a regular structure such as an SRAM design, but also FPGAs are very regular structures. We can even imagine that we could design random logic and design standard cells within the constraints of such a 3D Lego block and build up a logic circuit with these Lego blocks in a 3D fabric," he continued.

Heterogeneous integration with photonics is also on the drawing board. "We will combine this also with 3D heterogeneous integration where we will be using chip stacking technology with high bandwidth, high density through silicon vias. We can then combine all these layers with 3D stacking and through-silicon vias, integrate all of this on an interposer, which can also be the substrate to integrate these 3D cubes," he said. "By adding also photonics on such an interposer, we can also realize optical IOs. This is just another rendition of Moore's Law which will allow more complexity in a smaller form factor."

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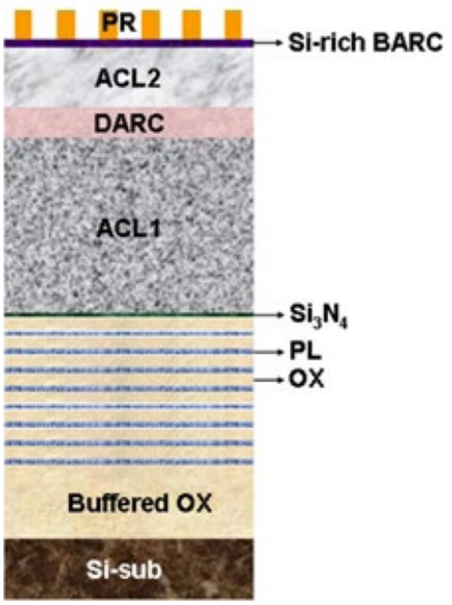
Tri-Layer Resist Resolution Extensions for Advanced ICs

BY ED KORCZYNSKI

In the advanced ICs with the smallest device features, there are new challenges with etching and with lithographic masks. At 22nm lines and spaces, the masking material must be just 44nm thick for desirable 2:1 aspect ratio. This has led to an increase in the use of Hard-Mask (HM) layers for etching, which typically use a correspondingly thin photoresist (PR) above for pattern transfer. Some manner of Bottom Anti-Reflective Coating (BARC) is used to smooth topography, and the combined stack of BARC+HM+PR is termed "Tri-Layer Resist" (TLR). TLR is one way patterning resolution can be "Extended" as detailed in the new report from TECHCET Group, "Critical Materials Report: Photoresists, Extensions and Ancillaries 2016." TECHCET is an Advisory Service company focused on Process Materials Supply Chains, Electronic Materials Technology, and Materials Market Analysis, and has produced the Critical Material Reports for SEMATECH members since 2000.

The TLR stack is often complicated by additional under-coats and over-coats and spin-on HM so that the actual number of layers in the "Tri-Layers" can be 4 or 5. The **Figure** shows a complex multi-layer stack shown by Macronix International Co. at ASMC 2016 used to etch holes through up to 16 alternating layers of silicon dioxide and polysilicon to form vertical-gate gate-all-around (VG-GAA) cells for 3D NAND Flash chips. The Amorphous Carbon Layers (ACL) separated by the Dielectric Anti-Reflective Coating (DARC) are used as a part of a negative tone development (NTD) process for hole patterning.



Source: ASMC 2016

While the global market for PR is mature and growing slowly, with revenues expected to hover around $1.4B for the next 4 years, the market for all of the specialty Extensions (EXT) spin-on layers used with PR is expected to grow steadily from 2016's forecasted global estimate of US$680 million. EXTs also include specialty chemical formations to "trim" lines by removing photoresist material, or to "shrink" holes by adding material to sidewalls. The extension materials submarket is now the fastest growing segment within the traditional lithography space, and it is forecast to reach $790M by 2020, as detailed in TECHCET's report.

Virtually all of the growth in lithography materials can be attributed to volume growth in advanced nodes. While the 5 year CAGR outlook for silicon wafer starts is relatively small for the 45nm node and larger, that same outlook is +10% growth for the 28nm node and smaller. ArF (193nm wavelength) resists already comprise over 40% of the total market. Extreme ultraviolent lithography (EUVL @ ~13nm wavelength) remains in the forecast for 2020, but it will be limited to mix-and-match implementation at the 10nm node due to its premium cost and low throughput. Nano-Imprint Lithography (NIL) is in limited use by one Asian memory fab. Multi-patterning with 193nm immersion will remain the workhorse for all leading edge IC fabs.

[*Disclosure: Ed Korczynski is also Sr. Technology Analyst with TECHCET Group, and author of the "Critical Materials Report: Photoresists and Extensions and Ancillaries 2016".*]

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A New Age of Smart Manufacturing Underway

BY PETE SINGER

A major theme at SEMICON West 2016 is Smart Manufacturing, a.k.a. Industry 4.0 and Industrial IoT (IIoT). One definition of smart manufacturing, said Tom Salmon, the SEMI vice president of collaborative technology platforms, is the use of production and sensor data with manufacturing technologies to enable adaptability in processing. It encompasses automation, data exchange, and the transfer of product design data and manufacturing state data.

SEMI estimates that by 2020 there will be about a billion IoT devices at work in manufacturing facilities. By 2020 global manufacturers will invest $70 billion in IoT solutions that year, compared with $29 billion in 2015.

Currently, these devices are used largely to track factory assets, to consolidate control rooms, and to increase analytics functionality through predictive maintenance. The goal is that product design data and manufacturing state data will travel through the manufacturing process with the product. This requires that data is communicated to product lifecycle systems at the product companies and to service providers simultaneously.

Tom Sonderman, Rudolph Technologies

A number of SEMI standards are facilitating this shift, including Equipment Data Acquisition (EDA), to improve and facilitate communication between manufacturer's data gathering software applications and factory equipment.

SEMI kicked off an advisory council around smart manufacturing, and will coordinate a Smart Manufacturing symposium at SEMICON West on Wednesday, July 14, and again at SEMICON Europa on Oct. 25 in Grenoble, France.

Thomas Sonderman, vice president/GM of Rudolph Technologies' software business, said the advisory council links the fabless and the equipment OEM supplier communities. One goal, Sonderman said, is "to help understand what's required to really take on these concepts, and turn them into something that people can use to improve their overall fab efficiency."

At the Smart Manufacturing Symposium, Sonderman will discuss what he calls traceability: optimizing the supply chain by blending IoT technologies. How information is acquired and used for Big Data predictive analytics and machine learning is one key aspect. "How do you turn data into some kind of actionable intelligence? I think the idea is to get some consensus around what it actually is, and then what's required to make it successful," Sonderman said.

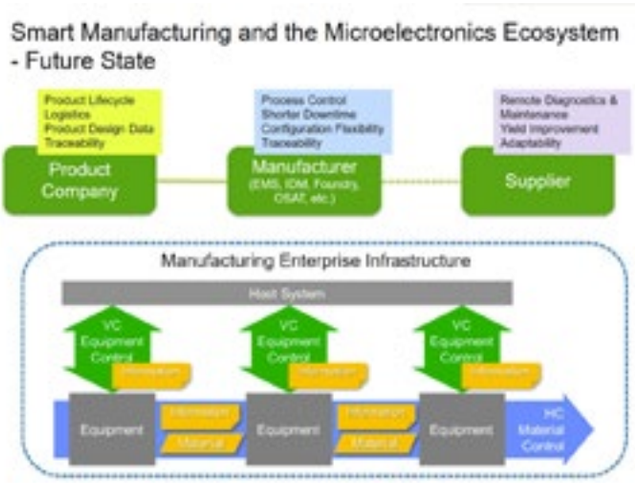

Figure 1. What the future may look like for smart manufacturing in the semiconductor industry.

Data security is also important. Data that comes out of fabs is of interest to suppliers, the fabless community and IP companies, among others who create a virtual IDM. "How does a Qualcomm get access to their relevant information, and on the other side, how does a company like Tokyo Electron Ltd. (TEL) or Applied Materials or Lam Research get access to that same information so that everybody can make the right decisions and shift the paradigm from reactive to a predictive/proactive approach.

"We need to go from 'Hey, I have this problem. What caused it? How can I go fix it,' to 'What kind of analysis do I need to do to run my business? What kind of business intelligence is required to run the business, and how can I create analytical scenarios so that I can make sure that I have the information relevant to me to make decisions I need to minimize my time to market, and maximize my profitability?'"

In order for smart manufacturing to succeed, companies must be able to build confidence that they can share data securely. (At Wednesday's symposium, NextNine, an Israeli IT security company, will present its work with TEL, several U.S. security agencies, and others concerned with moving information around securely).

One opportunity, Sonderman said, is to provide information-linking capabilities to 200mm and smaller wafer manufacturers, making RF filters, sensors, and other products.

"They don't have a lot of the traditional capabilities that you come to expect. The idea is to link their information together but do it in a way where you can adapt it into those older facilities," he said.

Rather than use a standard SECS/GEM interface, some tool data can be acquired wirelessly.

"There are all types of information that are relevant to the products, and if you think about what goes on a lot in the fabs it is linking what goes on in the product to what's going on inside the tools. At legacy or non-leading-edge technology fabs, some of this in itself is a challenge," he said.

Manufacturers also seek to link metrology data, with two different threads of information coming in: one from wafer-level metrology, and another stream of information from the equipment, which collects data each time the wafer crosses that piece of equipment. Also relevant is product information, including processes that can run multiple products. Figure 1

shows how this kind of data may be collected and shared in the future.

"The concept here is that you link these together in threads and then you create what we call the thread synchronization engine, which allows taking all of this relevant information and create a tapestry of data, which is a very pure data set that's very representative of the combination of all these different factors," Sonderman said.

The same types of information threads are woven together in the back-end (packaging) operations, where advance analytics are becoming as essential as in front-end processes.

Analytics are multifaceted, involving everything from visualization, data mining, spatial pattern recognition, and virtual metrology information. "Ultimately what I'm doing is trying to create a wafer-level signature and a tool-level signature and combine those together to create some kind of information I can take action on. That's the actionable Data Now concept," he said.

The goal is to combine information, separating the signal from the noise, and then analyze the data to ascertain whether or not a given process step or combination of process steps has contributed to yield loss. By drilling down into the shared data, engineers can discover whether a tool or set of tools is causing the problems.

"This is where things get really interesting. First, you have got to link everything together across the supply chain. Then you have to start looking at how do I drill down inside the equipment?" he said.

Large fabs with literally thousands of tools in operation are collecting huge amounts of information, essentially time series-based data. Linking tool information into an analytical combination with wafer-level information (what was going on inside the tool when those wafers were processed) is a powerful way to improve efficiencies. "That's where this combination of big data analytics and traditional real time FDC is coming together," Sonderman said.

To make this work, companies need a Big Data architectural environment, which combines structured data (in many cases in an Oracle database) with unstructured data (often text data, such as maintenance logs). Finally, there is a third space, a combination of time series-based data, such as images and spatial patterns.

The challenge, Sonderman said, is to link all the data together, standardizing the data so that it can be matched with various machine-learning algorithms. "From that I can analyze the data and start spitting out useful information that people can take action on," he said.

To do that, the industry must deal with the security challenge. "There are ways to solve that challenge, but if we don't solve that as an industry — and it really is an industry challenge — then we're going to be handcuffed in terms of being able to take this technology to its ultimate realization. I think that's now become the priority, versus preparing for the next wafer size and all that," Sonderman said.

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During SEMICON West, early adopters are promoting EtherCAT as a next-generation real-time Ethernet control solution, with a variety of attributes: it is fast (good for controlling ever-more precise process recipes), open source, and extendable to many more nodes than existing networking protocols. Those attributes make EtherCAT attractive to tool makers such as Applied Materials, Lam Research, and Tokyo Electron Ltd., as well as sub-systems suppliers such as Edwards (Crawley, England).

Fab managers increasingly are looking ahead to the availability of predictive maintenance and other data-based productivity approaches, all of which require fast, extendable networks.

EtherCAT is fast enough for near real-time control. Andrew Chambers, a product manager at Edwards, gave the example of a process recipe that requires a change in gas flow, resulting in a deviation in chamber pressure. To maintain good process control the pressure controller must respond to the change in flow as quickly as possible in order not to lose time as the process chamber conditions stabilize. The EtherCAT control architecture can enable the change in flow, and pre-emptively adjust the pressure control, in real time, using a central controller over the EtherCAT network, rather than relying on the devices responding individually to changes in circumstances.

Increasingly, shrinking device geometries and the trend towards "atomic-scale engineering" are putting pressure on the process tools to control all process parameters with high precision in real time. EtherCAT supporters argue that with very short cycle times and response rates, real-time process control becomes realizable, overcoming the problems that arise from serial control and looped-in control, which can introduce delays in the system.

Edwards' Gerald Shelley said as tool vendors seek to improve processes, they may need to reduce individual process steps to less than one second. That in turn requires a fast network to enable parameter changes at a correspondingly high rate.

Beckhoff Automation developed EtherCAT based on a specific functional principle, they describe it as "processing on the fly", which supports very short cycle times. EtherCAT's rapid response times have therefore proved attractive to semiconductor process tool developers, Shelley said.

Flexibility, another key virtue, allows EtherCAT to support more than 65,000 nodes on a

network. “It’s extendable. It can be reconfigured. And there is an emerging option where the network itself can provide power to the devices attached to the network, which reduces the cabling requirements to the system,” Chambers said. Pre-existing, conventional fieldbus networks can be added to the EtherCAT network as additional nodes. “If you’ve got a pre-existing system that you want to integrate into something new that has an EtherCAT network, then you can do that,” he also noted.

As an open protocol network, any party can use EtherCAT, which is described in international standards.

“It has the benefit that it doesn’t need any particularly special infrastructure components to make it run. There’s not a special master device. The devices themselves can incorporate the EtherCAT protocol. You can simply plug a device into the network and have it run. That makes it relatively easy to use,” Shelley added.

Toolmakers, such Applied Materials, Lam Research and Tokyo Electron Ltd., currently use a wide variety of tool control systems on their diverse product ranges. EtherCAT is seen as a route towards a common, adaptable control architecture that could support a diversity of process tools on a common platform.

Beckhoff Automation, with about 3,000 employees worldwide, has worked with its business partners to set up the EtherCAT Technology Group to further develop EtherCAT. The technology group currently has 3,810 members, up from just 300 in 2006.

“There will be open standards so that they’re available to all interested parties, but in particular the profiles of the devices which can be added to any EtherCAT network, the profiles which control how devices respond and communicate with a network, are being generated and developed by the supplier working groups, of which Edwards is a member. We, along with a wide range of other sub-system suppliers are developing devices to meet the requirements for installation in EtherCAT networks, to be able to provide the functions and features that are needed by the semiconductor industry,” Shelley said.

In the future, process tool manufacturers will be able to select from a range of devices with similar functionality which will fit on the same network, so it reduces the dependency of toolmakers on specific individual suppliers. This enables process tool makers to develop advanced bespoke control algorithms and address emerging process challenges.

“From a total process control perspective, our view is that as high volume manufacturing moves towards smaller and smaller nodes, introduction of those processes is going to depend on a complete sub-fab process solution per process tool. These solutions will be based on some kind of integrated best-known method that describes how you set up the sub-fab equipment to deliver what the process vendor needs,” Chambers added.

Test Protocols for the IoT

BY ED KORCZYNSKI

The Internet-of-Things (IoT) will require components that can sense the world, process and store data, and communicate autonomously within a secured environment. Consequently, IoT devices must incorporate sensors, wireless communication at Radio Frequencies (RF), logic, and embedded memory. Integrated circuit (IC) chips for IoT applications will have to be created at low cost in High Volume Manufacturing (HVM) lines, for which there are unique challenges with design and test. Presto Engineering's founder and president, Michel Villemain, spoke with the Show Daily about how his company's test services can accelerate the time-to-market and reduce risk in creating new IoT chip products.

"We started 10 years ago, and were differentiated on RF," explained Villemain. "We now have a good view on what test costs are in production for different chip functionalities. We focus on specific segments of the industry that are not the traditional 'drivers' such as SoCs and communications chips." Since most IoT devices are expected to use Over The Air (OTA, a.k.a. "wireless") links, Presto's expertise in RF test helps create a low-cost sensor solution for customers.

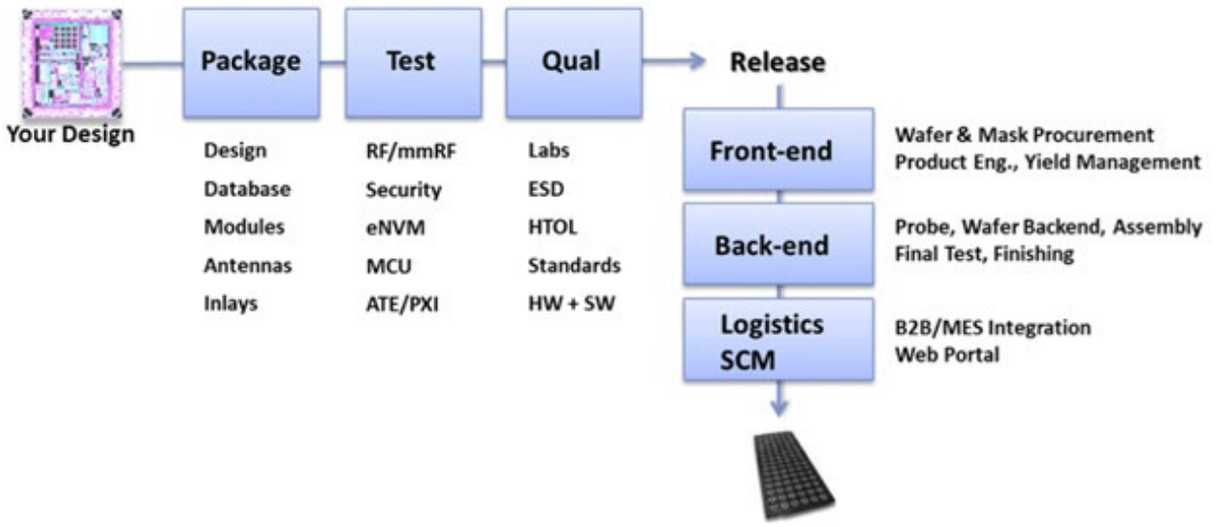
"We see some general trends in this area, "said Villemain. "The first one in IoT is there is a lot of activity in determining proper protocols for communications, as the industry moves from using short-range private area networks to low-power wide-area-networks with range up to 300 feet. The second trend which is not technical, is that more and more non-semiconductor companies such as 'system houses' will be designing chips to reduce costs and increase security.

"The need for security has been reported as one of the main issues in peoples' minds preventing deployment of the IoT. When security has to be hardware related and implemented in the chip, the only easy way to enable it is with test," confided Villemain. "Remember that security is not binary. There is a return-on-investment decision based on how easy would it be to break something and how much would it cost to prevent that breakage. There is somewhat of a consensus that hardware-based solutions provide more security for data traveling over a link, so what we are trying to do is lower the cost of adding security at the hardware level."

For the test of a very large and complex device, all of the digital instructions are generated by the design tools. However, for a primarily analog device the digital is not the core of the design and not the core expertise of the design team. The Figure shows the workflow used by Presto to methodically manage the establishment of rigorous test protocols for

complex SoCs.

"Provisioning" is defined as the use of embedded Non-Volatile Memory (NVM) such as Flash within a chip to be able to customize the functionality. If you need to test Flash cells and bake, then program the Flash and bake again before final test it calls for three probe insertions, so the type of NVM chosen can alter the text protocol needed.



At end end of last month, Presto announced a multi-year supply agreement with NAGRA—a Kudelski Group company in secure digital TV access and management systems—to provide supply chain management and production services for several of NAGRA's key products in the Pay TV market. "We are delighted that NAGRA has placed trust in Presto to be its production partner for volume products," said Michel Villemain, CEO, Presto Engineering. "Leveraging team and expertise acquired from INSIDE Secure in 2015, this is a natural complement to our strategy of deploying an independent subcontract back-end manufacturing and supply chain service for the secure card industry and IoT markets."

Applied Materials Intros High Res E-Beam Inspection System

On Monday, Applied Materials, Inc. its next-generation e-beam inspection system that offers resolution down to 1nm. This allows users to detect the most challenging "killer" defects that other technologies cannot find, and to monitor process marginality to rapidly resolve ramp issues and achieve higher yields. Called PROVision™, the system offers 3x faster throughput over existing e-beam hotspot inspection tools.

Ram Peltinov, senior director, strategic marketing for the Process Diagnostics and Control Group at Applied Materials, said the development of the new system was driven by a number of new challenges: Structures and defects are now too small for optical resolution; multi-patterning triggers a need for massive measurements; and 3D architectures limit the ability to detect and measure.

"FinFETs are becoming increasingly complex, the multi-patterning creates multiple steps, the DRAM aspect ratios are getting very high and the VNAND is going vertical," he said. "All these changes are happening in parallel and this creates great opportunity for metrology and inspection," he said. According to Gartner, the market for e-beam inspection systems has tripled in the last five years, from $81M in 2010 to $241M in 2015.

The PROVision features a newly designed e-beam column that can increase the amount of electrons without a large compromise in the resolution. "It allows them to capture defects they couldn't see before," Peltinov said. The system can detect, for example, epi-overgrowth in FinFETs. "While the epi overgrowth is clearly visible on the PROVision, it's almost impossible to see in conventional EBI. Without the resolution and the special imaging, it's very difficult to catch that."

The Applied Materials PROVision e-beam inspection system.

"They can also increase their sampling with the faster throughput on the most challenging layers. This also helps them reveal process signatures of their most subtle process variation." Massive sampling reveals hidden process trends and "signatures" that help identify sources of abnormalities, and shorten the time to root cause from days to minutes.

Collaboration in MEMS, Sensors and ICs

MEMS & Sensors Industry Group® (MSIG) invites attendees to a special half-day workshop on the convergence of MicroElectroMechanical Systems (MEMS) devices, sensors, flexible substrates and semiconductors in the Internet of Things (IoT) at SEMICON West on July 13, 2016. Speakers will explore the theme "From Collision to Convergence: Co-Creating Solutions in the Semiconductor and MEMS/Sensors Industry" as they address a new and necessary level of collaboration for enabling IoT and other growing applications.

"The supply chain for the IoT is complex, and navigating its dynamic ecosystem requires collaboration among stakeholders," said Karen Lightman, executive director, MEMS & Sensors Industry Group. "By focusing on pre- and non-competitive challenges, industry players work toward common goals that benefit all — and that are only possible through collaborative effort. Attendees of the MSIG and SEMI joint workshop will get updates on the most pressing challenges to the increased use of MEMS, sensors and semiconductors in IoT applications."

"Our joint workshop with MSIG at SEMICON West 2016 is a great forum to work together through the key convergence issues as well as to set the agenda for next steps on our shared goals," said Denny McGuirk, president and CEO of SEMI. "SEMI and MSIG started with a joint survey on MEMS, sensors and semiconductors in early 2015 and immediately found traction among industry players. With its focus on industry realities like consolidation and the extended supply chain, this workshop takes on the key intersections and inflections."

MSIG Chief Strategy Officer Steve Whalley and SEMI Vice President of Product Management and Business Development Bettina Weiss will co-chair the joint workshop. The agenda features:

- **Keynote:** Leveraging M&A in a Converging Semiconductor and MEMS/Sensor IoT World, Greg Mischou, senior partner, Woodside Capital Partners, LLC
- **Panel discussion** with panelists from:
  - A.M. Fitzgerald and Associates
  - Electronic System Design Alliance
  - FlexTech
  - Lam Research
  - Woodside Capital Partners
- **Breakout Sessions** — breakout groups will report on specific actions that companies can take to address these challenges/opportunities.

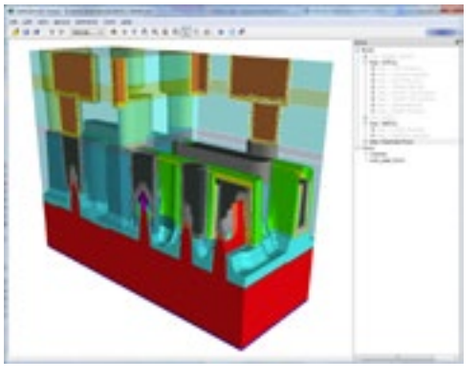
MSIG and MSIG member companies will be on the show floor at SEMICON West. Visit MSIG in Booth N4 or visit http://msigevents.org/semicon-west-2016 for a list of MSIG exhibiting member companies and partners.

The MSIG and SEMI joint workshop takes place July 13, 2016 from 1:00-5:00 p.m. at the San Francisco Marriott Marquis, 780 Mission Street.

The 2016 "Best of West" Award Finalists

Each year at SEMICON West, the "Best of West" awards are presented by *Solid State Technology* and SEMI. More than 700 companies exhibit at SEMICON West and 26,000+ professionals attend, from the electronics manufacturing supply chain. The "Best of West" award was established to recognize new products moving the industry forward with technological developments in the electronics supply chain.

The Best of West 2016 Finalists will be displaying their products on the show floor:



Coventor: SEMulator3D — A 3D semiconductor process modeling platform that can predicatively model any fabrication process applied to any semiconductor design. Starting from a "virtual" silicon wafer, the product performs a series of unit processes like those in the fab to create highly accurate 3D computer models of the predicted structures on wafer. *(Facilities and Software category; Booth #2622)*

CyberOptics: WaferSense® and ReticleSense® Auto Multi Sensors (AMS) — Wireless sensor devices capable of multiple measurements (leveling, vibration and relative humidity) to save time and expense while improving yields. WaferSense AMS travels through virtually any tool with its thin and light form factor, while ReticleSense AMSR has the same measurement capabilities in a reticle shaped form factor. *(Metrology and Test category; Booth #2323)*

Graphenea: Graphene Integration on CMOS-Fab — Allows large-scale manufacture of 200mm CMOS-compatible graphene wafers (SEMI Standards), with low metal contamination levels. The industrial production method will produce uniform, large-scale/high-performance graphene in high yields and a reliable manner. *(Advanced Materials and Materials Management category; Booth #632)*

Kulicke & Soffa Industries: IConn MEM PLUS High Performance Wire Bonder for Memory Devices — A new high-performance memory device bonder for gold and silver alloy wire bonding. With its advanced process, looping, overhang control and ease of use capabilities, it delivers high quality and productivity benefits in complex multi die stack package applications. *(Assembly/Packaging Solutions category, Booth #6060)*

Rorze Automation: Rorze N2 Purged LP — Maintains low humidity during critical steps. A typical bottom purged LP can only offer control of an average of 30 percent RH. However, N2 purge LP from Rorze (patent pending) can offer a humidity control that is better than 5 percent. *(Components and Subsystems category; Booth #1613)*

SPTS Technologies (an Orbotech company): Rapier-300S — A production silicon DRIE module, designed specifically for dicing of 300mm wafers mounted on 400mm frames. It builds on SPTS experience in plasma singulation of framed 150mm and 200mm wafers, and employs patent-protected end-pointing and process control techniques, critical to delivering stronger die than traditional dicing methods. *(Assembly/Packaging Solutions category; Booth #1417)*

The Best of West Award winner will be announced during SEMICON West on Wednesday, July 13, 2016.

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