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Chemical Mechanical Planarization
Historical Review and Future Direction

Gautam Banerjee and Robert L. Rhoades
Air Products and Chemicals, Inc., 1331 West Houston Avenue, Gilbert, AZ 85224
Entrepix, Inc., 2315 West Fairmont Avenue, Tempe, AZ 85282.

ABSTRACT

The advances in interconnection technology have played a key role in allowing continued improvements in manufacturing of an ever expanding list of semiconductor devices. Chemical Mechanical Planarization (CMP) is a key enabling technology to generate extremely flat and smooth surface at several critical steps in this manufacturing process flow. From the time CMP was first introduced two decades ago to flatten/planarize oxide inter-level dielectric layers, it has come a long way and is now used for tungsten for contacts or vias, for shallow trench isolation and for copper interconnects in dual damascene architecture. Along the way, many integration schemes now require the use of other low-k dielectric films, all of which are planarized using CMP process. In this review paper, various factors influencing CMP will be discussed. The discussion will focus on material challenges to develop consumables such as pad, slurry, post CMP cleaning solution etc. and the challenges for integrating different material stack including the cost of ownership issue. The authors will also provide some direction related to new applications under development and future potential direction.

INTRODUCTION

The driving force in the semiconductor industry continues to be relentless pursuit of higher performance and lower unit costs. An impressive series of process innovations, including chemical mechanical planarization (CMP), has enabled this trend for nearly four decades. At various steps in processing a silicon integrated circuit (IC), surface topography from underlying layers can cause yield-limiting problems for the next process step. CMP emerged as the premier method for achieving ultra-flat surfaces when they are most critical, thus enabling many of the advanced electronic devices currently in production.

CMP became a mainstream process at and below the 0.35um technology node. The first high volume processes were oxide CMP for ILD planarization and tungsten (W) CMP for contacts and vias. Since then the number of materials being polished in various CMOS process flows has steadily grown as shown in Figure 1.

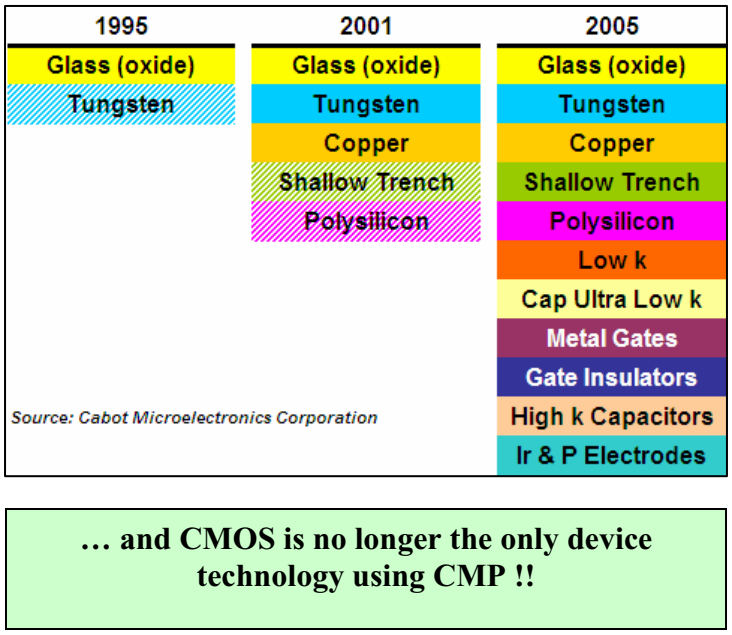

Figure 1: Various film stacks polished using CMP in CMOS Technology

Table 1 below lists the technology node and the year in which the manufacturing of key CMP processes was introduced at Intel Corporation[1].

Node	Year	CMP	Enabling
0.8 µm	1990	ILD	Multilevel metallization
0.35 µm	1995	STI	Compact isolation
		PSP	poly-Si patterning
		W	yield/defect red.
0.18 µm	1999	SiOF ILD	RC scaling
0.13 µm	2001	Cu	RC scaling Electromigration
90 nm	2003	SiOC ILD	RC scaling
65 nm	2005		
45 nm and beyond	2007	unknown	

Table 1: CMP Enabling Intel Technologies

A complexity involved with CMP is that each material generally requires unique slurry, a properly designed pad, optimized process settings for both polish and post-CMP clean, and other factors that must be individually tailored to the application. Successful results are achieved only when all the pieces of the puzzle fit together [Fig. 2].

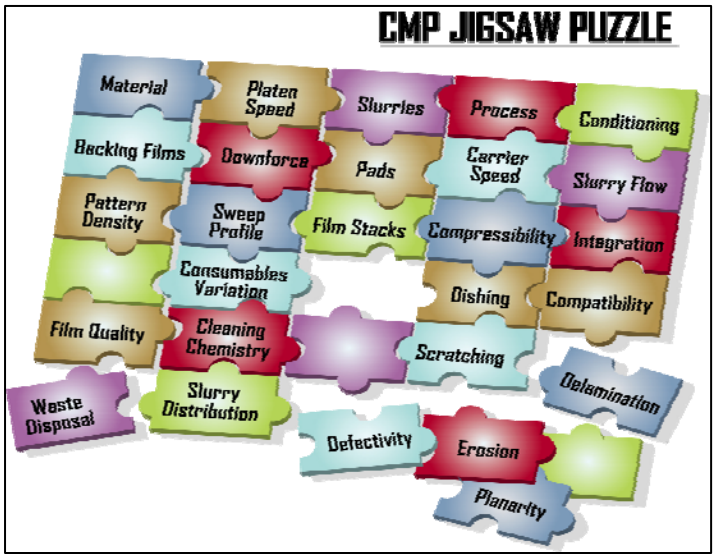

Figure 2: Various factors responsible for achieving successful CMP results

HISTORY

The first widespread application of CMP was the planarization of inter-level dielectric oxide layers. The topography resulting from lower levels of patterned films can create a very non-planar ILD surface, which creates severe difficulties for at least three subsequent process steps: photo, metal deposition and metal etch. [2] The depth of focus (DOF) at photolithography is a direct function of the illumination wavelength and sets an upper limit on surface height variation that can be accommodated and still maintain crisp feature definition. In order to print smaller features, topography had to be reduced. A second problem was poor sidewall step coverage at the next metal deposition. Finally, metal etch required excessive over-etch for complete removal of metal stringers at the bottom inside corners. All three of these factors became virtually impossible to solve with existing techniques at the 0.35 micron technology node, thus oxide CMP was born.

After the successful introduction of ILD CMP, a flood of new CMP steps was introduced in 1995 with the 0.35-mm node technology. Shallow trench isolation (STI) CMP significantly improved FEOL planarity and also compacted the area required for isolation by eliminating the bird's beak characteristic of the LOCOS (Local Oxidation of Silicon) isolation step that was displaced. Poly-Si polishing (PSP) enabled sub- 0.5-mm poly-gate patterning by further reducing FEOL topography. Tungsten (W) CMP improved back-end-of-the-line (BEOL) defect densities by replacing W etch-back processes, a notoriously defect riddled process.

In 2001, the long anticipated conversion from aluminum metallization to copper metallization occurred, yielding lower interconnect resistance and higher immunity to electro-migration. Because of the lack of suitable copper etching processes, Cu CMP was introduced as a necessary replacement to subtractive etching processes. Borrowing from

STI CMP the concept of patterning using inlaid structures, Cu metallization patterns were delineated by CMP using the so-called damascene patterning method [Fig. 3].

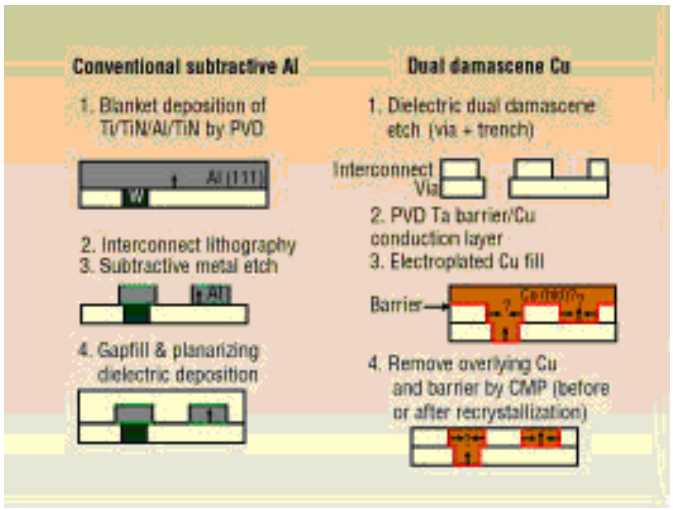

Figure 3: Comparison between conventional Al interconnect and Cu dual damascene

Basic terms and failure modes associated with Cu CMP are shown in Figure 4. [3]

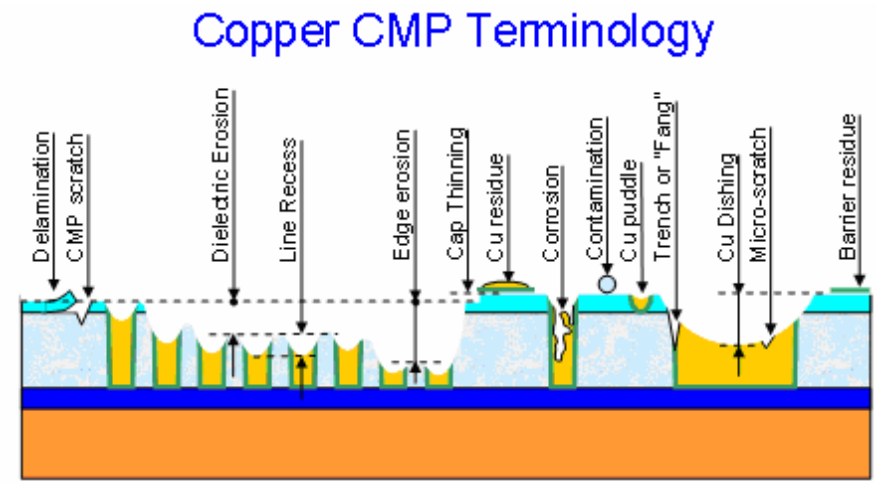

Figure 4: Basic failure modes for Cu CMP

The 1990s saw not only the birth of the CMP technology but also the greatest innovation in the CMP industry. As a result of the fast pace of innovation and introduction of new CMP processes, the CMP industry grew rapidly outpacing even the growth rate of the semiconductor industry as a whole (Fig. 5)[4].

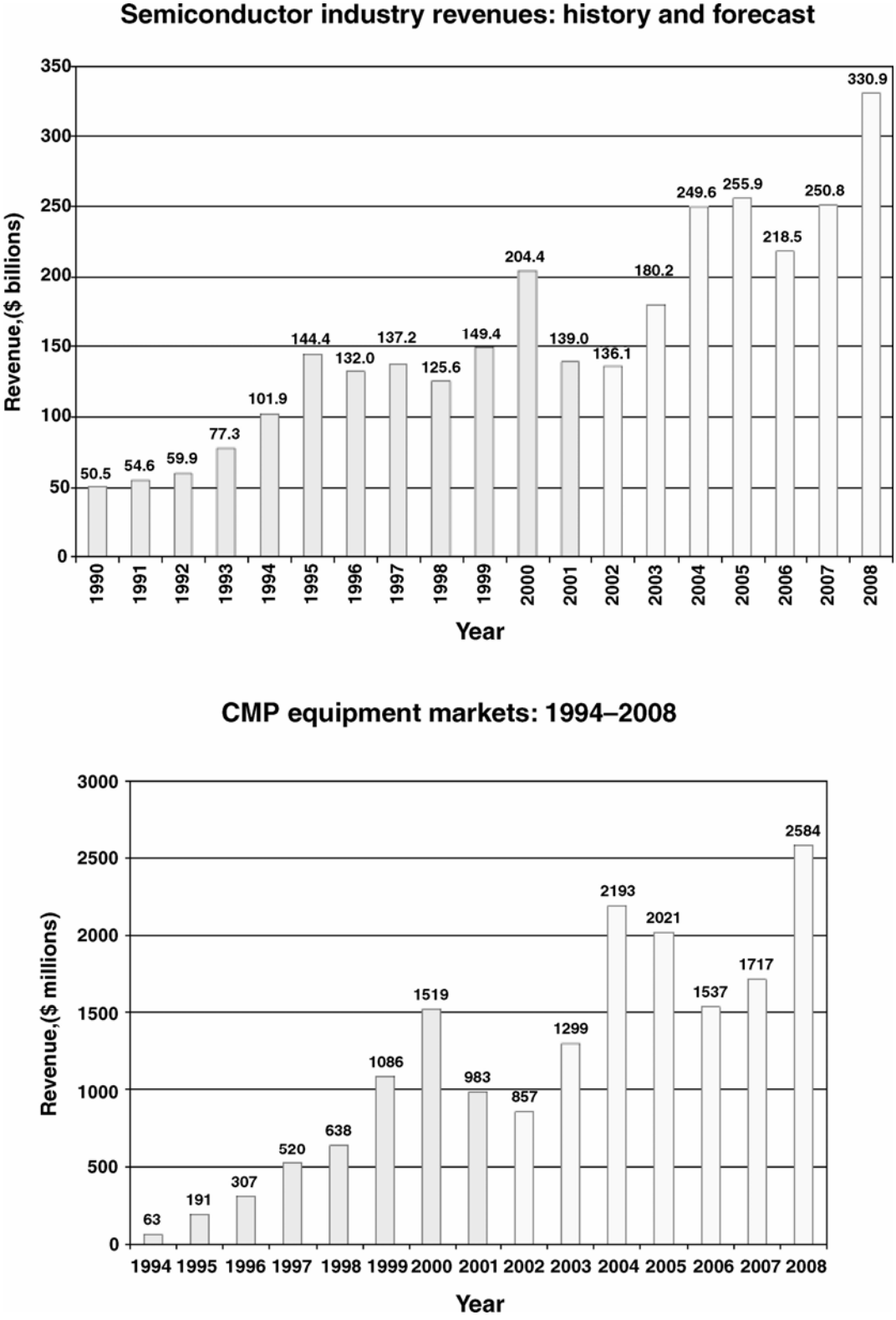

Figure 5: Growth of semiconductor industry and CMP industry revenues (from Ref. 1). Years 1994–2001 are actual data. Years 2002–2008 are projections.

THEORY & LENGTH SCALES

Many theoretical models of CMP are based on or derived from a simple equation known as Preston's Law, which states that removal rate is linearly proportional to the product of pressure and velocity. This "law" provides a reasonable model for mechanical wear, but is not adequate for CMP. It does not account for chemical effects, such as etching, reaction thresholds, depletion/saturation, temperature sensitivity, or electrochemistry (in metals). It also does not account for non-linear fluid dynamics, particle-surface interactions, tribological effects, time-dependent pad surface wear, pad conditioning, polymer properties, and more. [5, 6, 7]

A recurring complexity of CMP is pattern density sensitivity. Simply stated, pattern density is the fraction of high area to total surface area. For oxide CMP, this is driven by the underlying metal. For other layers, high may refer to field areas between recessed features. The rate at which high features are removed is proportional to the effective contact pressure which equals the average pressure divided by the local pattern density. The region considered "local" is a direct function of planarization length which is roughly the lateral distance required for relaxation of deflections in the pad surface. The impact of pattern density variation can be dramatic as shown in Figure 6 for a typical oxide CMP process. The commercially available test wafer is based on line-space patterns in 4mm x 4mm arrays with constant pitch and varying linewidths[8]. Initial step height of all features was 8 kA and data points were taken at the center of each array.

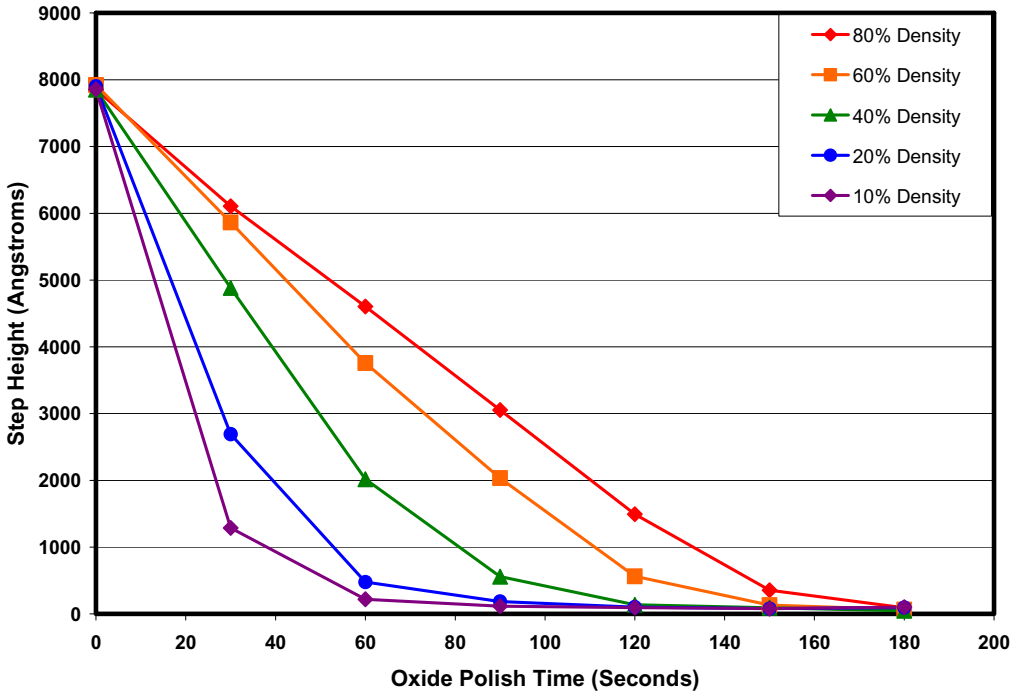

Figure 6. Step height as a function of oxide CMP polish time for structures with differing pattern densities.

All of the features were planarized by the end of polish (step height near zero), but a substantial difference in oxide remaining was induced by the pattern density variation. Oxide thickness remaining over the lines in the 80% array was just over 11 kA while the oxide remaining over the 10% array was less than 8 kA – a difference of over 3 kA! This difference is nearly equivalent to the blanket film removal rate for a period of 100 seconds which is how long the 10% array was polished after reaching local planarity.

One final thought experiment illuminates the relative sizes and scale lengths involved in CMP. Imagine a world in which 1 micron is scaled up to one inch (2.54 cm). A typical slurry particle (actual diameter about 100nm) would be scaled up to 0.1 inches, or roughly the size of a large grain of sand. The approximate size of other relevant physical CMP elements are shown in the table 2 below. With this upscaled world in mind, it may be easier to understand why CMP is considered a dark art. It is like planarizing an airport with bumps ranging from toothpicks to tool sheds by pressing it against a spinning polymer city flooded with chemical soup.

Slurry particle	0.1	um	0.1	inch	BB or large grain of sand
Pad asperity	10-40	um	10-40	inches	Basketball to laundry basket
Planarization length (typical)	4	mm	333	feet	Length of a soccer field
Diamond on a conditioning disk	80-150	micron	7-12	feet	Compact car
Device - minimum feature size	65	nm	0.065	inch	Diameter of a toothpick
Device - metal line thickness	500	nm	0.5	inch	
Device - bond pad	100	micron	8.33	feet	Tool shed footprint
Width of one average die	12	mm	1000	feet	3.3 soccer fields end-to-end
200 mm Wafer	200	mm	3.16	miles	Area covered by average airport
300 mm Wafer	300	mm	4.73	miles	Area covered by large airport
Polishing pad diameter	20-30	inches	8	miles	Area covered by a small city

Table 2: Table of relative sizes if 1 micron were upscaled to 1 inch

PROCESS ISSUES

Virtually any CMP module can be described by a series of events.

1. Deposit desired film or film stack onto the device side of wafer
2. Load unprotected wafer into rotating carrier (device side down)
3. Flow slurry (mixture chemicals and trillions of suspended particles) onto large diameter rotating polymer pad

4. Lower wafer onto pad and apply a controlled pressure ranging from roughly 50 lbs to several hundred pounds
5. Polish until sufficient amount of the film stack has been removed
6. Clean up mess left behind on wafer surface

One challenge is that interactions between process settings and output metrics are not simple to predict. They are seldom linear and they strongly depend on slurry, pad, film stack, process recipe settings, and design rules of devices being polished. However, certain trends generally hold true as summarized in table 3 below.

	CMP Process Metrics			
Process Settings	**Rate**	**Uniformity**	**Defectivity**	**Planarization**
Down force, DF	**STRONG**	**weak**	**Moderate**	**STRONG**
Back pressure, BP	**weak**	**Moderate**	**weak**	**weak**
Table speed, TS	**STRONG**	**weak**	**Moderate**	**STRONG**
Carrier speed, CS	**weak**	**Moderate**	**weak**	**weak**
Slurry flow, SF	**nonlinear**	**nonlinear**	**Moderate**	**weak**
Conditioner force	**weak**	**weak**	**weak**	**Moderate**
Conditioner speed	**don't care**	**don't care**	**weak**	**weak**

Table 3: Output metric interactions with process recipe settings

One of the biggest concerns in IC manufacturing is killer defects. Over a span of four decades, the industry has spent billions of dollars and thousands of careers battling the forces of defectivity. Slurries have trillions of particles that MUST be removed before wafers leave the process bay. Numerous approaches have been attempted for post-CMP cleaning, but the most popular involve immersion in a megasonic bath or double-sided scrubbing with PVA brushes or both. These processes utilize post-CMP cleaning chemistries formulated for the exposed materials and slurry particle type. Beyond slurry particles, wafers are vulnerable to other defect mechanisms during CMP. Particle size distribution must be tightly controlled in both manufacturing and slurry handling systems to avoid large agglomerates that can scratch the surface. Chemistries of the both slurry and post-CMP clean must be controlled to avoid pitting or surface roughening. Buried defects that were initially not observable can be uncovered during CMP which requires more troubleshooting.

In addition to the general concerns, each CMP process has unique issues. For oxide CMP, the polish begins and ends in the same material unlike most other CMP processes. This makes repeatability and control important since variations in polish rate or uniformity translate directly into oxide thickness. Pad conditioning is key to process stability. Proper pad surface texture is required for optimal removal rate and uniformity, but establishing this texture once at the beginning of pad life is not sufficient. Each cycle

tends to wear down the high points (called pad asperities) [Fig. 7] and polishing byproducts tend to form a "glazing layer" on the pad. Pad conditioning counteracts both of these effects, but overly aggressive conditioning cuts away more pad than necessary and artificially shortens pad life.

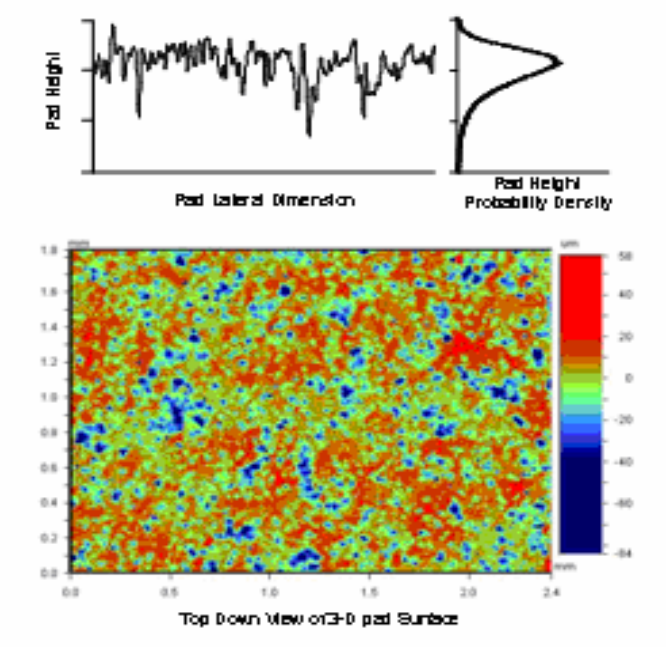

Figure 7: Pad Asperities [9]

Tungsten CMP generally runs at higher pressures and relatively aggressive settings which tends to shorten pad life. The process also generates higher pad temperatures and thermal variations can translate into process instability. The pad life extension can be achieved using new generation pad cleaning chemistry which reduces the aggressive use of pad conditioning disk after each wafer is polished[10]. Failure mechanisms on device structures include erosion and plug coring. Erosion is array thinning of densely spaced plugs due to mechanical wear of the oxide stop layer. Coring is a term used to describe undesired etching of weak plug centers by slurry chemistry, which can lead to high contact resistance or electrical opens affecting both yield and potentially reliability of finished devices. Appropriate post CMP cleaning methodology can prevent plug coring as is seen in figure 8 [11] next page.

STI CMP is similar to oxide CMP in that silicon dioxide is the primary material being polished, but with very different performance requirements. Successful completion of the STI module requires that CMP fully remove oxide over all nitride features (active areas) without breaking through nitride anywhere. With nitride layers typically only a few hundred Angstroms, this is a significant challenge, especially if attempted with traditional oxide slurries with only about 3 to 1 selectivity. Pattern density variation renders this approach nearly impossible if small isolated features and large or dense structures exist in the same die. The preferred solution today is slurries specifically formulated with extremely high selectivity to nitride[12].

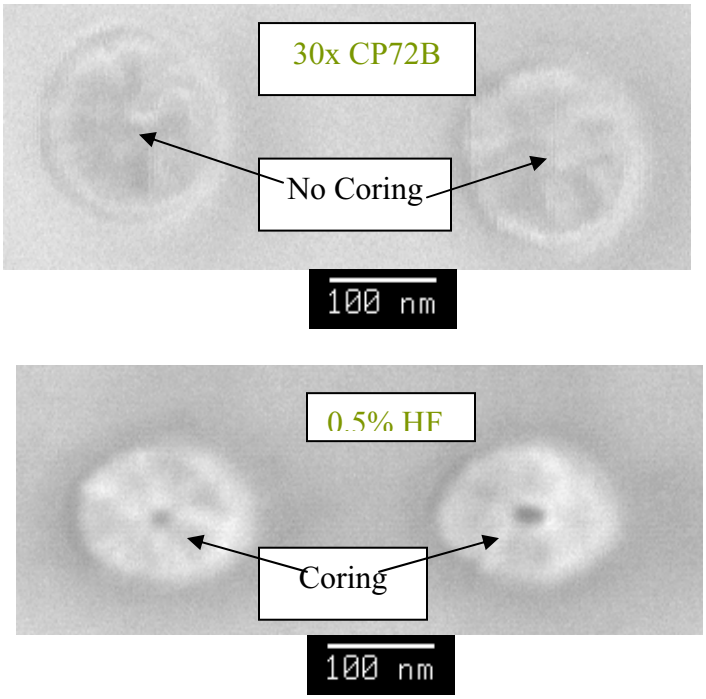

Figure 8: SEM images of plug structures processed with different chemistries

Copper CMP is the last mainstream process to be considered and is arguably the most complex. Cu is highly reactive and has a tendency to scratch, corrode, etch, or form a galvanic cell with other metals in many aqueous chemistries. From beginning to end of the polish sequence, the surface goes from being 100% Cu to a blend of 2 metals to a composite surface with both metals and the underlying dielectric exposed. All factors that could damage the Cu surface must be controlled throughout the sequence.

An optimized CMP process depends on several key factors such as removal rates of the film being planarized, adhesion stability of the film, minimum or no defect such as scratch or pit formation on the film, corrosion in the case of Cu film, adhesion of organic or inorganic surface residues formed during the CMP process, etc. It may be noted that the pad, slurry, particular tool used and the pattern on the wafer etc. – all contribute to the final outcome. Usually, the Cu-CMP process consists of the major steps as shown in Figure 9.

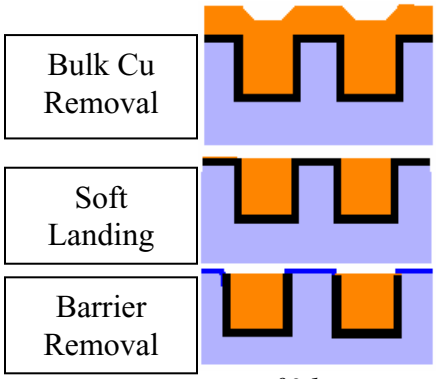

Figure 9: Schematic representation of 3 key steps in the modern Cu-CMP process.

First, a selective slurry is used to remove Copper layer down to the barrier layer. Sometimes, even two slurries are used. The first one removes the bulk Cu layer at a relatively high rate while the second slurry is used to achieve final planarity of the surface with a relatively lower Cu removal rate. The slurry used in this step does not damage the Ta barrier layer or the dielectric film layer, if the slurry comes in contact with the dielectric layer due to any damage to the barrier layer.

Once the barrier layer is exposed and the Cu film is almost removed, another slurry is used which helps to remove the barrier layer (most common is Ta) without damaging the Cu or the dielectric film layers. After the barrier layer is removed from the top surface, due to the nature of the process, there will always be two major defect issues – dishing and erosion. In the case where a low-k dielectric film replaces silicon dioxide as the dielectric layer, the field oxide loss will be field-dielectric loss.

The goal of an optimized CMP process is to minimize the dishing and erosion without compromising the removal rates of the different layers and at the same time, achieve the lowest overall defect counts. Among the various defects, the most important are scratches (formed by the agglomerated particles or debris generated during the CMP process), corrosion of lines (due to galvanic corrosion when exposed Cu/Ta forms a galvanic couple in the slurry), fangs in the trenches (may be a combined effect of mechanical stress and galvanic corrosion), organic residues on surface (due to strong adsorption of the corrosion inhibitor from the slurry on Cu surface).

The agglomeration of abrasive particles is preventable by adjusting the slurry pH to ensure the zeta potential of the abrasive particles remain stable during CMP. When a pattern wafer is polished to the barrier layer, it is essential to adjust the slurry formulation so that Cu behaves as electrochemically noble to Ta in order to prevent galvanic corrosion. In a slurry where Cu was active to Ta, fang formation was observed to occur after barrier CMP (Figure 10).

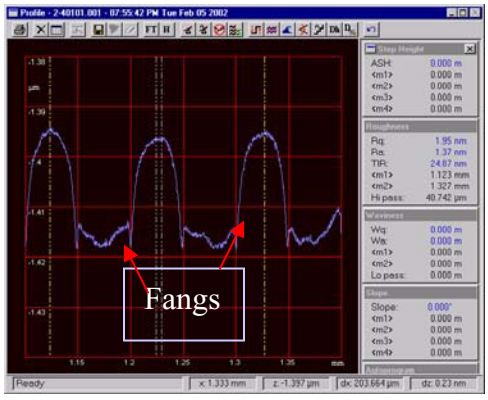

Figure 10: Atomic Force Profile of a pattern wafer (MIT 854) after barrier CMP showing fang formation in the trenches [13].

By adjusting the slurry chemistry in which Cu became electrochemically noble to Ta, not only the galvanic corrosion of Cu line was prevented, the fang formation effect was also prevented as is evident from Figure 11.

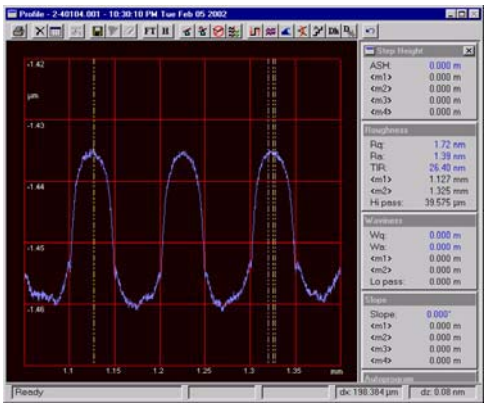

Figure 11: Atomic Force Profile of a pattern wafer (MIT 854) after barrier CMP, showing no fang formation in the trenches [13].

In addition to minimizing dishing, erosion, corrosion etc., optimized slurry also can be formulated to have desired rates of removal for different film layers. While a slurry formulated for Cu layer removal is usually very selective for Cu and have minimum or negligible removal rates for other film layers in the stack, a barrier layer removal slurry may be either selective or non-selective depending on the process requirements.

POST-CMP CLEANING

Post CMP cleaning is an integral part of the CMP process module to clean up the debris and other chemical residues left on wafers during CMP. There are two types of cleaning technology in use: megasonic bath and double-sided scrubber with PVA brushes. Both have advantages and disadvantages and may be employed individually or in combination as needed to achieve effective cleaning of the wafers. The megasonic approach is sometimes useful in removing particles from narrow recesses of a polished wafer if the surface features are not completely coplanar. Brush scrubbers, on the other hand, are particularly useful at dislodging particles that may be physically attracted to the copper surface. It is relatively common to use the combination of both megasonic cleaning and brush scrubbing to give a more robust cleaning process. There are cases of fabs using only one technique and the more common single method is brush scrubbing. This practice is still possible due to new generation of cleaning chemistries which enable complete removal of particles from the copper surface through chemical and electrochemical means without the need of megasonic energy to physically lift the silica particles out of copper surface.

The technology of using chemistry and electrochemistry to remove particles from a copper surface has become necessary to address the constantly shrinking size of what are

considered "killer" defects. In general, this includes any particle greater than the linewidth of the smallest feature, which is now smaller than the particle sizes used in most commercial slurries. Silica particles, for example, will stick on the metal surface by electrostatic bonding if the slurry is acidic in pH. In this case, silica acquires a net positive charge while the surface charge of copper becomes negative. The electrostatic bonding is fairly strong and traditionally, megasonic energy was needed to lift the particles off the copper surface. With the new generation of acidic post-CMP cleans, the particles are lifted off the copper surface by a very slight etching of underlying copper which is not enough to damage the copper surface topography. In contrast, if alkaline slurry is used for the final step in the CMP process, the silica becomes negatively charged and floats near the copper surface. It becomes easy to remove these particles, either by an alkaline or acidic cleaning chemistry, as there is no significant particle-surface attraction. Surfactants can also be useful to form a layer around the particles which assists in not only removing them from wafer surface, but also preventing their re-deposition.

While concern for CMP defects is not new, their impact and the concern for them are likely to be greater in the next 15 years. Rapid yield learning during the development cycle has become a critical factor to getting a technology to market quickly, and high product yields during the manufacturing cycle are the key to keeping product cost low. Processes that limit yield learning or manufacturing yield levels due to high defects are not likely to be selected for inclusion into new technologies. Thus, for new CMP processes to make it from research to manufacturing, CMP defects must become a top consideration.

Most of the low-k and ULK films are hydrophobic in nature. In order to efficiently clean particles as well as trace metals and organics off the surface of the wafer, it is essential to make the film hydrophilic, at least temporarily, to enable the smooth flow of aqueous cleaning solution followed by rinse water. This is also necessary to avoid leaving water marks. When the dielectric is made temporarily hydrophilic with a wetting agent in order to clean the surface, there is often a concern about damaging the dielectric properties, especially since uncapped dielectric film is now in use. The following example shows that for non-porous dielectric films, a well formulated post-CMP cleaning chemistry does not change the film properties before and after cleaning (Figure 12).

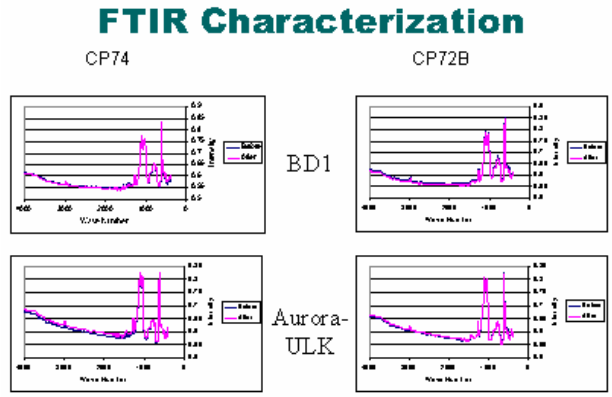

Figure 12: No Damage to Dielectric Films after post CMP Cleaning[14]

Even for porous low k film such as PDEMS, where a cap layer needs to be used, there are concerns about what impact will be if the cap layer is breached. Experiments performed on uncapped PDEMS ULK suggest that there is a slight shift in k-value and modulus when processed with a standard post-CMP cleaning process. However, a post cleaning technique was developed to drive out the liquid that penetrates the surface pores of the film. After this step was performed, the PDEMS returned to its normal properties with no apparent residual effects (Figure 13).

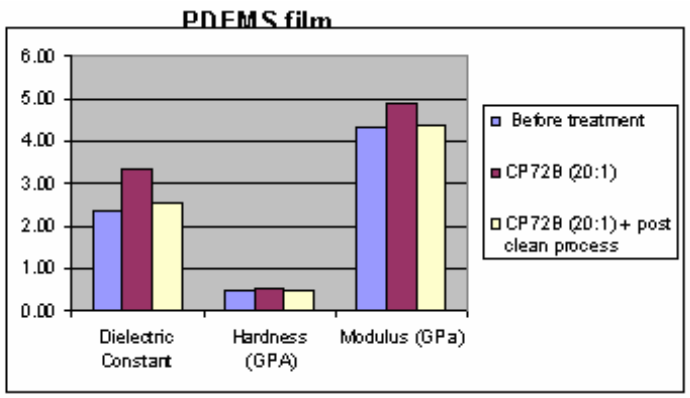

Figure 13: Effect of CoppeReady® CP72B on PDEMS Film[15]

A novel approach to dealing with porous ULK materials in the CMP process module is to delay the formation of the pores until after the entire CMP process module is complete. Several companies are investigating this delayed removal of the porogen as a possible means to not only avoid the liquid penetration issues, but also provide additional mechanical stability for the film stack during polish.

INTEGRATION

The interconnect metal of choice for at least a few more generations of advanced devices appears to copper. Targets for dishing and erosion of Cu lines continue to decrease. According to the ITRS roadmap, maximum allowable Cu line thinning in an array is already less than 15 nm and is projected to be only 6 nm by the 32 nm node.[16] Achieving this target consistently in manufacturing will require slurries formulated to specific materials, pads with excellent surface texture control, and processes with razor-sharp endpoint and/or high selectivity to a stop layer.

The dielectric film stack appears to be the next battleground for improving interconnect speed. For most 65 nm process flows, CDO-based materials are the dominant choice for low-k dielectrics. However, they are not porous and the effective k-value is >2.5 in most cases. At the 45 nm node currently being developed, integration activities seem largely focused on extending the 2nd generation modified CDO films, preferably without introducing porosity if it can be avoided. It remains to be seen how low the effective k-value can be pushed and what speeds can be achieved through this approach. As the

industry moves forward into the 32 and 22 nm nodes, it is expected that devices will require ultralow-k (ULK) dielectric with k-value < 2.5 to achieve the desired performance targets. Issues of water absorption and chemical retention during CMP and post-CMP cleaning with porous ULK materials appear to be driving most integration teams to include a capping or sealing layer. Unfortunately for CMP, all known ULK materials have a strong trend of lower mechanical strength with lower k-values, primarily due to required porosity. Typical mechanical failure modes include delamination, cracking, and inelastic deformation. As the industry transitions to these materials, the CMP process must accommodate mechanical fragility of ULK by moving toward lower pressure and lower shear process recipes. Most copper and barrier polishing work for these applications is now focused at 2psi and below, with some targets as low as 0.5 psi.

A properly designed integration effort can achieve lowest defects and good compatibility with porous low-k film. At Air Products and Chemicals, Inc., for example, focus is to have a common clean to achieve cleaning performance on various barrier slurries as well as barrier metal based Cu pattern wafers. Figure 14 shows the efficiency of a good clean formulation to clear particles and organics in sub 50 nm level.

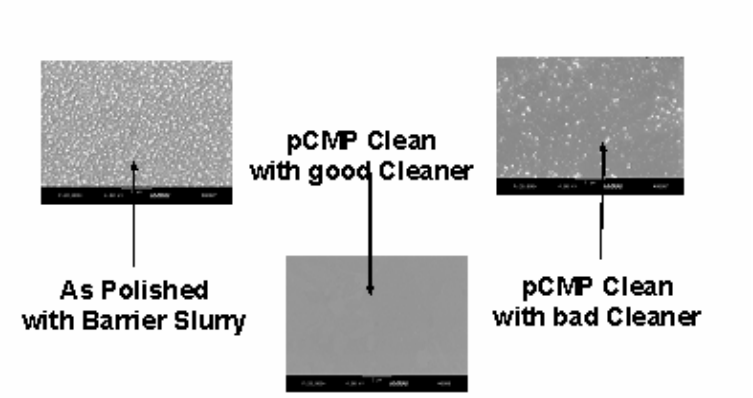

Figure 14: Post CMP cleaning performance comparison on Cu wafers[17]

Further, porous low-k dielectric films (PDEMS®) have been characterized after CMP and post CMP cleaning. For uncapped films, the k value initially increased due to trapping of the cleaning solution but could be restored back close to the original k value by extracting the trapped solution [Figures 15 and 16].

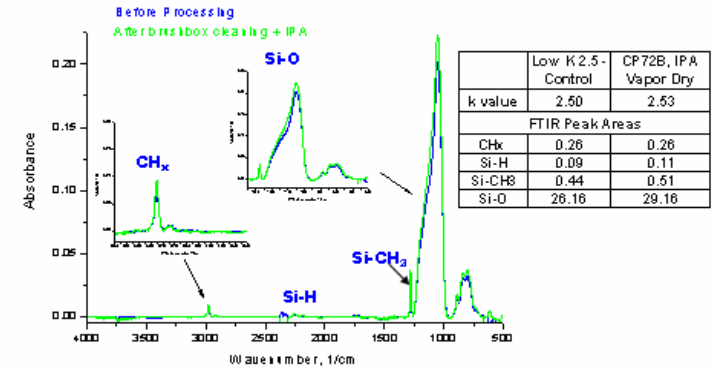

Figure 15: FTIR Spectra of CoppeReady® CP72B on PDEMS® (k=2.5)

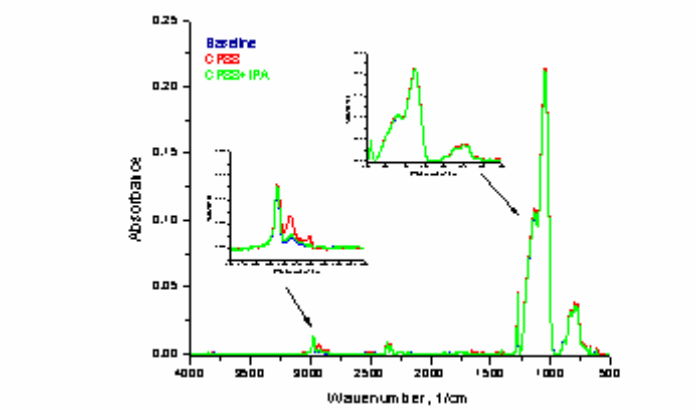

Figure 16: FTIR Spectra of CoppeReady® CP72B on PDEMS® (k=2.2)

NEW APPLICATIONS FOR CMP

Now that CMP is established as mainstream for advanced CMOS manufacturing, other technologies are attempting to leverage CMP to achieve the performance they need. These applications represent emerging growth areas and often hold significant planarization challenges of their own. Analog, mixed signal, and even power devices are now investigating advantages that can be realized in their unique process flows. Advanced packaging concepts and through silicon vias (TSV's) represent two more areas where planarization is key to successful technology deployment.

MEMS (micro electro-mechanical systems) are frequently constructed with alternating polysilicon and oxide layers. Compared to CMOS, the topography encountered in MEMS is generally much larger in all dimensions. Step heights up to tens of microns and feature sizes of several hundred microns are common. Polish times are long which exaggerates issues of pattern density and process instability. Slurry manufacturers are developing slurries specifically to address the growing MEMS market.

The development of engineered substrates and custom epitaxial layers has accelerated in recent years, especially SOI, SiGe strained layer structures, and various III-V and II-VI compound semiconductors. Many of these technologies require unique new polishing processes to achieve smooth, low-defect, device-ready wafers.

Direct wafer bonding is a growing trend that encompasses efforts to bond virtually anything-on-anything. The technical challenge often arises in getting the two surfaces smooth enough to achieve a good bond, which generally means Ra values less than 1 nm.

FUTURE DIRECTIONS

The need for the CMP processes arose as a direct result of shrinking circuit dimensions. Figure 17 (next page) shows that Intel's release of recent technologies is on pace with 2-

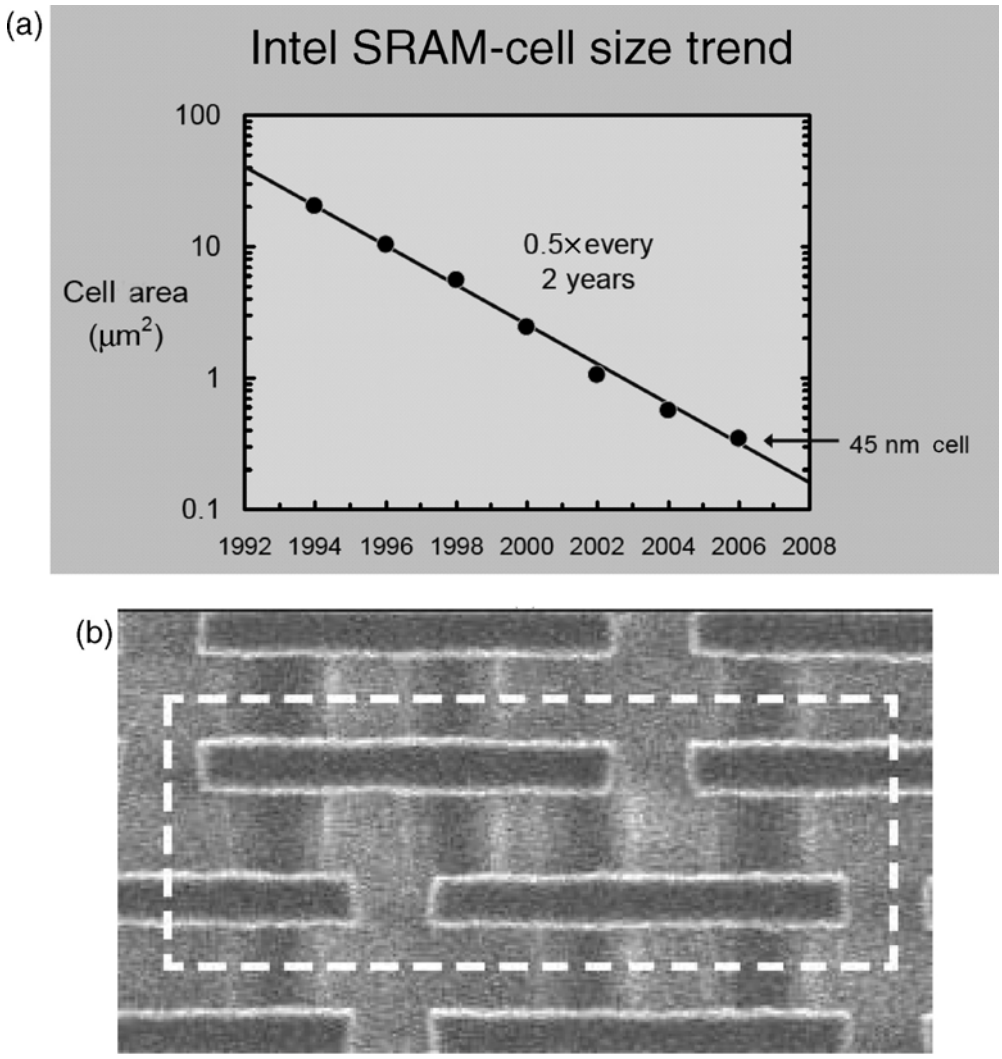

FIGURE 17: SRAM-cell size is a key metric of scaling for microprocessor technologies. Intel Corp. maintains a 50% aerial shrink of SRAM cell with each technology - (a). 45-nm technology SRAM cell (b) is the latest addition to the trend. The dotted line represents the six transistor cell—horizontal lines are the MOS gates and the vertical lines are diffusion regions

year schedule of density scaling[18]. The question for the CMP technologist is what are the future challenges to the IC industry and will CMP be used to meet those challenges? CMP is one of the most expensive unit processes in IC manufacturing today from the viewpoint of any fab although from the viewpoint of consumable suppliers, the margins are too low and that the business is barely profitable. So how is it that the process costs too much yet the suppliers are not making larger profits? The reason is that the run rates and availability of CMP tools are low compared to other process tools and the consumption of consumables is high. Therefore the CMP process is not efficient. CMP cost is split between capital cost (cost of CMP tools and slurry delivery tools) and cost of consumables (pads, slurries, and consumable parts). By increasing the run rates (number of wafers processed per hour) of tools, both capital cost and cost of consumables can be

decreased. Higher run rates require fewer tools, fewer tools require fewer consumables. Consumable cost can be further cut by extending the lifetime of consumables (if a pad can be made to last twice as long, then the pad cost will be cut in half) or the consumption rate of consumables (slurry flow rate, for example). If the CMP market is to grow, it will grow because of the increased usage of CMP in the process flow. In the future, most of the potential new usages of CMP will be discretionary because techniques using CMP must compete with techniques not using CMP. As the IC industry focuses on cost, the techniques that will survive the research and path-finding phases will be the techniques that deliver the technical solution at an acceptable cost [1].

Semiconductor manufacturers are required to manage the economic aspects of their business in addition to technology. The goal of delivering products to their customers in spec, on time, and at the lowest reasonable cost involves managing both production capacity and new product development. When demand for any product ramps, one solution to increasing output is outsourcing to dedicated foundries for additional wafer capacity. Commonly referred to as the 'fab-lite' or 'asset-lite' model, this allows companies to increase wafer output beyond internal capacity limits during periods of high demand while eliminating risks of carrying stranded capital during periods of weak demand. This option can be utilized for full flow processing as well as constraints at a specific process step, such as CMP. In addition, companies can outsource a portion of CMP engineering projects to a capable outsource provider. These external resources can then provide the staff, expertise, time on process tools, and metrology execute projects that might otherwise compete with available production resources in the fab.

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