LEAD-FREE MULTILAYER DIELECTRIC SYSTEM FOR TELECOMMUNICATIONS

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ABSTRACT

A totally lead-free, low loss multilayer materials system was developed for telecommunication applications. It includes cofireable silver based conductors, embeddable ferrites for inductors and embeddable dielectrics for capacitors covering a K range from 18 to 265. The LTCC tapes in which these materials can be buried are available in K values of 4, 7.5 & 13, so that one can choose whether they want the speed and isolation advantages associated with low K or the size and cost advantages associated with high K. Meeting the cost target was addressed by using low cost raw materials, parallel processing and low firing temperatures.

INTRODUCTION

There is a common desire among designers of telecommunication systems to provide more functions in an equal or smaller space. They want to do this using proven manufacturing procedures while lowering overall costs. The LTCC based approach is an excellent way to achieve this goal. [1] It is a flexible technology with proven reliability in which one can increase functionality by burying components. In addition, low loss dielectrics and conductors are available providing the desired increased battery life for portable devices.

It was recognized at the onset of this program that even with all the performance advantages associated with LTCC, the device cost was going to be the factor determining its success. With this in mind a number of features were built into the program.

Material costs were reduced by using silver based conductors while manufacturing costs were kept in check by using parallel processing methods to form the modules. In this scheme the printing, hole punching and tape sizing operations are done to the various tapes in parallel. The processed tapes are then inspected before they are brought together for lamination and a final cofiring step. Schemes like this are routinely used to make reliable capacitors of 50 layers or more for less than a penny [2].

There is another advantage LTCC has over PC boards that translates into cost savings. This relates to the variety of materials which can be used in the LTCC approach. The LTCC system includes high K dielectrics and ferrites, that bring about reduced component sizes which usually result in lower overall costs.

This improved LTCC approach is highly reliable. It uses (1) metal ion diffusion inhibiting dielectrics, (2) sintered metal interconnects and (3) has mechanically and electrically stable structures. The high reliability affects cost in that dissatisfied customers and/or returned parts affect the bottom line.

One of the issues which was a subject of considerable debate early on in the program was whether lead containing materials should be used in developing the various components of our system. It is present in one or more of the components in most all of the present LTCC systems. Its presence is understandable as it provides unique contributions to the properties of electro-ceramic devices like capacitors, thermistors and to glasses used in IC's, coating, displays and thick film hybrids. In addition, its combination with tin provides an excellent combination of low cost, low melting temperature and good ductility in solders.

Unfortunately, lead in even minute quantities can be shown to cause brain, nervous system, liver and kidney problems, especially in children. One of the primary concerns is that lead containing products disposed in landfills will be leached into the soil and eventually wind up in water supplies resulting in the poisoning of humans and the Ecosystem.

Electronic products are being upgraded and new ones are coming to market so fast that substantial quantities are indeed going to landfills. It is estimated that every citizen in the European Union generates 23 kg of electronic/electrical trash each year [3], which has the potential for a lot of hazardous material getting into waste streams. Each economic region has a different approach toward solving this problem.

One could argue that the threat posed depends on the types of leaded material and further that the commercial importance of the electro-ceramic and glass should be considered. There is certainly logic to that argument, but it is clear that there will probably be added costs and certainly headaches associated with the use of leaded materials in the future. We decided to avoid the problems by developing a completely lead-free system, i.e., the LTCC tape, the buried components, conductors and solders are all lead-free.

EXPERIMENTAL DESIGN

The designation and description of the non-leaded cofireable dielectrics used in this study are given in Table 1. The LTCC tapes are the glass/ceramic sheets, which form the matrix in which the components are buried and which forms the substrate on which the IC's are placed. These tapes are available with three values for dielectric constant (4, 7.5 & 13). Each has its advantages. We chose the K-13 tape for this study because using it as the matrix tape allows one to make the smallest parts which result in lowest overall cost.

The designations of the lead-free compatible capacitor tapes and pastes and the ferrite tapes which were developed for embedding in the K-13 tape are also listed on this table. The K values are approximate values for the tape (pastes) because they also depend on the firing conditions and electrodes used.

The compatible non-leaded conductors developed for use with the dielectrics listed in the previous table are shown in Table 2. Shown in this table are the buried silvers for conductive traces and vias, buried platinum / silver and

Table I
Non-Leaded, Cofireable Dielectrics

Designation	Description
41110	K-4 LTCC Tape
41020	K-7.5 LTCC Tape
41050	K-13 LTCC Tape
41230	K-18 Capacitor tape
41240	K-50 Capacitor Tape
41250	K-100 Capacitor Tape
41260	K-250 Capacitor Tape
40010	Ferrite Tape
4162	K- 50 Capacitor paste
4163	K- 85 Capacitor paste
4164	K-100 Capacitor paste

Table 2
Non-Leaded, Cofireable Conductor Pastes

Designation	Description
903-CT-1	High conductivity buried Ag
903-CT-1A	Buried Ag, best shrink match
953-1G	Buried Pt/Ag, low cost term.
963-G	Buried Pd/Ag
902-G	Ag via fill
962-G	Ag to Au transition via fill
903-CTA	Solderable top layer Ag
963-G	Solderable top layer Pd/Ag
953-AG	Low cost, leach resist Pt/Ag
803-MG	Top layer, wire bond gold
Solder	95.5 Sn, 3.8 Ag, 0.7 Cu
9904	Top layer photoimage Ag*
8804	Top layer photoimage Au*

*post fireable only

palladium / silver for component termination. There is also a lead free top layer, wire bondable gold and a Pd/Ag via fill that allows transitioning from the buried silver to the top layer gold without the deleterious (Kirkendall voiding) effects. Leach resistant, solderable metallizations and a lead free solder are listed. The table also lists photoimageable Au and Ag pastes that can be used to create fine lines.

The buried capacitor data shown later in the paper was obtained on tape laminates in which conductors and capacitor dielectrics in either tape or screen printed thick film formats had been placed. The tape stacks were laminated with a uniaxial press using pressures from 1000 to 3000 psi at temperatures of 50 to 70˚C. The laminated tape stacks were slowly heated to 450˚C and held at this temperature for one hour. They were then heated at various rates to the peak temperature (normally 875˚C) and held at that temperature for 15 to 60 minutes.

The dielectric loss versus frequency for the three different LTCC tape matrix materials is shown in Figure 1. The data is from measurements made on 903-CT-1 silver terminated ring resonator samples. The K-4 sample was fired at 850˚C with a 12 minute hold at peak while the K-7.5 and K-13 test samples were fired at 875˚C with a 15 min hold at peak. The loss curve for FR-4/Cu is shown for comparison since it is a competitive technology.

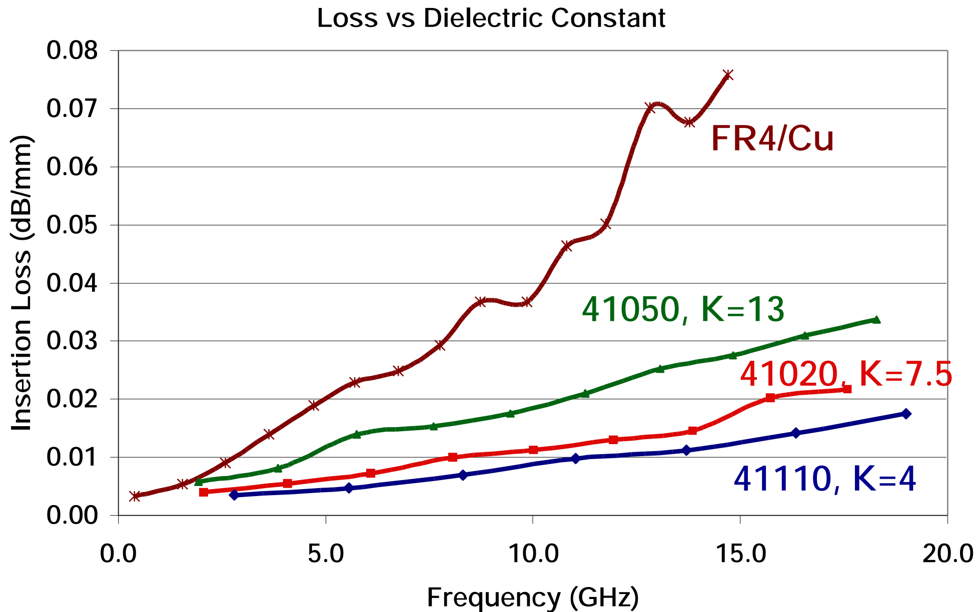

Figure 1

All testing of the K-13 tape indicates it is very robust. Its loss versus frequency curve doesn't change with time at peak firing temperature (at least over the 15 to 60 minute interval) (See Figure 2). Changes in the heating rates after burnout from 2˚C to 10˚C / min also has no affect on the loss curve (See Figure 3).

Measurements were made of the Dielectric Constant, Dissipation Factor and Insulation Resistance for the buried capacitor test samples at 1 KHz. In addition, the temperature coefficient of capacitance was measured at –55, -30, +85 & 125˚C on all these test samples. The ability of the ferrite tape to enhance the inductance of a buried spiral was also tested.

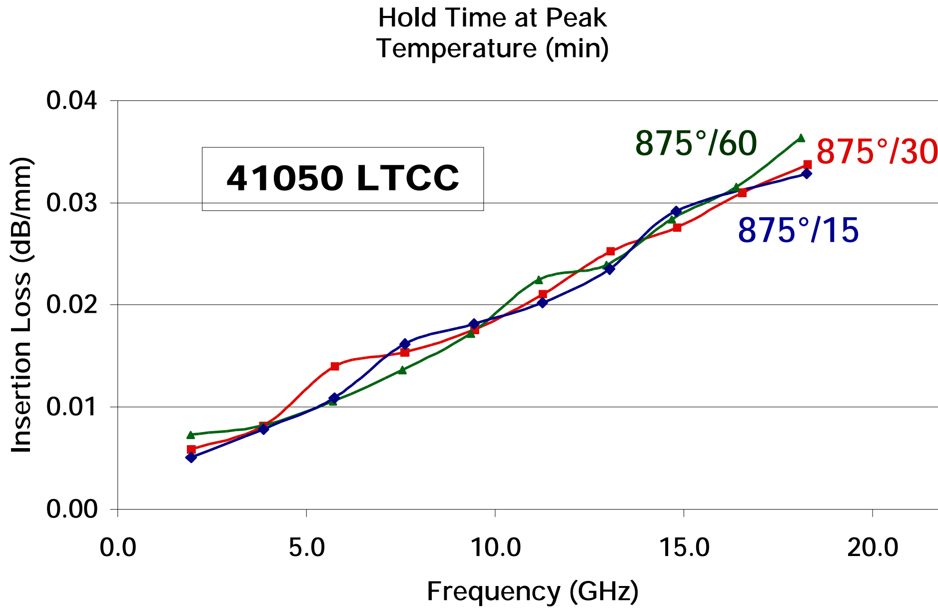

Figure 2

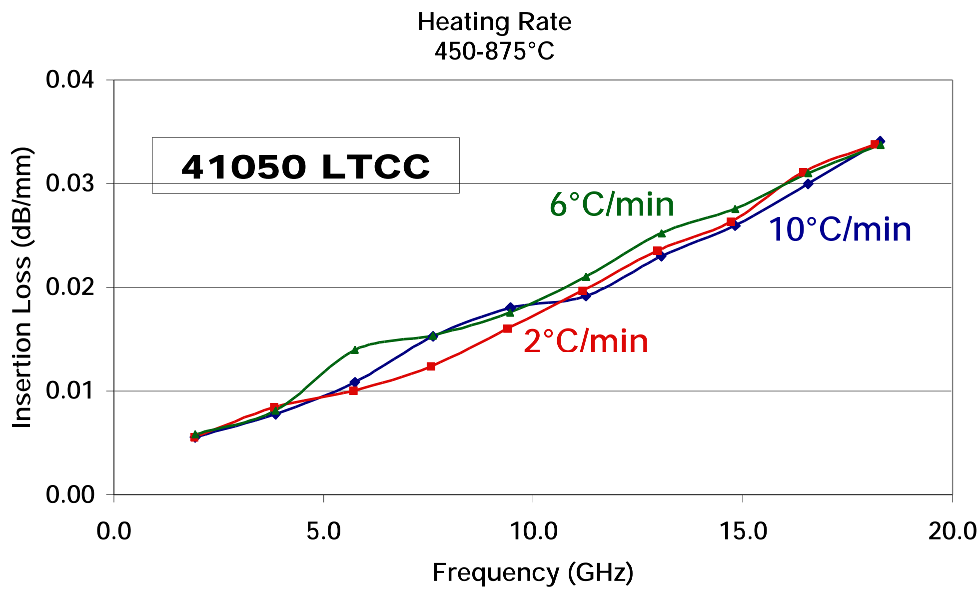

Figure 3

RESULTS

Table 3 shows the results of burying the four different capacitor tapes in the K-13 LTCC tape matrix. These capacitor tapes were formulated to give specific K values but as indicated in the table, the actual values and their environmental stability are influenced by firing conditions and electrode composition.

Table 3

Buried Capacitor Tape	Electrode Designation	Time at 875˚C (min)	Dielectric Constant K	Dissipation Factor DF	Insulation Resistance IR	Maximum |% C| -55 to 125˚C
41230	953-1G	60	18	0.1%	2 x 10^{11}	1.4
41240	953-1G	15	60	0.3%	4 x 10^{11}	5.8
41250	953-1G	15	103	0.6%	2 x 10^{11}	8.2
41250	903-CT-1	15	98	0.7%	9 x 10^{10}	5.5
41250	953-1G	60	108	0.6%	1 x 10^{11}	5.7
41250	963-G	15	110	0.6%	4 x 10^{11}	5.2
41250	963-G	60	107	0.5%	3 x 10^{11}	4.6
41260	953-1G	15	225	1.3%	7 x 10^{9}	15.2
41260	963-G	15	265	1.0%	2 x 10^{11}	13.2

Comparable data for non-leaded screen-printed capacitor dielectrics developed for use with the K-13 LTCC tape is presented in Table 4. We didn't investigate as many processing and electrode variations on screen printed buried capacitor pastes, so the data available is limited.

The fired laminates were cross-sectioned to get dielectric thickness for calculating K values and to examine the interface bonds between the LTCC matrix and the capacitors. Figure 4 shows backscattered micrographs of capacitor tape (41250) embedded in K-13 tape at magnifications of 100X and 500X. The conductive electrodes are 953-1G Pt/Ag. The samples were fired at 875˚C – 15 minutes

Figure 5 shows comparable backscattered micrographs of screen- printed 4164. It also used the 953-1G Pt/Ag and the 875˚C - 15 minute firing cycle.

Table 4

Buried Capacitor Paste	Electrode Designation	Time at 875˚C (min)	Dielectric Constant K	Dissipation Factor DF	Insulation Resistance IR	Maximum |% C| -55 to 125˚C
4162	953-1G	15	54	0.3%	8 x 10^{11}	0.8
4163	953-1G	15	84	0.8%	8 x 10^{10}	9.2
4164	953-1G	15	102	2.5%	1 x 10^{11}	17.5
4164	963-G	60	70	1.1%	1 x 10^{9}	13.7

Note that in the case of both the tape sheet capacitor and the screen-printed capacitor, the bonds between the tape, capacitor dielectric and conductor is very good. No delamination, bubbles or blisters were detected and no warpage occurred.

In an experiment to evaluate the effectiveness of the ferrite tape, the inductance of a screen-printed silver spiral pattern was measured on samples in three configurations. In the first the silver spiral was printed directly on the 41050 (K-13 LTCC) tape. This was buried between other sheets of 41050, laminated and fired. In the second set the silver spiral pattern was printed on a sheet of 40010 ferrite tape and covered with a second so the printed spiral inductor had one ferrite sheet on each side of it. This two layer structure was then embedded in sheets of 41050 (K-13) tape, laminated and fired. The third set was formed like the second except that two layers of 40010 ferrite tape were placed on either side of the printed spiral. Firing in all three cases was at a peak temperature of 875˚C with a hold time at this temperature of 60 minutes.

While printed conductive spirals can be used to create inductors in LTCC based modules, the results shown on Table 5 indicate that 40010 ferrite cover layers can be used to enhance inductance. They can be used to either reduce the area to achieve a given inductance value or to increase the inductance achievable on a given area. Optical micrographs of buried ferrite and capacitor tape

Table 5

Part Description	Inductance (µh)
Silver conductive spiral buried in LTCC	2.0
Silver conductive spiral with 2 layers ferrite tape *(one each side) buried in LTCC	3.5
Silver conductive spiral with 4 layers ferrite tape *(two each side) buried in LTCC	6.5

*each layer about 60µm thick

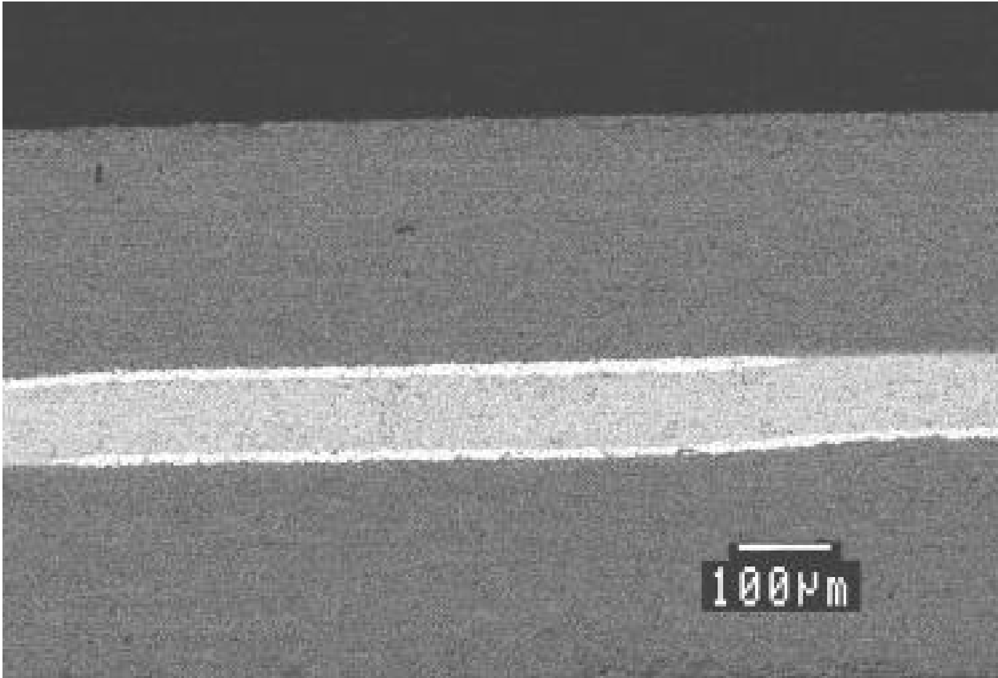

Figure 4a 100X 875°C -15 minutes

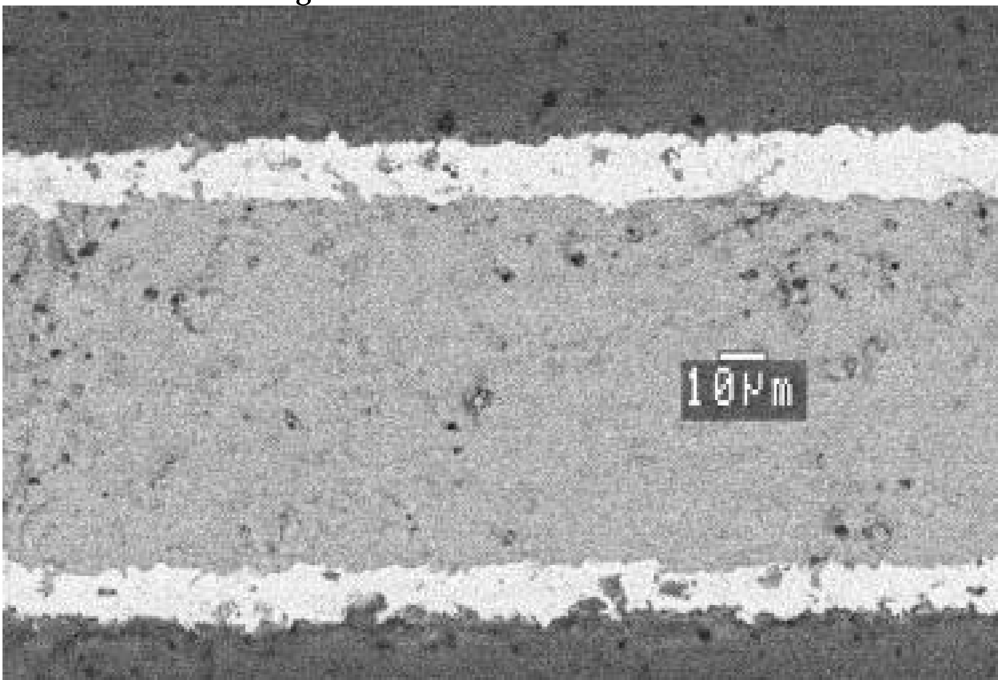

Figure 4B 500X 875°C - 15 minutes

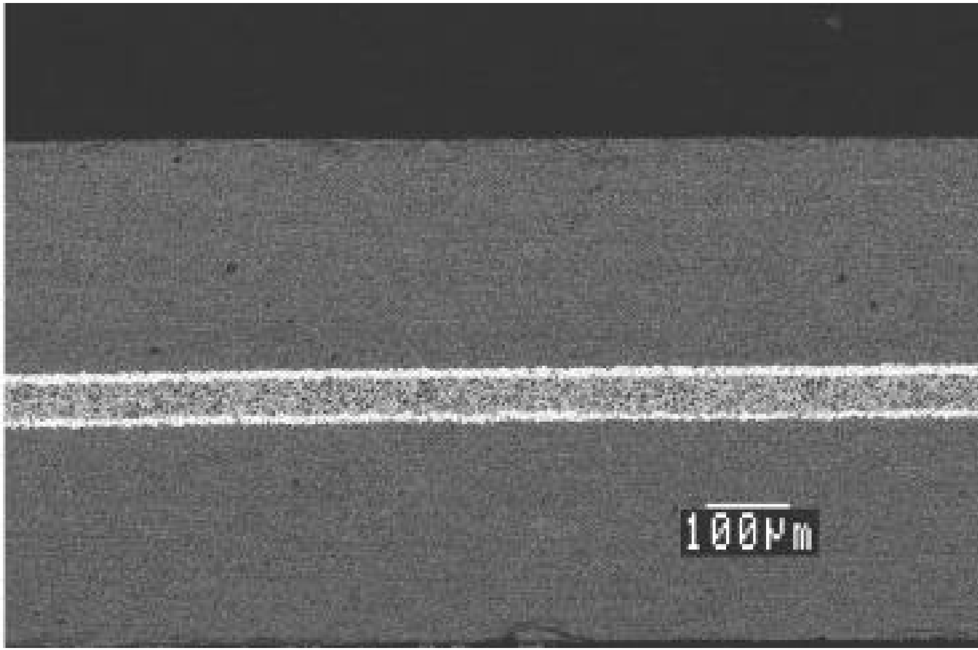

Figure 5A 100X 875°C 15 minutes

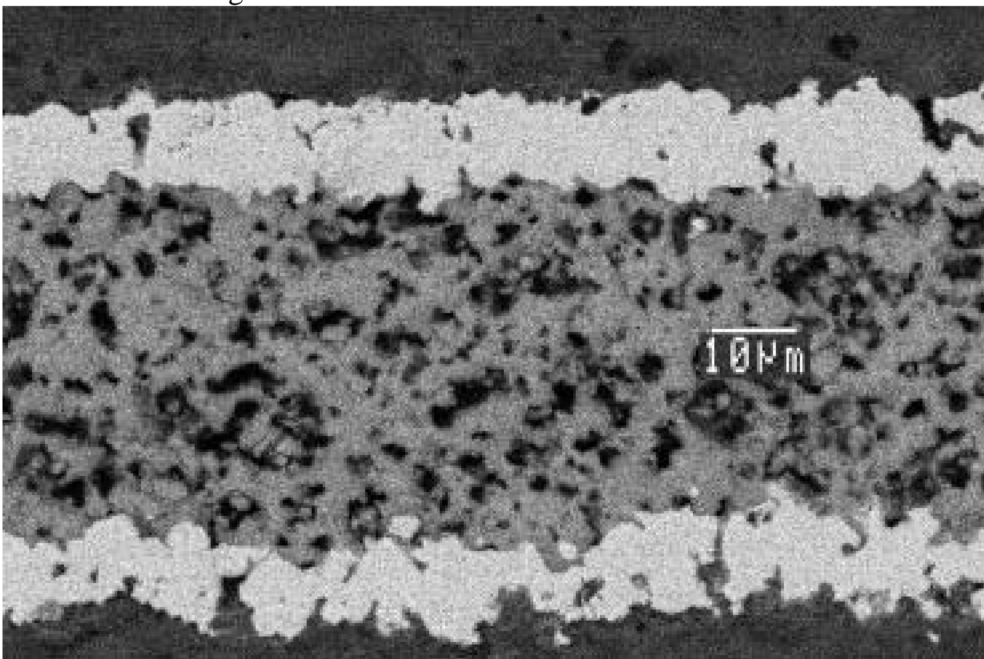

Figure 5B 500X 875°C 15 minutes

combinations are shown in Figure 6 . Again, good bonding is seen between the various components. It is more clearly shown in Figure 6B, which is at higher magnification than Figure 6A.

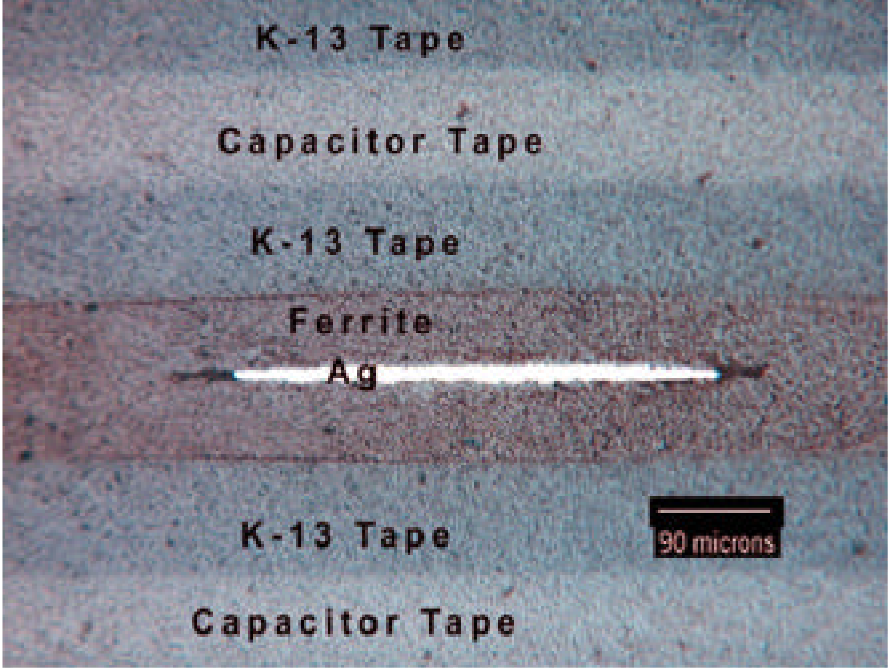

Figure 6A-100X

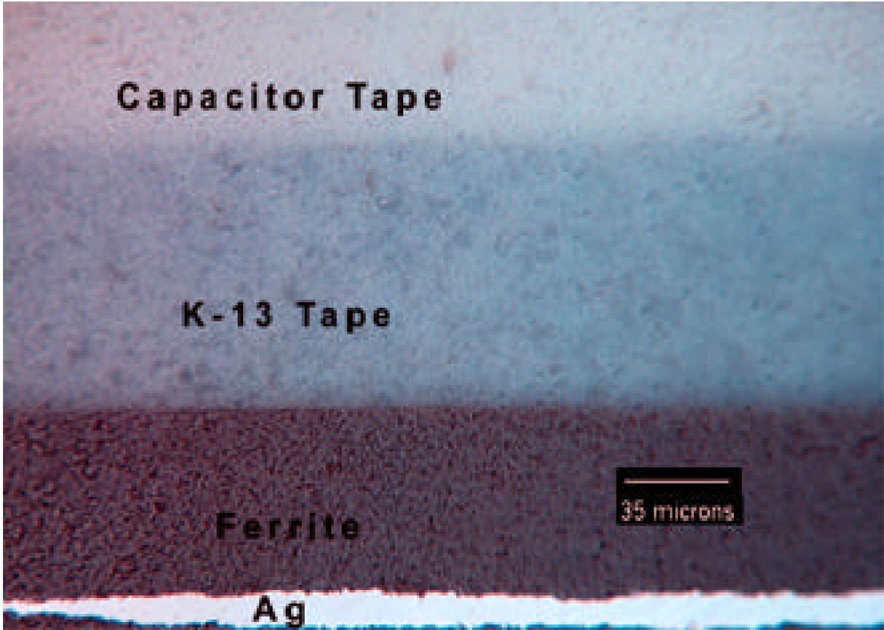

Figure 6B 500X

SUMMARY

A materials system was developed for telecommunication applications consisting of:

- LTCC tape with better loss than FR-4 and a K of 13 providing for size reduction (and potential cost reduction).
- Cofireable, low cost, low loss silver base conductors.
- Reduced cost processing through materials choice, parallel processing and peak firing temperatures below 900°C
- Capacitor dielectrics in tape and paste configurations with K values from 18 to 250 which can be embedded in K-13 LTCC tape.
- An inductance increasing (area reducing) ferrite tape that can be buried in the K-13 LTCC tape.
- A completely lead free system, including LTCC tape, low cost conductors, capacitor tapes and pastes, ferrite tape and solder with demonstrated compatibility.

REFERENCES

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2) D. L. Wilcox, R. F. Huang & R. Kommusch, "The Multilayer Ceramic Integrated Circuit (MCIC) Technology; An Enabler for the Integration of Wireless Radio Function", Advancing Microelectronics, vol. 25, no. 4, pps. 13-18.

3) K. Snowdon; "Towards a Green 2000" Proceedings of IMAPS Europe, June 1999, pp. 71-77.