Lead Free, Zero Shrink, Substrate Bonded LTCC System

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Abstract

Previous papers have reported on LTCC tapes for high frequency applications with K values from 4-16. High K (50 - 250) capacitor and high permeability (50 - 500) inductor materials have also been developed for buried component applications. Limitations in these materials have resulted in interest in transfer tapes (LTTT). These are laminated directly to prefired substrates. The resulting zero XY shrinkage provides precise dimensions while the intimate contact to ceramic substrates provides improved thermal conductivity and added strength. This paper presents a technology that takes advantage of the strengths of both. The new technology offers the ability to cofire multiple layers of lead free tape onto a ceramic substrate using low cost parallel processing .

Test parts were built with LTCC tapes using low cost silver. Metallized layers were stacked before lamination to the ceramic substrate. Capacitors and inductors were formed in these structures. Symmetrical placement of the components was not required because the restricted XY shrinkage limits warping. Photoimageing on intermediate prefired layers can be used to attain precision feature definition. This technology also provides the ability to fire specific components at optimized temperatures directly on the prefired substrate as well as for placing low loss transmission lines before the laminate is applied. Data will be presented for the capacitors and inductors buried in these structures on alumina substrates.

Introduction

There has been an unquenchable demand for substrates / packages that is pushing circuit designers to increase component density and reliability while decreasing size and cost. For those modules used in microwave applications low loss is added to the list. Even incremental success in meeting these needs often leads to significant performance improvement which in turn leads to users discarding the old equipment and buying the new upgraded versions. This creates sizeable quantities of electronic / electrical waste.

It has been estimated that the 15 countries of the European Union generate 8 million tons of such waste per year.[1] Unfortunately much of the discarded equipment contains lead in one form or another, and many fear that it will be leached into the soil and eventually wind up in water supplies. Legislation aimed at preventing this from happening is under consideration in many countries.

Lead provides many beneficial effects to the various circuit elements and there is no hard evidence that it would wind up in the water supply. However, we believe the approach with the fewest potential problems would be to use lead free materials systems. In particular, it appears that an LTCC approach involving burying the required resistors, capacitors, and inductors in a stack of low loss, lead free ceramic tape would result in the desired properties. Burying the passive components frees up surface space for active components, and increases the circuits per substrate. Low loss materials can prolong battery life in portable electronic device applications. If the dielectric in the matrix is low K, signal tract isolation and signal propagation rate are improved.

Modules (packages, etc.) are made from ceramic tape sheets and auxiliary materials, following the steps prescribed by either (1) Cofire Tape[2] or (2) Transfer Tape[3] processing methods. In the cofire tape process, cavities, vias and registration holes are punched in the tape sheets. This is followed by the deposition of conductor traces and other thick film circuitry. After inspection the tape sheets are stacked, registered, laminated and fired (peak temperature ~ 850˚C) forming a dense monolithic structure. In making transfer tape products, the tape sheets are laminated to a ceramic substrate. Conductors and other component pastes are printed and fired on each fired layer as needed. Each layer and each screen printed element is separately fired at about 850˚C. This layer by layer sequential build up process is repeated until the desired configuration is achieved.

The different tape processing schemes result in different part properties. Table 1 gives a comparison of the two. The "advantage" column lists areas in which the technology is deemed to have a definite advantage. The "Key Factor" is the process step or material difference responsible for the advantage. (So for example the zero (XY) shrinkage advantage that transfer tape has is the result of the presence of a substrate in this technology.)

An examination of the data suggests that the areas where transfer tape outperforms cofire tape processing are connected with the presence of the substrate. Transfer tape problems arise as a result of its multiple fires, which add labor cost and increase the chance of extended damaging interactions. Cofire tape processing's strength is related to its parallel processing and single fire feature.

Table 1
Tape Technology Comparison

Cofire Tape Processing		Transfer Tape Processing	
Advantage	**Key Factor**	**Advantage**	**Key Factor**
Low Cost	Parallel Processing	Zero (xy) Shrinkage	Substrate
Planarity	Single Fire	Strength	Substrate
Component Tolerance	Single Fire	Thermal Dissipation	Substrate
Low Interaction Potential	Single Fire	Low Loss/ High Frequency	Substrate
Small Size	No Substrate	Component Stability	Substrate
		Wide Range Component Value	Firing Temperature Range

This paper reviews an approach (Substrate Bonded Tape System) aimed at creating an improved packaging scheme by combining the strengths of transfer and cofire tape processing to form the required structures using lead-free materials.

Materials

Substrate

The substrate bonded tape system (SBTS) is an approach that involves parallel processed tape laminates that are subsequently bonded to a ceramic substrate. Firing is limited to a few fires usually done in a box furnace at a peak temperature around 850°C with a profile adjusted to the part size and number of tape layers.

The substrate provides strength, heat removal and limits XY shrinkage. Al_2O_3 is the usual choice because it is relatively low cost and provides a good combination of the above properties. Another attractive feature of Al_2O_3 substrates is their low loss characteristic which allows them to be used as the RF dielectric. Figure 1 shows the insertion loss of alumina compared to the most commonly used FR-4.

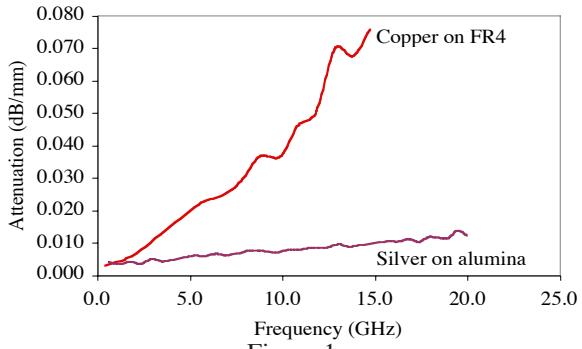

Figure 1
Attenuation of Alumina and FR-4

BeO substrates also have been successfully used in transfer tape processed parts where very high thermal conductivity was needed and should work for substrate bonded tape processed parts. This would be particularly useful in higher circuit density applications where large power dissipation is required. Other substrates like YSZ, glass bonded AIN and insulated metals are possible but have only had limited testing. Al_2O_3 was used in our study.

Compatible Tapes and Conductors

The properties of the lead-free tape dielectrics and conductors designed for use in the Interconnect & RF sections of the package are listed in Tables 2 and 3. Two mutually compatible tapes are described. The first is a low K, low loss dielectric which offers high signal propagation rates and provides excellent isolation[4]. It has been used on both Al_20_3 and BeO substrates. The second tape features excellent materials compatibility and enhanced solderability to the conductor deposited on it.

Table 2
Lead Free Tape Properties

Tape Designation	Dielectric Constant	Insertion Loss (dB/mm)	Used in Section
41110	4.2	0.004	RF
41020	7.5	0.006	Interconnect
Note: Alumina substrate, 850-875°C pesk fire			

These tapes have the same binder (composition and concentration) as is used to make the cofire tape products. This provides high green strength, gives fewer binder burnout problems, and results in less chance of via closure. It requires, however, that the tapes be laminated using cofire processing conditions, i.e., 3000 psi - 70°C (conditions that often cause breakage in alumina substrates). Transfer tape processing avoids substrate breakage by (1) increasing the binder content and by (2) making it "softer". This binder modification allows the lamination pressure to be reduced, which effectively solves the problems. The process under consideration "substrate bonded tape" avoids the problem by laminating the package without the substrate at a pressure of 3000 psi. The green tape laminate is then bonded to these substrates at a pressure of 1000 psi. This acceptably lower pressure provides the required bond through the use of a

Table 3
Lead Free Cofireable Conductors

Designation	Description
903-CT-1	High conductivity silver
903-CT-1A	Ag matched for shrinkage
953-CT-1G	Low cost Pt/Ag
963-G	Pd/Ag soldererable electrode
902-G	Ag via fill
962-G	Via fill for Ag/Au transition
903-CT-A	Solderable top layer silver
953-AG	Leach resuistant Pt/Ag
803-MG	wire bondable gold
8804	Photo-imagable gold
8881-B	Photo etchable gold
9904	Photo-imagable silver

screen printed thermoplastic "glue" layer.

The lead-free conductors are shown in Table 3. The majority of these are silver based and are all screen printable to meet the low cost need. 803-MG is a gold paste for wire bonding and 8804 & 9904 are photoimagable pastes used for producing fine lines on alumina. Fine lines may also be created using the photo-resist-etch techniques with 8881-B gold.

Insertion loss of the 41110 tape up to 16 GHz is shown in Figure 2. The ring resonator technique [4] was used to obtain the loss data. The insertion loss of 96% Al_2O_3 and 41110-70C tape (without the substrate) measured over the same frequency range is shown for comparison purposes. At the low frequencies (below ~ 8 GHz) the values are close with the cofired 41110 showing perhaps some advantage. Above 8 GHz the Al_2O_3 starts to show a definite advantage.

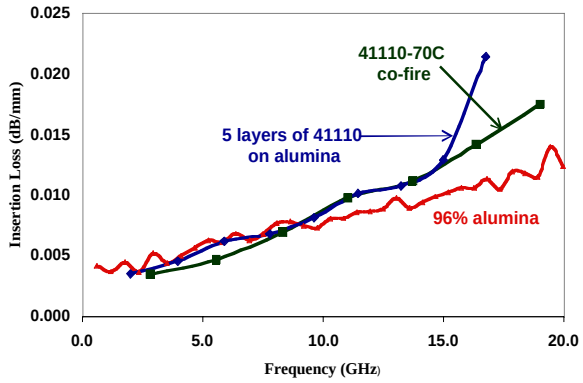

Figure 2

Fired Shrinkage:

A major advantage of using this new processing technology is the ability to restrict XY shrinkage. Since cofire tape typically shrinks ~15% in the XY direction print features generally need to be adjusted to accommodate the dimensional change associated with the firing process. Zero shrink alleviates this problem. For applications at conventional frequencies, the advantage of zero XY shrinkage is related to size effects. Multilayer interconnect depends on the ability to align vias. Although layer to layer shrinkage does not vary significantly, when overall shrinkage is large (15%) the tolerances are also large. The differences between x and y tolerances are also related to the overall shrinkage. Zero (<1%) overall shrinkage provides smaller tolerances and therefore allows much larger boards to be built. This significantly lowers manufacturing costs. Conventional transfer tape technology also offers zero shrink, but at the cost of multiple firing steps.

Another advantage of zero shrink is the precision and predictability of the printed features. This is particularly important when high frequency circuits are being designed as the impedance of transmission lines can be more accurately predicted. If cost is not critical, conventional transfer tape technology can be used. Dielectric thickness can be measured after each layer is fired, before the transmission lines are printed, so that precise values of line widths can be obtained (with photo-etching) to obtain the ultimate in precision for impedance values.

In the scheme described in this paper, transmission lines can alternatively be printed accurately directly on the alumina or they can be printed in the multilayer interconnect structure made up of low K, 41110 tape. The loss characteristics of this tape are actually better than that for alumina for lower frequencies (2-4 GHz, see Figure 2). In the latter scenario, only z shrinkage is required. This is generally has the same tolerance as Z axis thickness.

Low K tape can be parallel processed in thicknesses up to 8 layers with zero shrinkage. Shrinkage data is presented in Table 4. Stacks of up to eight layers of 41110 and 41020 tape were laminated together at 3000 psi. The eight layers can also be made up of four interconnect layers of 41110 and four LTCC layers of 41020 which can be used for buried components. The individual layers can be printed, vias filled, inspected, aligned and then laminated. This process is characteristic of the advantages presented by the LTCC cofire process. The package is then attached to an alumina substrate which has been preprinted with a specially formulated glue. When 41110 is used, the glue is a fugitive phase which cleanly burns away during the firing process. For 41020, the bond is formed using both glue and 903-CT-1 silver. 41020 will not bond to an alumina substrate or the 41110 tape if glue alone is used as a bonding agent. It is therefore necessary to use both glue and 903-CT-1 silver to attach it to 41110 (or the substrate). This additional layer of silver will act as a shield between the RF and low frequency sections of the circuit. The firing schedule is that recommended for the individual tape. A grid

pattern printed on the top layer is used to determine shrinkage.

The values for shrinkage listed in Table 4 were obtained by measuring the distance between grid lines near the outer edge of the part. X-Y direction shrinkage was measured as well. No difference was observed. The negative values reported imply growth of the laminate and are likely due to experimental error. The dimensions measure were compared to values obtained from the same grid printed and fired directly on an alumina substrate.

The combination of 41110 layers for interconnect and transmission lines can be combined with layers of 41020 tape which contain buried components. Shrinkage data for the composite structure is also presented in Table 4, below.

Buried Components

Capacitors

This technology is also important for it ability to accommodate buried components. Zero shrink allows placement of prefired chip components in the structure as well as buried cofired passives. Table 5 presents data obtained from buried capacitor tapes and pastes in the 41020 tape that is attached to an alumina substrate. 903-CT-1 silver bottom electrode was printed onto 41020 green tape. After drying, a layer of capacitor tape or printed capacitor paste was put into place. This was followed by a second print of silver electrode. A final layer of 41020 covered the capacitor.

This structure was then laminated onto an alumina substrate which was preprinted with glue and 903-CT-1 silver. The entire structure was fired at 875°C for 30 minutes at peak temperature. A set of capacitors buried in 41020 on an alumina substrate is shown in Figure 3. Capacitance measurements were used to determine K values after the structure was cross-sectioned to determine fired dielectric thickness. Figures 4 and 5 show cross sections of 41260-70C (K=250) tape and 4164 (K=250) paste buried in 41020 and attached to an alumina substrate. It is important to note from these

Table 5
Buried Capacitors

Designation	Description	K value obtained	DF %
41240-70C	K-50 tape	47.9	0.4
4162	K-50 paste	43.7	0.4
41250-70C	K-100 tape	95	0.7
4163	K-100 paste	128	3.0
41260-70C	K-250 tape	210	3.5
4164	K-250 paste	200	6.5

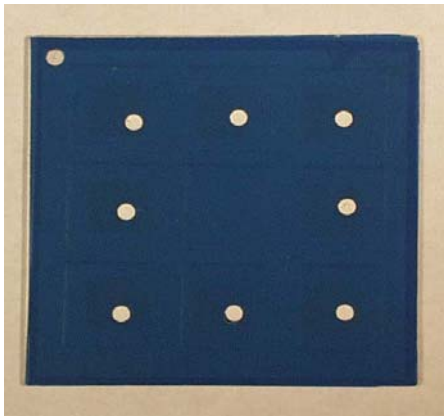

Figure 3
Capacitors Buried in 41020

Table 4
Shrinkage

Number of Laminates	Number of Layers 41110	Number of Layers 41020	Substrate Bonding	Mid-stack Bonding	Peak Firing Temp.	Shrinkage (xy) %
1	2	0	glue	none	850	-0.2
1	4	0	glue	none	850	-0.05
1	6	0	glue	none	850	0
1	8	0	glue	none	850	0.015
1	0	2	glue + 903-CT-1	none	850	-0.08
1	0	4	glue + 903-CT-1	none	850	-0.078
1	0	6	glue + 903-CT-1	none	850	-0.015
1	0	8	glue + 903-CT-1	none	850	0
2	4	4	glue	903-CT-1	850	0

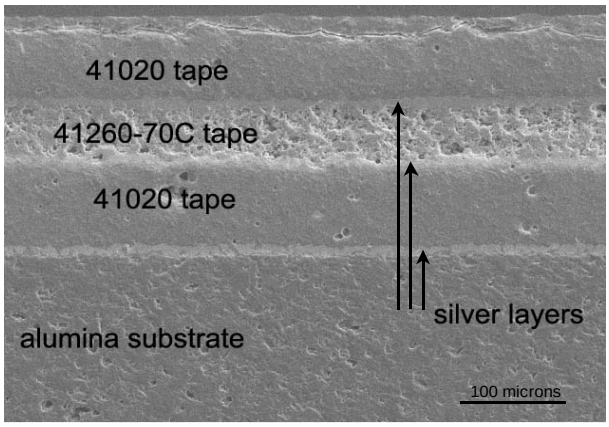

Figure 4
41260-70C (K=250) Tape Buried in 41020 Tape

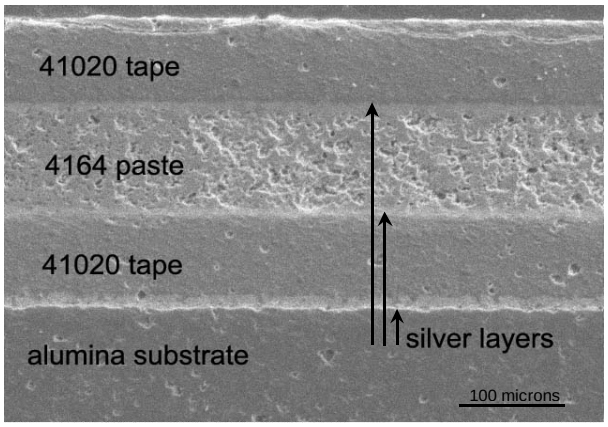

Figure 5
4164 Paste (K=250) Buried in 41020 Tape

photomicrographs that the interfaces between the various phases are void free and well defined.

Inductors

Inductors are another important passive component that can be effectively buried in LTCC packages. Spiral inductors are large consumers of space and this inductor configuration may not be chosen for this reason. Wirewound inductors are expensive because they require hand labor to manufacture, and discrete components are more costly than screen printed ones because they require handling and inventorying. The ability to obtain higher inductance values for printed spirals has been described in a previous publication [5]. Spirals printed between ferrite layers can have inductance values several time higher than the same spiral printed on any dielectric with unit permeability. The ferrite tape used in the previous paper has a nominal permeability of 200. These spirals were buried in 41050-70C LTCC tape as well as tapes from other vendors. The spirals in this paper were printed on dried ferrite paste and covered with screen printed ferrite paste. The resulting inductor was covered with (buried in) 41020 tape. This presents an example of the flexibility of this new process technology. The firing temperature of the ferrite paste can be optimized for higher permeability before the covering tape package is applied. Previously published results [5] indicate that higher firing temperature for ferrite tapes results in higher permeability.

Ferrite paste was printed onto alumina substrates coated with 903-CT-1 and glue. Small silver spirals (7mm diameter, 5 turns) were printed on the dried ferrite. These were then covered with subsequent prints of ferrite paste. After drying, layers of 41020 tape were applied and the entire structure laminated. Figure 6 is a schematic. This configuration of inductor has a value calculated to be 0.1μH [6]. The value measured at 500 KHz was consistent with this calculation. The measured values for inductance of the spiral buried in ferrite paste was 0.2-0.3 μH. These parts were fired at 900-920 °C. The increase in inductance is dependant on both thickness of the ferrite and the firing temperature. The 2-3 times

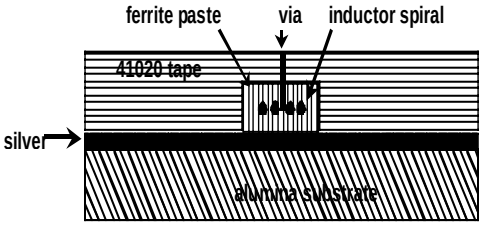

Figure 6
Schematic of Buried Inductor

increase in inductance would allow a reduction in area required for any given inductance. Figure 7 shows the interface between the various components of this structure. No delamination or voids are evident at the interface.

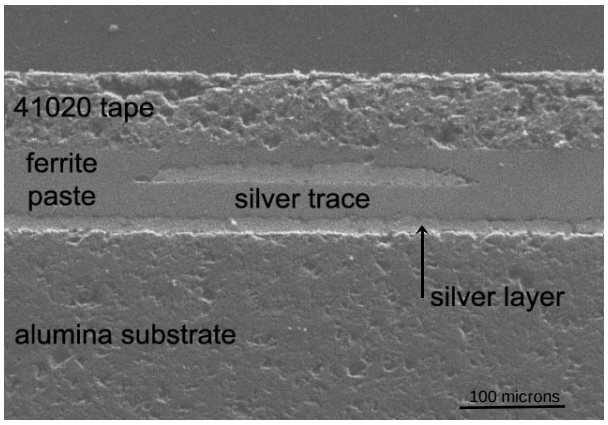

Figure 7
Spiral Buried in Fired Ferrite Paste

Finished Components

This technology also make possible the ability to bury finished surface mount components. Although these are more expensive than screen printed components, they can be chosen when very precise values are required. The property values of these finished components should not be affected by the firing schedule required to fabricate these packages. This allows the use of chip resistors with

tolerances much smaller than anything obtainable from buried components. It also eliminates the need for trimming.

Summary

A processing technology has been developed that combines the best features of two existing LTCC technologies. Transfer tape technology provides the precision associated with zero xy shrinkage, high thermal conductivity, strength from the substrate and flexibility for features and passive components. Cofire technology provides the cost savings which result from parallel processing and the ability to inspect features before they are committed to the package. The flexibility resulting from combining these technologies is its strongest point. The alumina substrate can be prefired with transmission lines and/or high value capacitors and inductors before the interconnect package consisting of low K dielectric is attached. Resistors can be buried or printed on the back side of the alumina. Complex modules can be build up as needed.

References

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