SUCCESS STORY

CADENCE AND NVIDIA

Constraint-Driven High-Density Interconnect (HDI) PCB Design Flow Helps NVIDIA Speed Products to Market

"Having tools with the flexibility to drive the high-speed constraints in our designs is paramount to meeting our time to market. Cadence tools give us that flexibility, especially with the new HDI design capability. We are shaving up to 25% off our PCB layout design cycle time."

Greg Bodi, *Senior Manager, System Design, NVIDIA*

CORPORATE PROFILE

- NVIDIA develops visual computing technologies and high-performance processors that enable cutting-edge graphics on workstations, personal computers, game consoles, and mobile devices

BUSINESS CHALLENGES

- Meeting tight six-month time-to market windows
- Increasing design density and complexity requires more in-house design tools to optimize fanout and high-density interconnect

DESIGN CHALLENGES

- Having HDI design capabilities in a constraint-driven PCB design flow
- Driving micro vias quickly and accurately
- Reducing the number of layers on customers' boards
- Shortening the PCB layout design cycle

CADENCE SOLUTIONS

- High-speed constraint-driven HDI flow to shorten the design cycle while adhering to high-speed rules
- Mitigate risk, boost performance, and increase efficiency with a set of proven, unified PCB design, layout, editing, and routing technologies
- Collaboration with NVIDIA engineers to streamline time to productivity with the enhanced flow

CADENCE PRODUCTS

- Cadence® Allegro® PCB Design

STAYING COMPETITIVE IN THE CONSUMER ELECTRONICS MARKET

NVIDIA leads the industry in developing visual computing technologies and is the inventor of the GPU, a high-performance processor that generates breathtaking, interactive graphics on personal computers, game consoles, and mobile devices such as smartphones. To keep up with consumer demand for such high-performance gadgets, NVIDIA must meet stringent time-to-market windows. Their average design cycle is less than six months, from silicon tapeout to printed circuit boards (PCBs) ready for the marketplace.

NVIDIA design teams rely on Cadence tools to create their IC package and board designs. They developed several in-house tools for fanout and routing to augment the Cadence Allegro constraint-driven PCB design flow, which they have been using for quite some time now. But the pressures of product miniaturization and

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high-density interconnect (HDI), combined with an increasing number of constraints on nets, was creating new challenges. NVIDIA required a complete HDI solution that includes high-speed rules to shorten their design cycles and meet their market window.

Greg Bodi, NVIDIA Senior Manager, System Design, explains, "NVIDIA designs require a robust, constraint-driven PCB design flow. And having HDI capabilities driven by that flow is critical for us to meet our time-to-market objectives."

The question was whether to invest time and resources developing their own tools to enable HDI, or to incorporate the latest Allegro PCB Design technologies, which provide the unique combination of a proven constraint-driven flow and comprehensive automation-assisted HDI manufacturing rules. Having worked with Cadence tools and experts before, NVIDIA felt assured that adopting the new Allegro constraint-driven HDI flow would be easy and that collaboration with Cadence would optimize their time to productivity.

SMALLER GADGETS REQUIRE HDI CAPABILITIES

Designers of high-end consumer electronics face the challenge of miniaturization and its resulting complexity. Often the solution is to use a "build-up" process to fabricate PCBs in order to handle the high-density interconnect. Not only are the device and overall design pin counts increasing, but the pitches (distances between pins) are rapidly shrinking. Designing circuit boards to connect with all the pins on advanced-node, ball grid array (BGA)-packaged ICs is an evermore time-consuming task. And while miniaturization is not necessarily the primary objective for customers in other market segments, more and more companies are now relying on build-up technology to handle high pin-count BGAs. The number of nets on a PCB that have high-speed constraints has also been growing. And as the industry migrates to standards-based interfaces like DDR2/DDR3 and PCI Express, the number of constraints on nets is also increasing. Combining DDR2/DDR3, PCI Express, and SATA II signals with the HDI build-up process requires a complete constraint-driven HDI design flow.

NVIDIA designs with high-speed constraints but also uses build-up technology to handle BGA fanouts. So they needed a design environment that could handle both sets of design requirements. Cadence has offered constraint-driven PCB design flows for many years, but with the significant improvements in the 16.2 release of Allegro PCB and IC packaging technology, Cadence offered NVIDIA both of these capabilities in an integrated design environment.

The Allegro constraint-driven HDI design flow provides a proven, robust constraint-driven PCB design flow with a comprehensive set of design rules for all different styles of HDI designs, from a hybrid build-up/core combination to a complete build-up process. "Having tools with the flexibility to drive the high-speed constraints in our designs is paramount to meeting our time to market. Cadence tools give us that flexibility, especially with the new HDI functionality," says Bodi. Allegro PCB Editor now includes automation for adding and managing micro vias to shorten the time to create designs that are correct-by-construction. From front-end design creation to signal integrity to back-end layout, the 16.2 release boosts productivity and predictability while streamlining the product development cycle.

SHORTENING NVIDIA'S PCB DESIGN CYCLE BY 25%

HDI designs are extremely complicated to develop, fabricate, and assemble because of the small pitches on the components. New technology introduced in Allegro PCB Design for HDI designs includes new objects, an extensive set of new HDI rules for micro vias and same-net elements, an enhanced via-transition use model, via stacking rules (staggered and inset vias), and powerful automation-assisted interconnect and via pattern insertion. Manufacturing IP-driven wirebonding and co-planar waveguide modeling further boost productivity and reduce manufacturing-driven engineering change orders (ECOs). Design partitioning has been enhanced with new capabilities for partitioning the design horizontally and adding soft boundaries, allowing users to work in parallel more efficiently, which further shortens the design cycle.

For NVIDIA, the key advantage of the new tool's added HDI functionality is the ability to handle micro vias—blind and buried vias, how the vias are built, how they affect the lamination cycle. "Cadence has really done a lot of good engineering work to come up with a methodology for driving down the micro vias through the layers to get the correct via structure, spacing for the vias themselves, through-hole vias, and to other metal shapes and traces in a design," Bodi explains. "With the significant improvements in the Allegro 16.2 release, we are shaving up to 25% off our PCB layout design cycle time for complex high-speed designs that use HDI technology."

NVIDIA's designs require certain spacing from one micro via to an adjacent micro via or blind/buried via. In the past there was nothing to control that, but with the new Cadence HDI functionality, it can be done on-the-fly. The Cadence tool automatically drops the vias in the correct location, which greatly increases efficiency

and eliminates previous user-developed and user-maintained workarounds. Now that the NVIDIA design team has an integrated HDI design and validation mechanism, they don't have to spend time building their own internal automation tools or perform any post-processing. Using Cadence technology, NVIDIA doesn't need to build their own workaround to develop ways to keep the correct spacing, which applies to both IC package substrate design and PCB HDI design. This also enhances their overall ability to design products.

Another key enhancement in the 16.2 release is more flexibility to handle HDI design specifically when it comes to constraints for HDI—"One of the best improvements in the tools set," according to Bodi. With the proven Cadence constraint-driven flow, electrical engineers can specify physical and spacing constraints for critical high-speed nets and embed those in the design to improve the chances of first-time success. These constraints are required for signals such as those found in memory interfaces (DDR2/DDR3), where the engineer needs to specify line widths and spacing to manage impedance and shield critical signals from crosstalk. "We need to know what our signal integrity and power delivery is going to be like. Some of our products have designs with currents up to 200 amps. R&D engineers at Cadence did a tremendous amount of work to make the new tools fit the high-speed design flow with good signal integrity," says Bodi.

NVIDIA also uses the built-in Allegro Field Solver to push the correct impedances into their designs and to eliminate unnecessary iterations between hardware designers and PCB layout designers. After pushing the correct impedances, they enter numbers quickly into the Allegro Constraint Manager flow and start the design. "NVIDIA uses SKILL programming/scripting language to increase our efficiency with all the different features in the Cadence tool sets. But we go a step further," Bodi explains. "We enhance our SKILL to drive this, so the layout person can actually begin design immediately. They can place their components, start routing, and have the correct line spacing and trace."

CADENCE SUPPORT SERVICES OPTIMIZE TIME TO PRODUCTIVITY

Throughout the development process, Cadence technology experts worked with the NVIDIA design team to address their concerns or questions about any new design processes or tools. This collaboration allowed NVIDIA to quickly incorporate the enhanced flow and tool capabilities, helping them to further streamline the design cycle and meet their market window. "We have an extremely strong relationship with Cadence. Probably one of the best engineering supports systems I've seen. They do a good job of listening to our concerns, addressing our bugs and our enhancements requests—with 16.2, some of the enhancements we requested made it into the release," Bodi explains. "They are definitely diligent about making sure NVIDIA is a successful company."

NVIDIA is pleased that Cadence has improved its Allegro technology to enable shorter, more predictable design cycles for their PCB designs. And now with a constraint-driven HDI design flow, NVIDIA can develop smaller boards with fewer layers and higher performance to stay on top of the competitive and price-sensitive consumer electronics market.

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