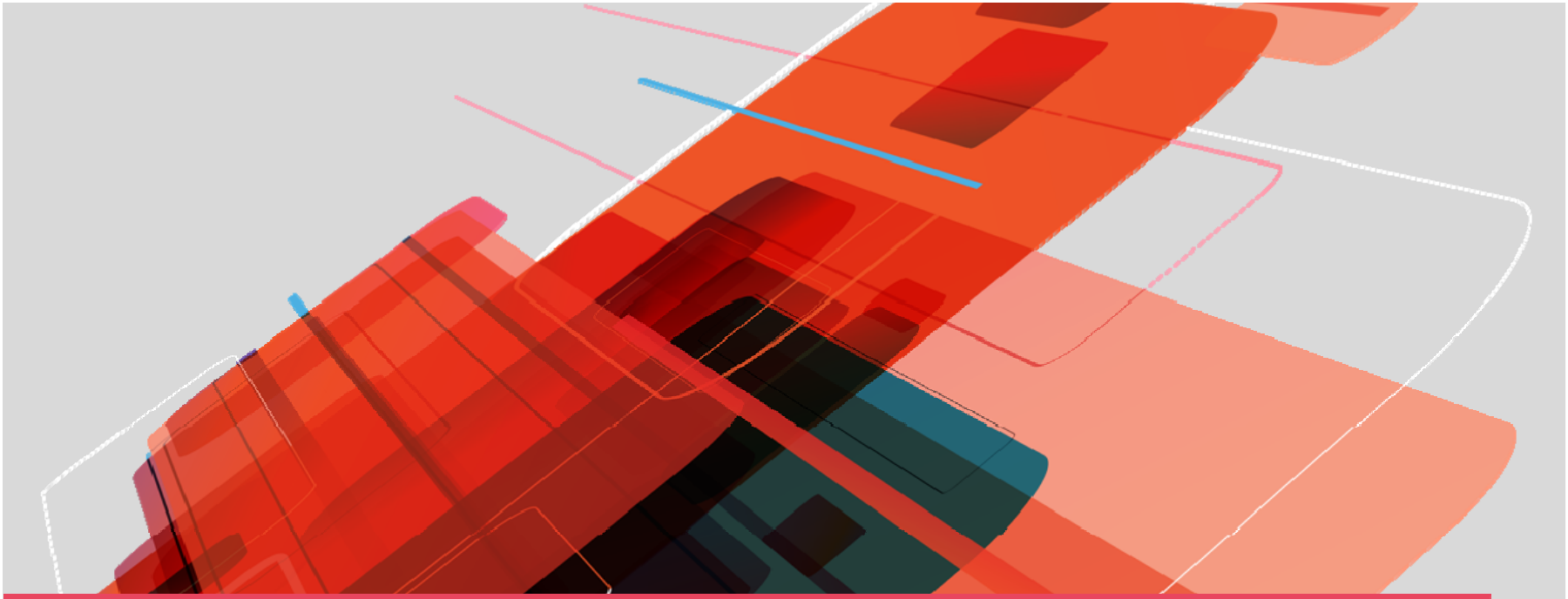


OrCAD Constraint Driven Design Flow

Presented By: Janine Flagg
Sr. Field Applications Engineer
eMail: JanineF@ema-eda.com

Customer promise…

Our focus today, as it was in 1989, is to meet our customers' requirements with quality products, leading technology, and exceptional technical support.

OrCAD™ CADENCE PCB SOLUTIONS

EMA Design Automation®

EMA Design Automation
Corporate Overview

- **From point solutions to fully integrated EDA systems including Cadence Design Solutions:**
  - Cadence® Allegro® PCB Design Tools
  - Cadence® OrCAD® PCB Design Tools

- **Complimentary technologies:**
  - CircuitSpace - Component Placement and Design Reuse
  - TimingDesigner® - Timing analysis for digital design
  - CIP - Component Information Portal
  - Enterprise Link - CIS to PLM/MRP Synchronization

Webinar Topics

- **Assigning Component and Net Properties in OrCAD Capture**
- **Auto Assigning Differential Pairs in OrCAD Capture**
- **Passing Properties from OrCAD Capture to PCB Editor**
- **Placement of Components with ROOM Properties**
- **Using Technology Files into PCB Editor**
- **Anatomy of a Differential Pair**
- **Routing Differential Pairs**
- **Routing Nets with Total Etch Length Constraints**
- **Constraint Resolution**
- **Design Reuse**
- **Demos**

Assigning Component Properties in OrCAD Capture

- Component Properties
  - **ROOM** – Floor planning
  - **HARD_LOCATION** – Locks reference designator from being modified by Auto Rename and back-annotation process

PCB Footprint	SM_1206	SM_1206	SM_1206	SM_1206
PIN_ESCAPE				
PINUSE				
PLACE_TAG				
POWER_GROUP				
Power Pins Visible	☐	☐	☐	☐
Primitive	DEFAULT	*DEFAULT*	DEFAULT	*DEFAULT*
RATED_MAX_TEMP				
REFERENCE	C?	C19	C?	C15
REUSE_INSTANCE				
ROOM	MEM	MEM	MEM	MEM
SIGNAL_MODEL		DEFAULT_CAPACITOR_10		DEFAULT_CAPACITOR_10
Source Library	C:\CADENCE\PSD_9.2. ...	C:\CADENCE\PSD_9.2. ...	C:\CADENCE\PSD_9.2. ...	C:\CADENCE\PSD_9.2. ...
SWAP_GROUP				
T_TEMPERATURE				

Assigning Net Properties in OrCAD Capture

- Net Properties
  - **NET_PHYSICAL_TYPE** – Creates a Net Class in Physical Domain
  - **NET_SPACING_TYPE** – Creates a Net Class in Spacing Domain
  - **MIN_LINE_WIDTH** – Physical Constraint override

MAX_XTALK				
MIN_BOND_LENGTH				
MIN_HOLD				
MIN_LINE_WIDTH	15 mil	15 MIL		
MIN_NECK_WIDTH	8 mil	8 mil		
MIN_NOISE_MARGIN				
MIN_SETUP				
Name	*GND*	*GND_EARTH*	*HS*	*MCLK*
NET_PHYSICAL_TYPE				CLOCK_PH
NET_SCHEDULE				
NET_SPACING_TYPE	DC_NETS	DC_NETS		CLOCK
NO_GLOSS				
NO_PIN_ESCAPE				

Assigning Net Properties in OrCAD Capture

- Net Properties
  - **ROUTE_PRIORITY** – Instruction for the Autorouter to prioritize net
  - **TOTAL_ETCH_LENGTH** – Controls the maximum length of the overall net

PULSE_PARAM				
RATSNEST_SCHEDULE				
RELATIVE_PROPAGATION_DELAY				
ROUTE_PRIORITY	1	1	1	1
SHIELD_NET				
SHIELD_TYPE				
STUB_LENGTH				
SUBNET_NAME				
TIMING_DELAY_OVERRIDE				
TOTAL_ETCH_LENGTH	2300MIL:2400MIL	2300MIL:2400MIL	2300MIL:2400MIL	2300MIL:2400MIL
TS_ALLOWED				
VOLTAGE				

Differential Pairs:
Auto Assign in OrCAD Capture

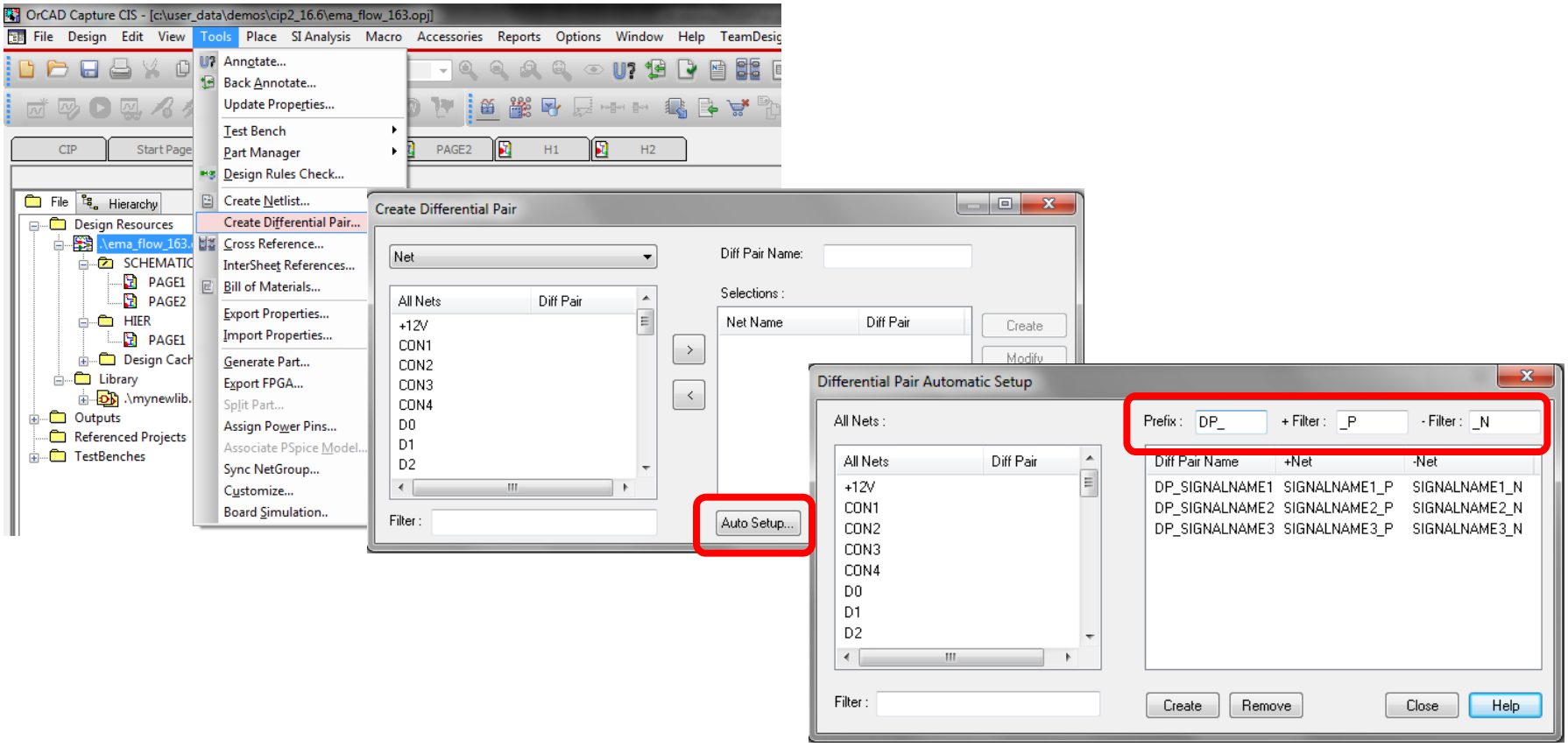
- Signal Naming Convention for Auto Setup of Differential Pairs

  Examples:

SignalName_P	SignalNameP
SignalName_N	SignalNameN
SignalName_H	SignalNameH
SignalName_L	SignalNameL
SignalName_+	SignalName+
SignalName_-	SignalName-

Differential Pairs
Auto Setup in OrCAD Capture

Tools > Create Differential Pair > Auto Setup



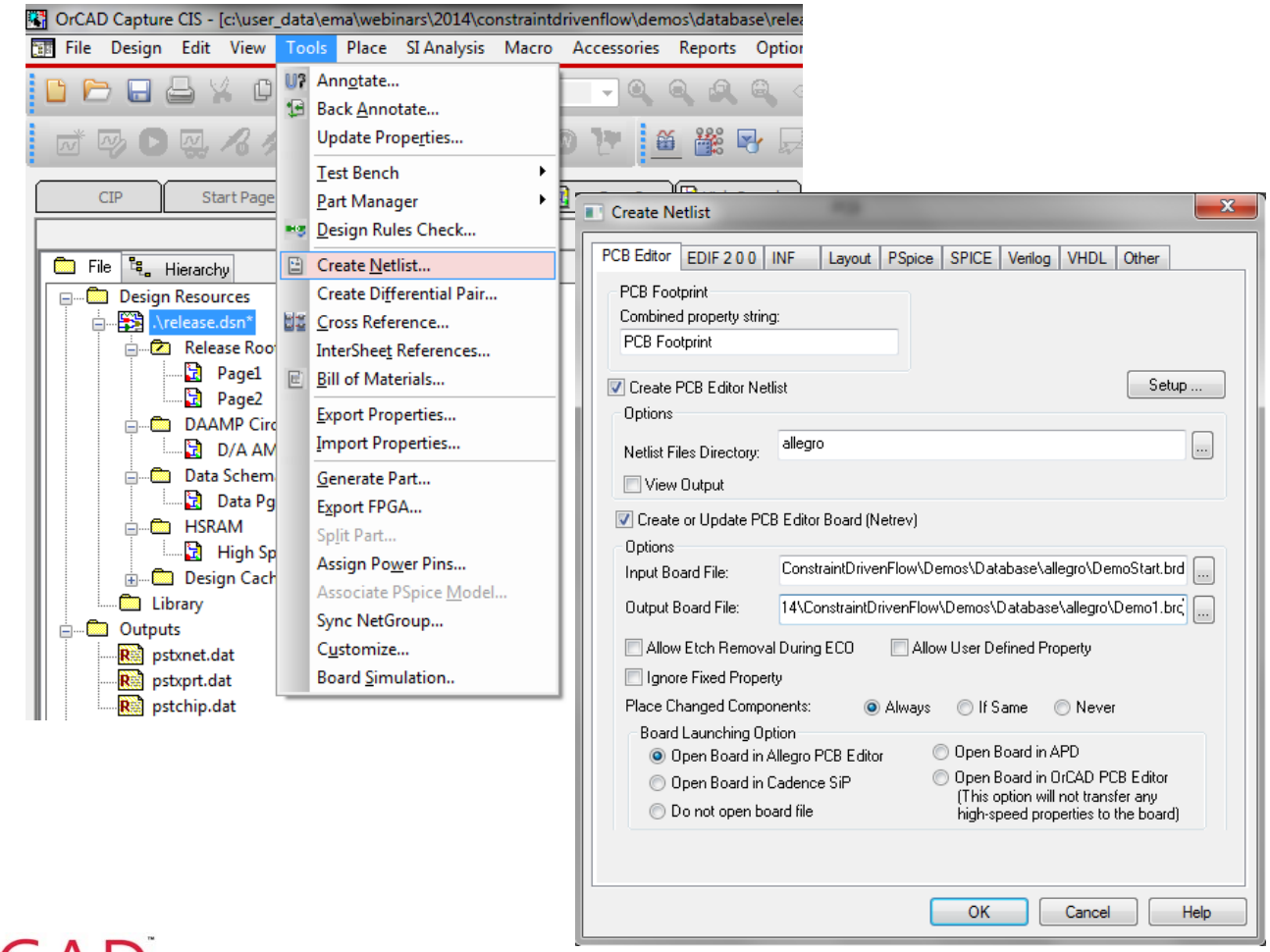
Other Differential Pair Properties

- Set constraint overrides for Differential Pairs
  - **DIFF_MIN_SPACE** - Minimum Spacing
  - **DIFF_UNCOUPLED_LENGTH -** Maximum Uncoupled Length

	A	B	C	D	E	F
	SIGNALNAME1_N	SIGNALNAME1_P	SIGNALNAME2_N	SIGNALNAME2_P	SIGNALNAME3_N	SIGNALNAME3_P
BUS_NAME						
CLK_2OUT_MAX						
CLK_2OUT_MIN						
CLK_SKEW_MAX						
CLK_SKEW_MIN						
CLOCK_NET						
DIFFERENTIAL_PAIR	DP_SIGNALNAME1	DP_SIGNALNAME1	DP_SIGNALNAME2	DP_SIGNALNAME2	DP_SIGNALNAME3	DP_SIGNALNAME3
DIFF_MIN_SPACE	4 mil	4 mil	4 mil	4 mil	4 mil	4 mil
DIFF_UNCOUPLED_LENGTH	200 mil	200 mil	200 mil	200 mil	200 mil	200 mil
ECL						
ECL_TEMP						
ELECTRICAL_CONSTRAINT_SET						
EMC_CRITICAL_NET						

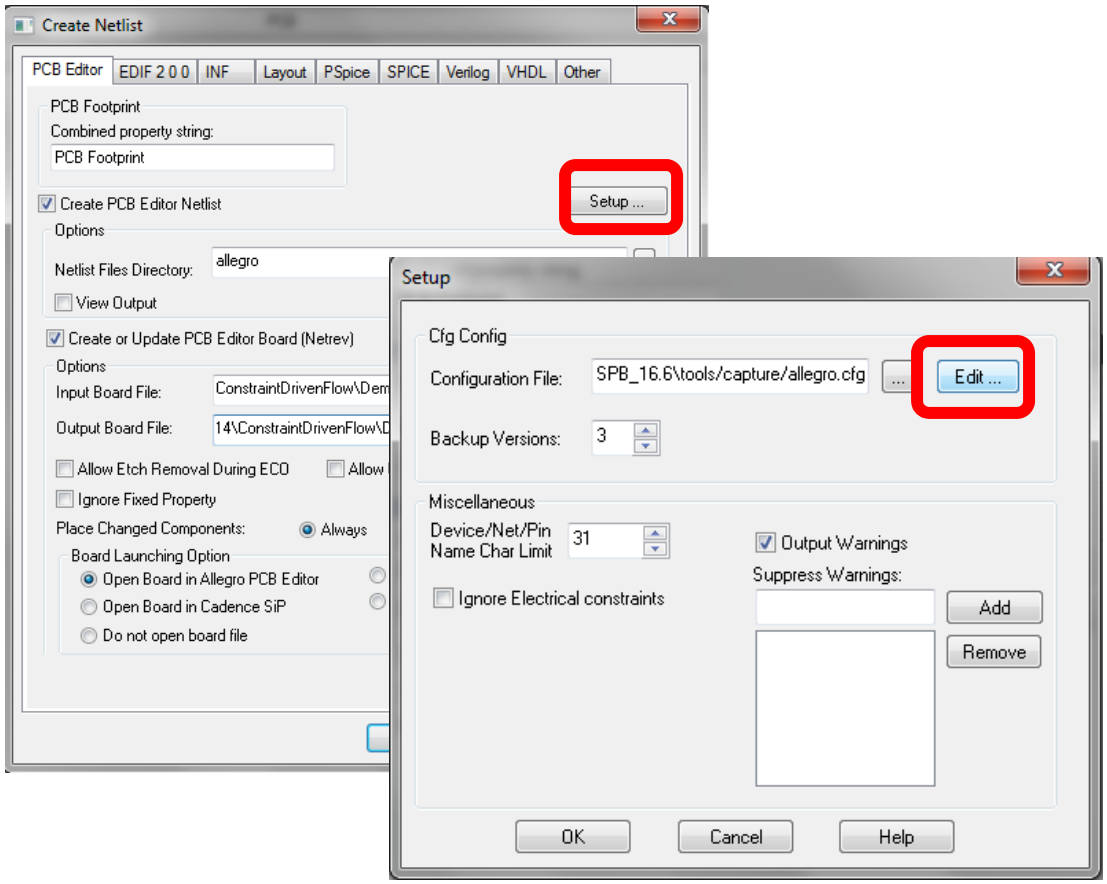
Passing Properties from OrCAD Capture to PCB Editor

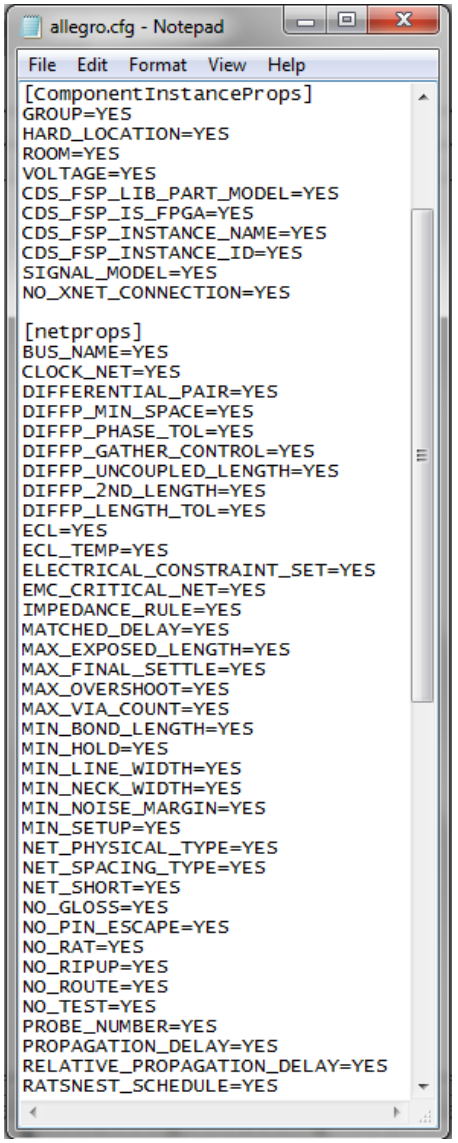
Tools > Create Netlist



Passing Properties from OrCAD Capture to PCB Editor

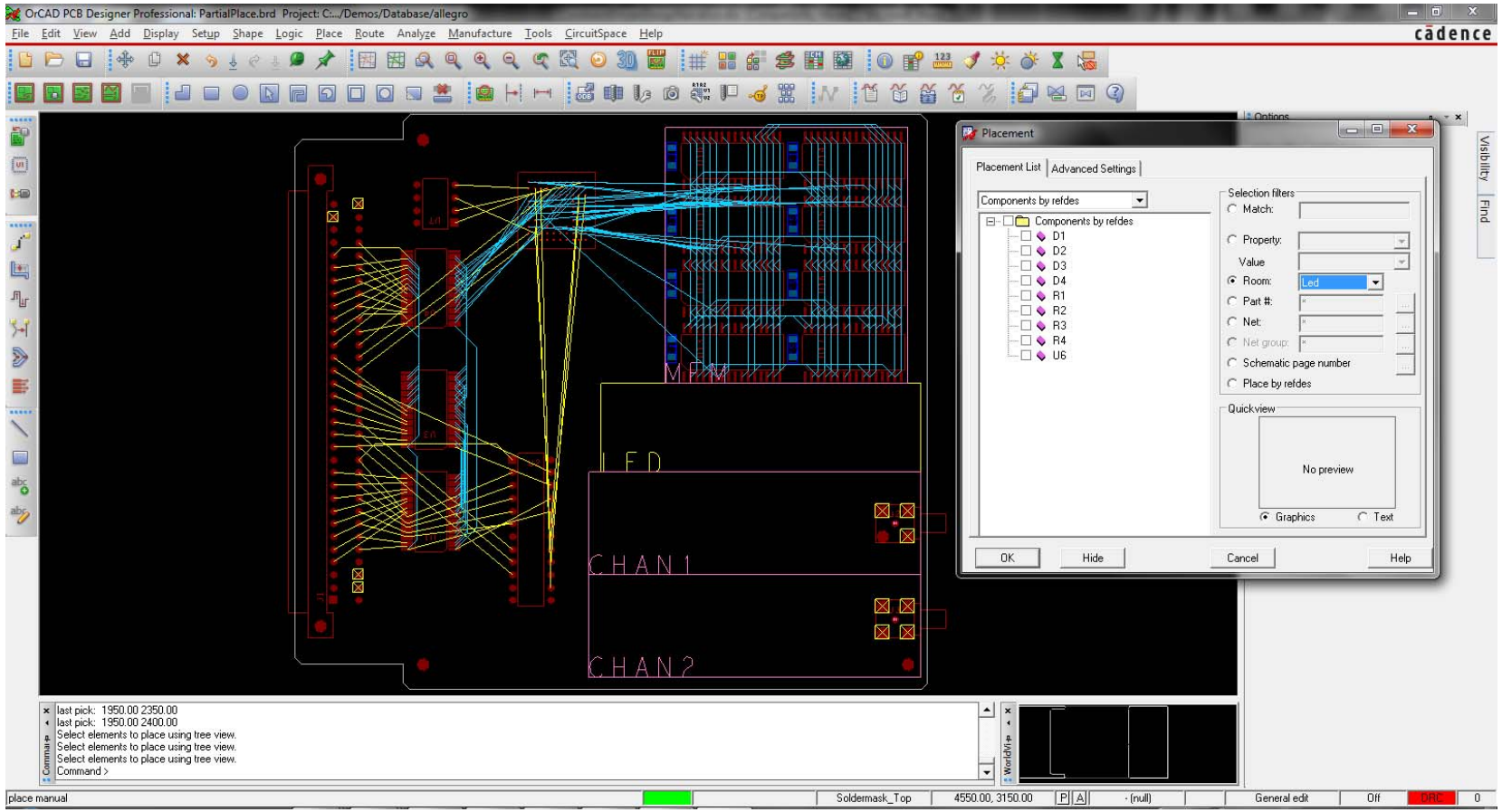
- Edit *allegro.cfg* file





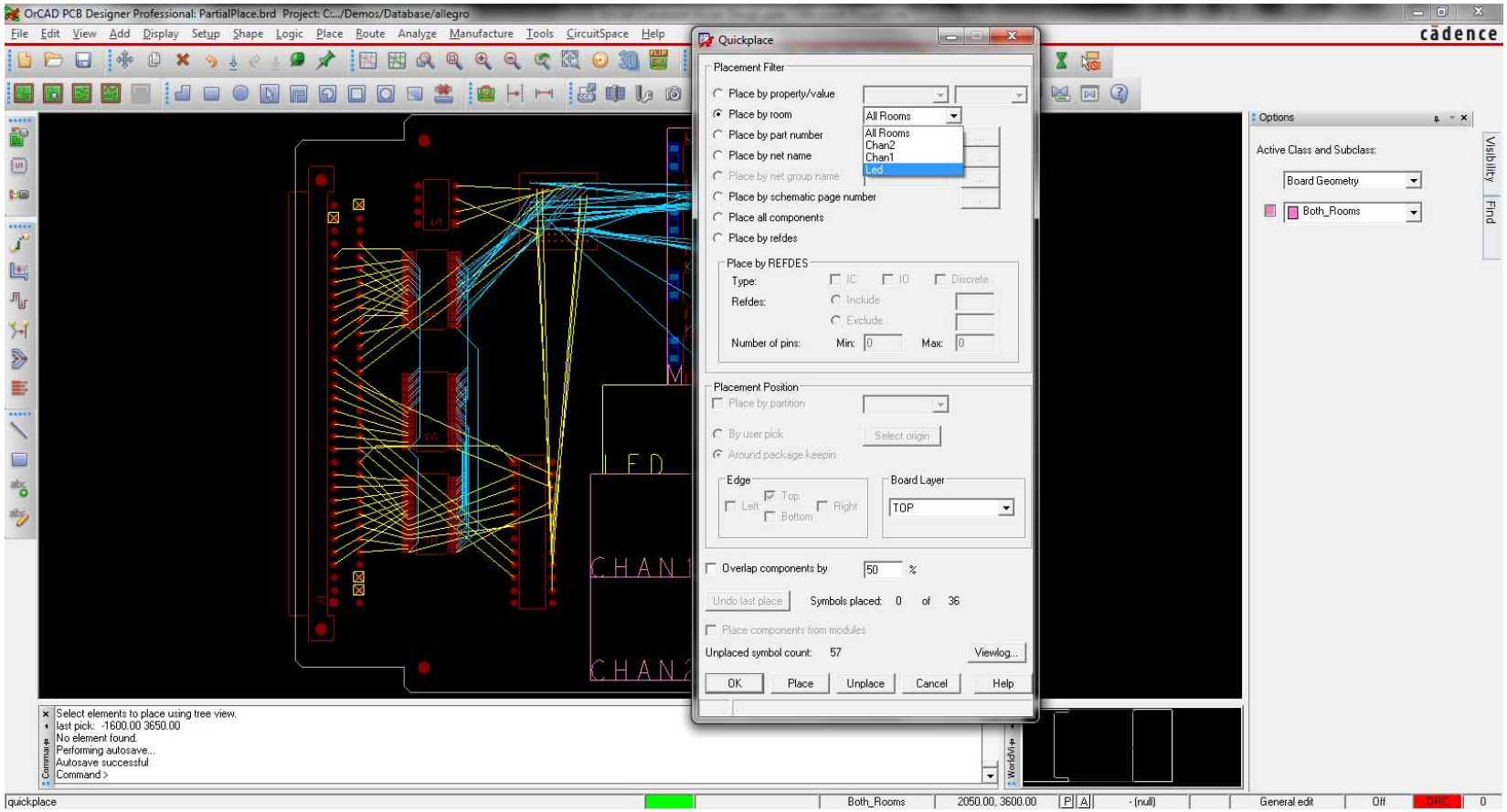
Placing Components with ROOM Properties

Place > Manually > Room



Placing Components with ROOM Properties

Place > Quickplace > Room

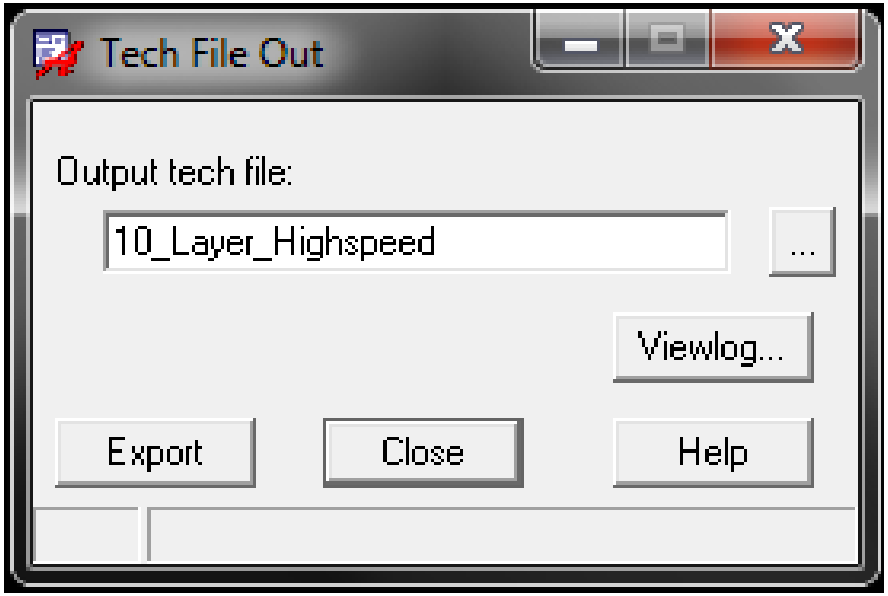


Using Technology Files

- Technology files (tech files) contain:
  - Parameters
  - Design-level constraint data
  - Constraint Modes
  - Cross-section
  - User-defined properties
- Stored on disk
- Preserve company standards while creating new databases
- Results reported in techfile.log

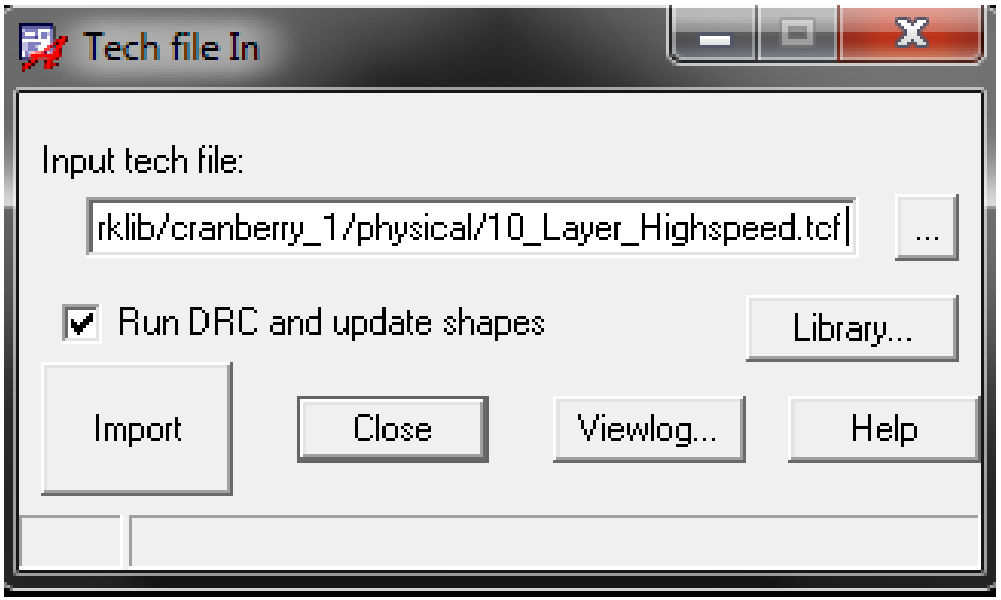
Using Technology Files - Export

File > Export > Techfile…



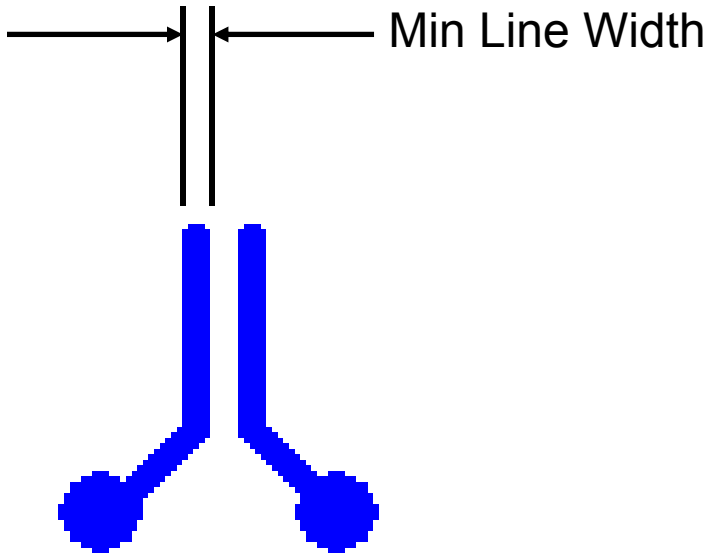
Using Technology Files - Import

File > Import > Techfile…



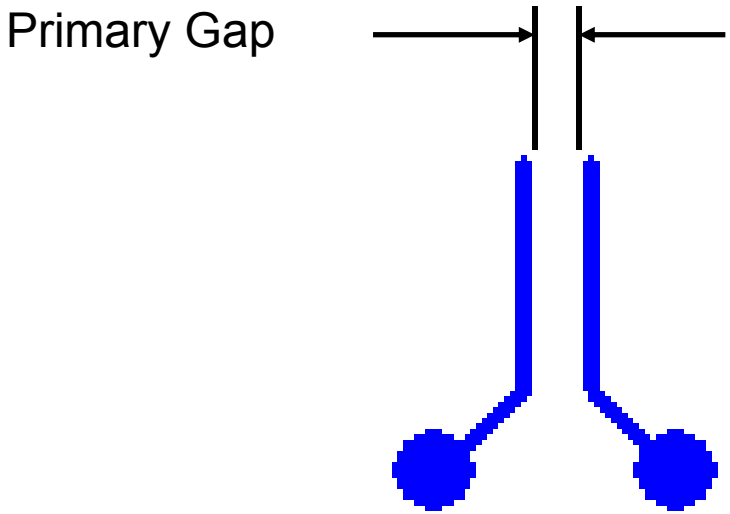
Anatomy of a Differential Pair
Minimum Line Width

- The trace width that should be used to route the differential pair nets the majority of the time
- The width you prefer your differential pairs to be routed



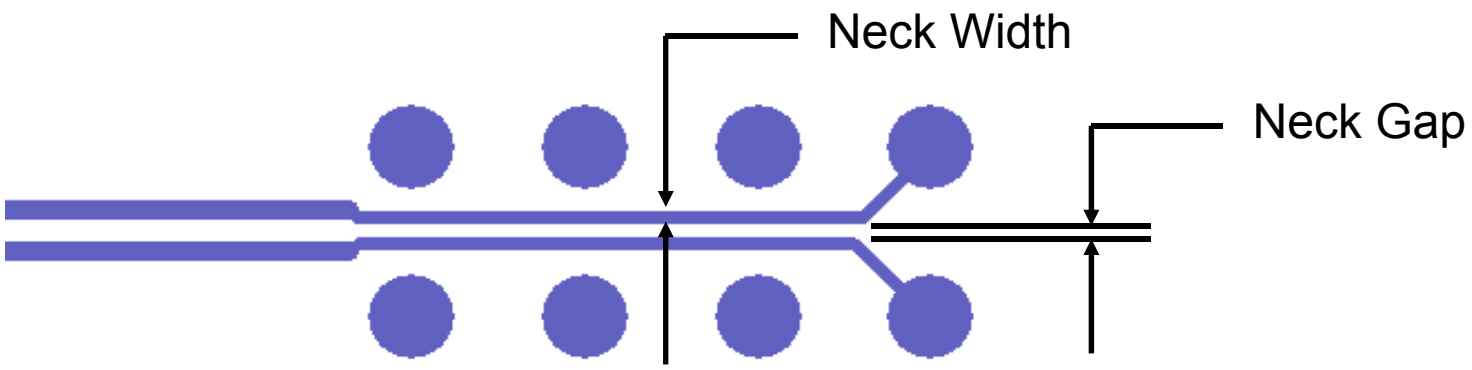
Anatomy of a Differential Pair
Primary Gap

- The Spacing, edge to edge, that should be used to route the differential pair nets the majority of the time
- The rule you prefer your differential pairs to follow
- This only applies to the two differential pair nets. Other net spacing to the differential pair nets is controlled by the Spacing Rule set Line to Line clearance



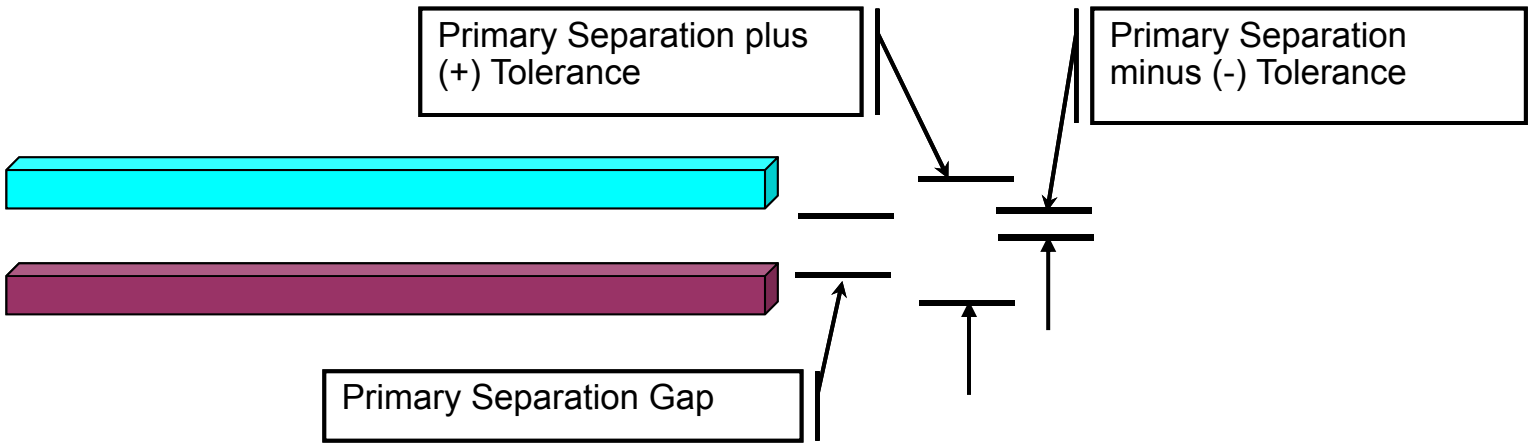
Anatomy of a Differential Pair
Neck Width and Neck Gap

- Rules to be applied when the traces must “squeeze” down to be routed between pins/vias (for example, in BGA areas)
- Neck Gap is the new spacing, edge to edge, that should be routed to route the differential pair
- Neck Width is the new trace width that should be used to route the differential pairs



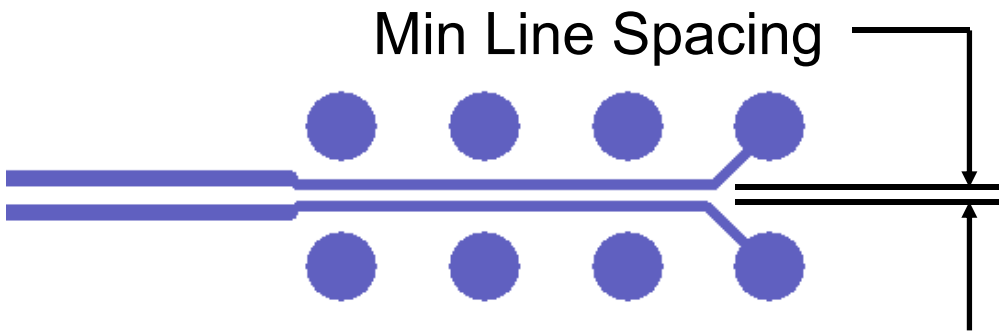
Anatomy of a Differential Pair
Separation Gap Tolerance

- Coupled Tolerance (+)/(-)
  - Provides a coupling range based on the Primary Separation Gap
  - Summing Primary Separation Gap and Coupled Tolerance (+) provides the maximum coupled gap
  - Subtracting Primary Separation Gap and Coupled Tolerance (-) provides the minimum coupled gap
  - Values above or below these become an uncoupling event



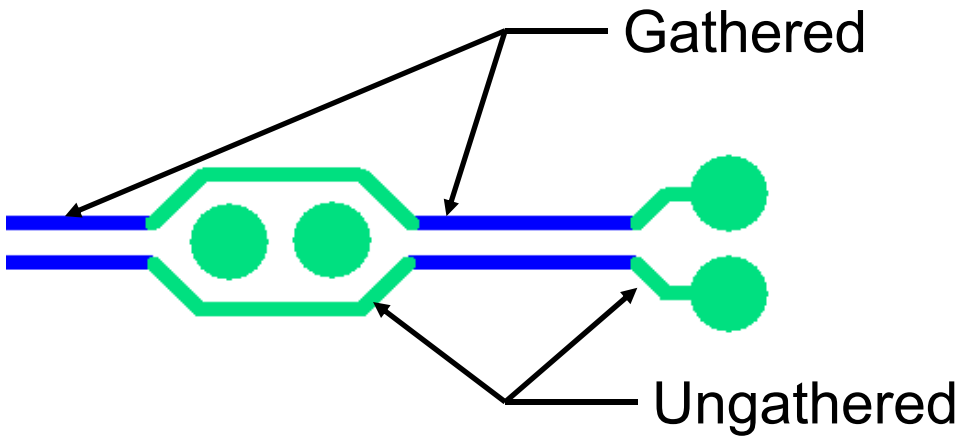
Anatomy of a Differential Pair
Minimum Line Space

- For the differential pair itself
- If set, this value must be less than your Primary Gap minus the Coupled Tolerance Minus value
- Use this value to override the Spacing Constraint set line-to-line value



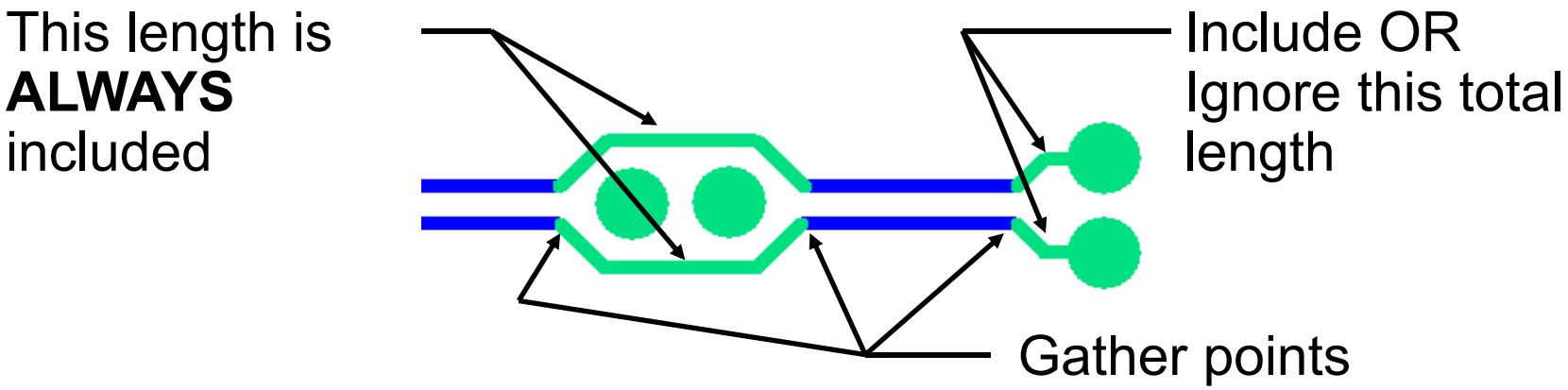
Anatomy of a Differential Pair
Max Uncoupled Length

- Maximum length of uncoupled trace summed throughout the entire differential pair route
- See green etch below:



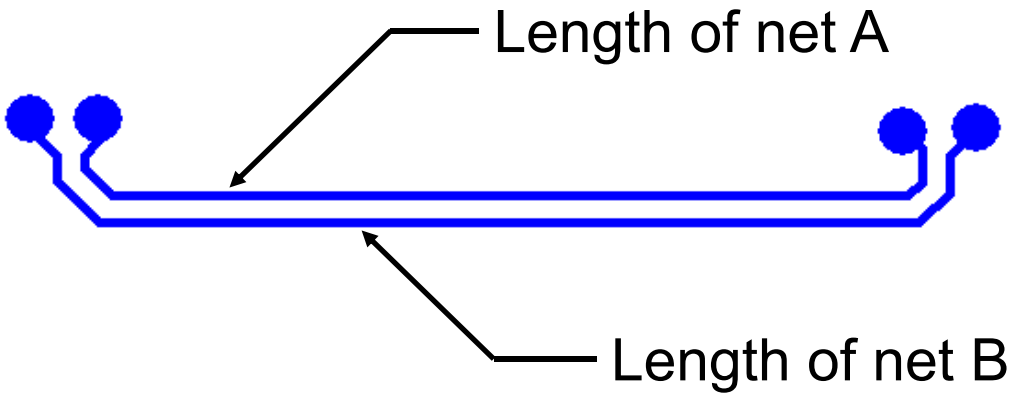
Anatomy of a Differential Pair
Gather Control

- Choices are **Include** & **Ignore**
- Controls whether or not to include the etch length from pin to gather point when calculating Max uncoupled length



Anatomy of a Differential Pair
Static Phase Tolerance

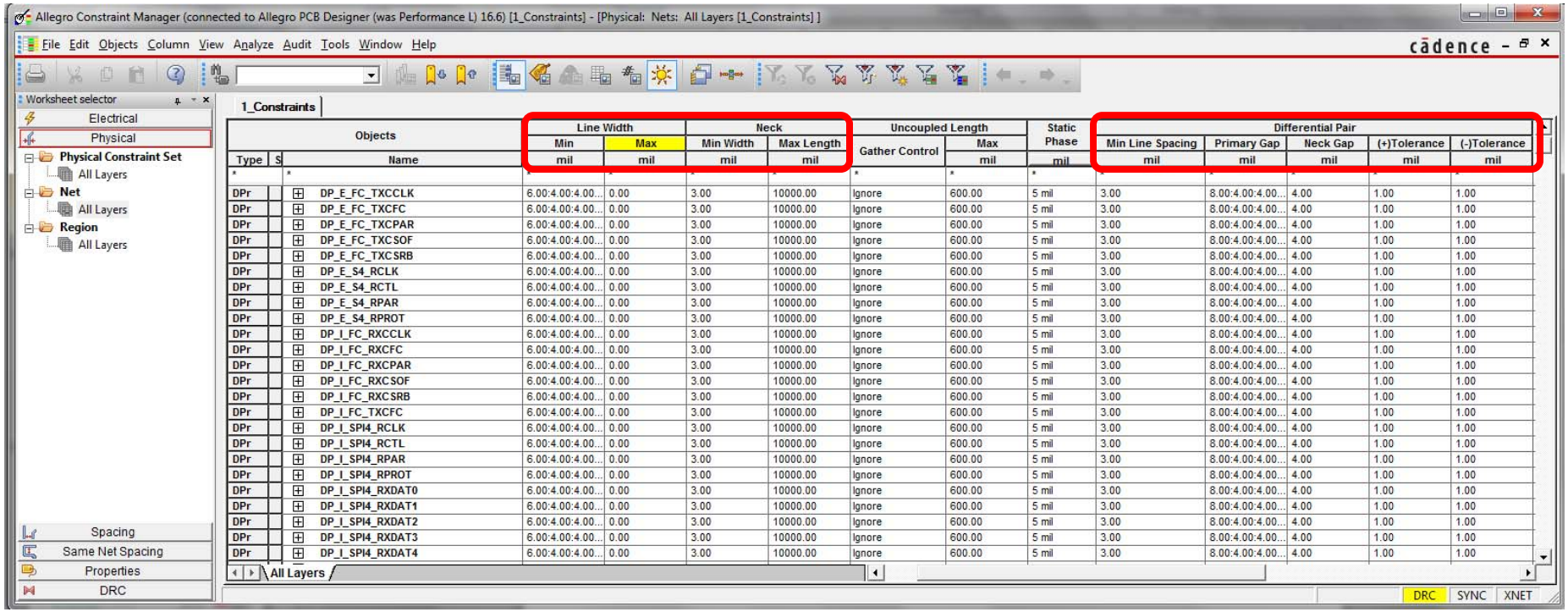
- Allowable difference in length between the differential pair nets
- When the Phase Tolerance Value is -1 (unspecified), phase checking is disabled



Note: Available only in **Allegro PCB Designer** and above.

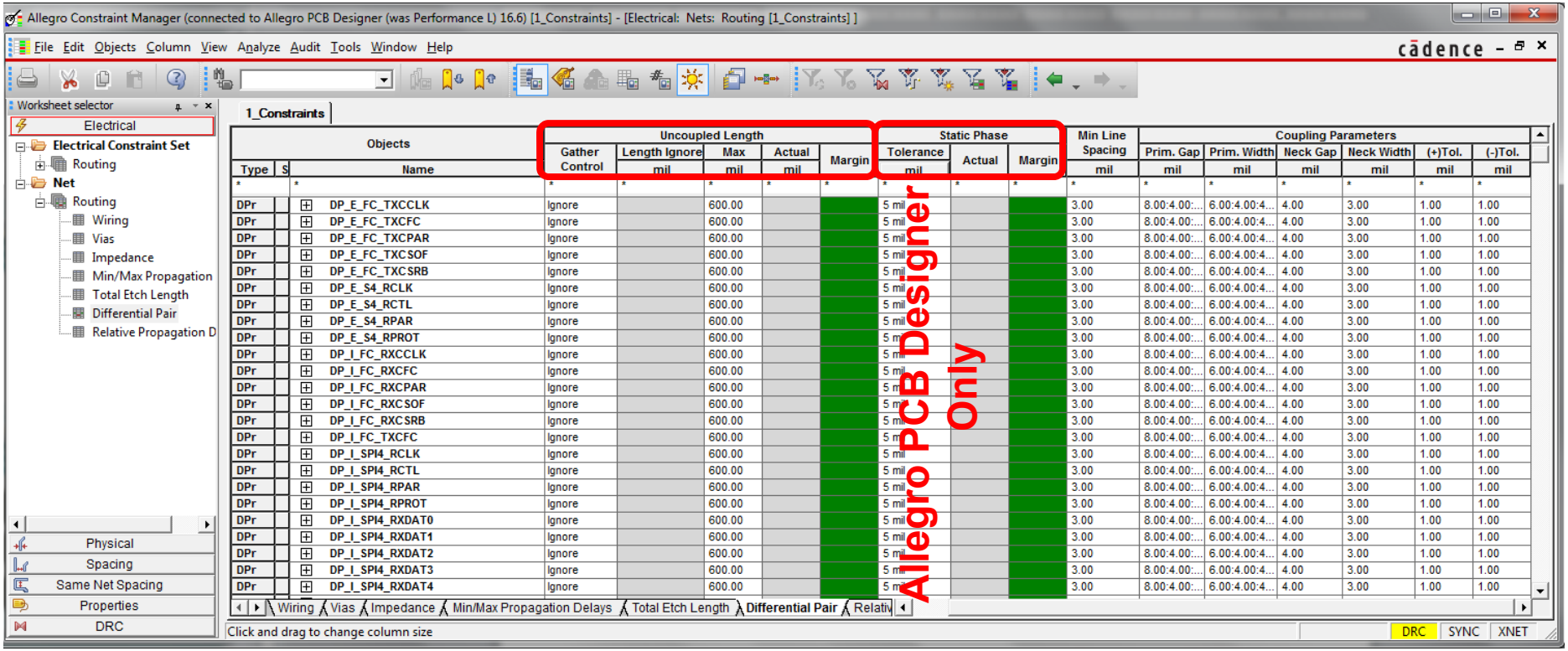
Differential Pairs
Physical Constraints

- Differential Pair Constraints set in the Physical Domain



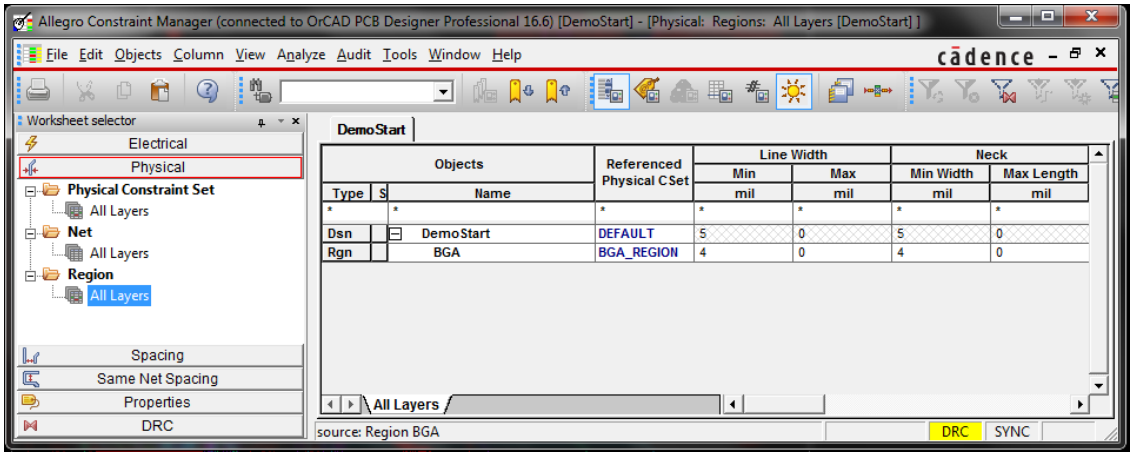
Differential Pairs
Electrical Constraints

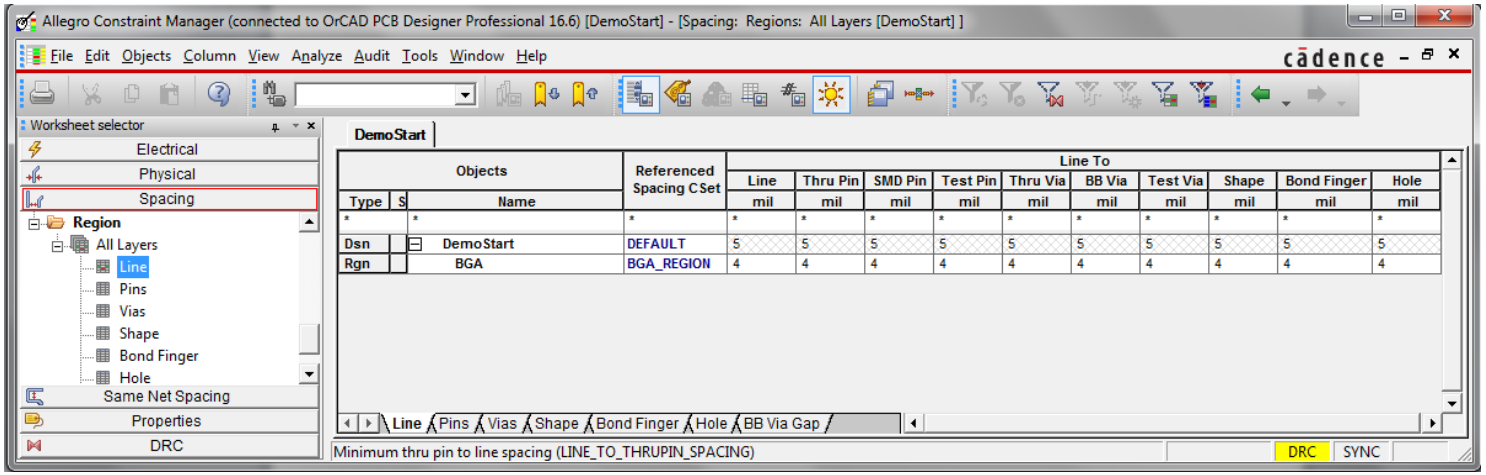
- Differential Pair Constraints set in the Electrical Domain



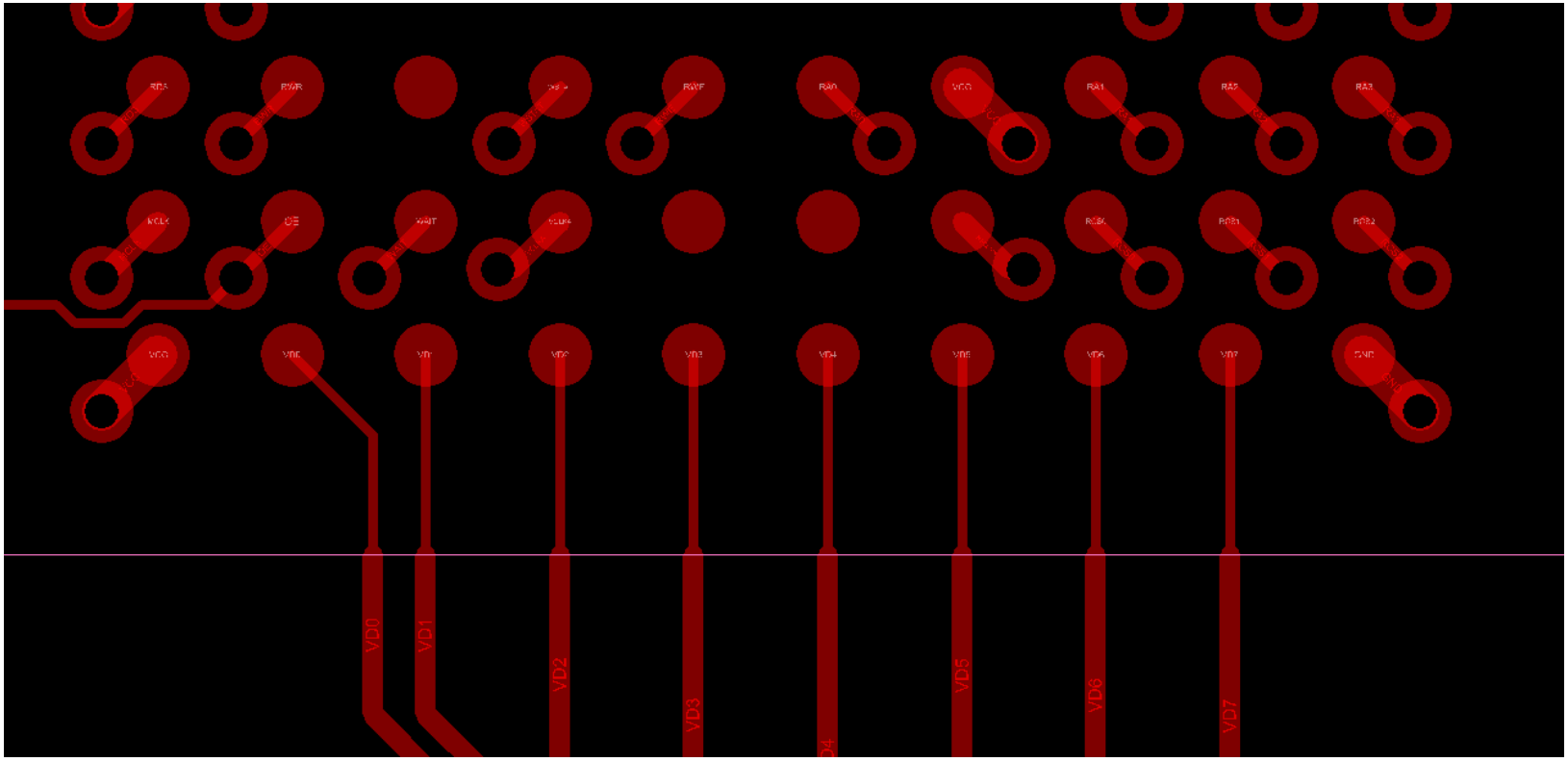
Constraint Regions

- Constraint Regions are Shapes with associated Physical and Spacing Constraints

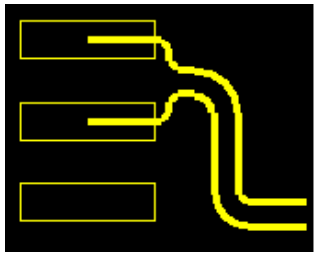


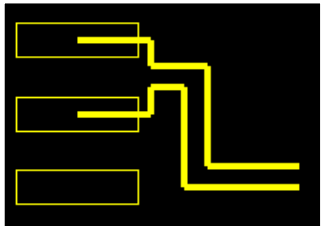


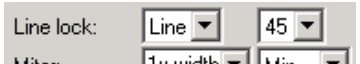
Constraint Regions

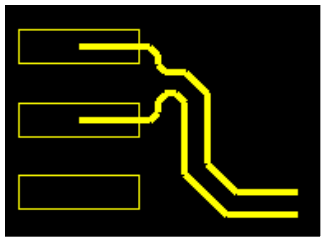


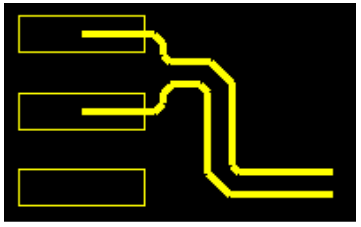
Differential Pairs
Routing Options



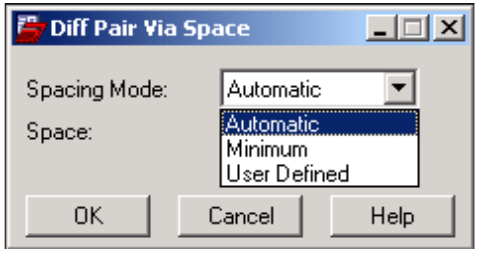




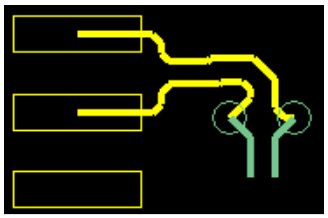




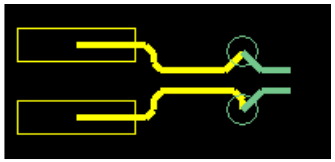
Route > Connect



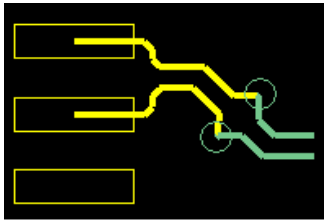
Horizontal



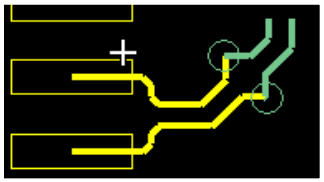
Vertical



Diagonal Up

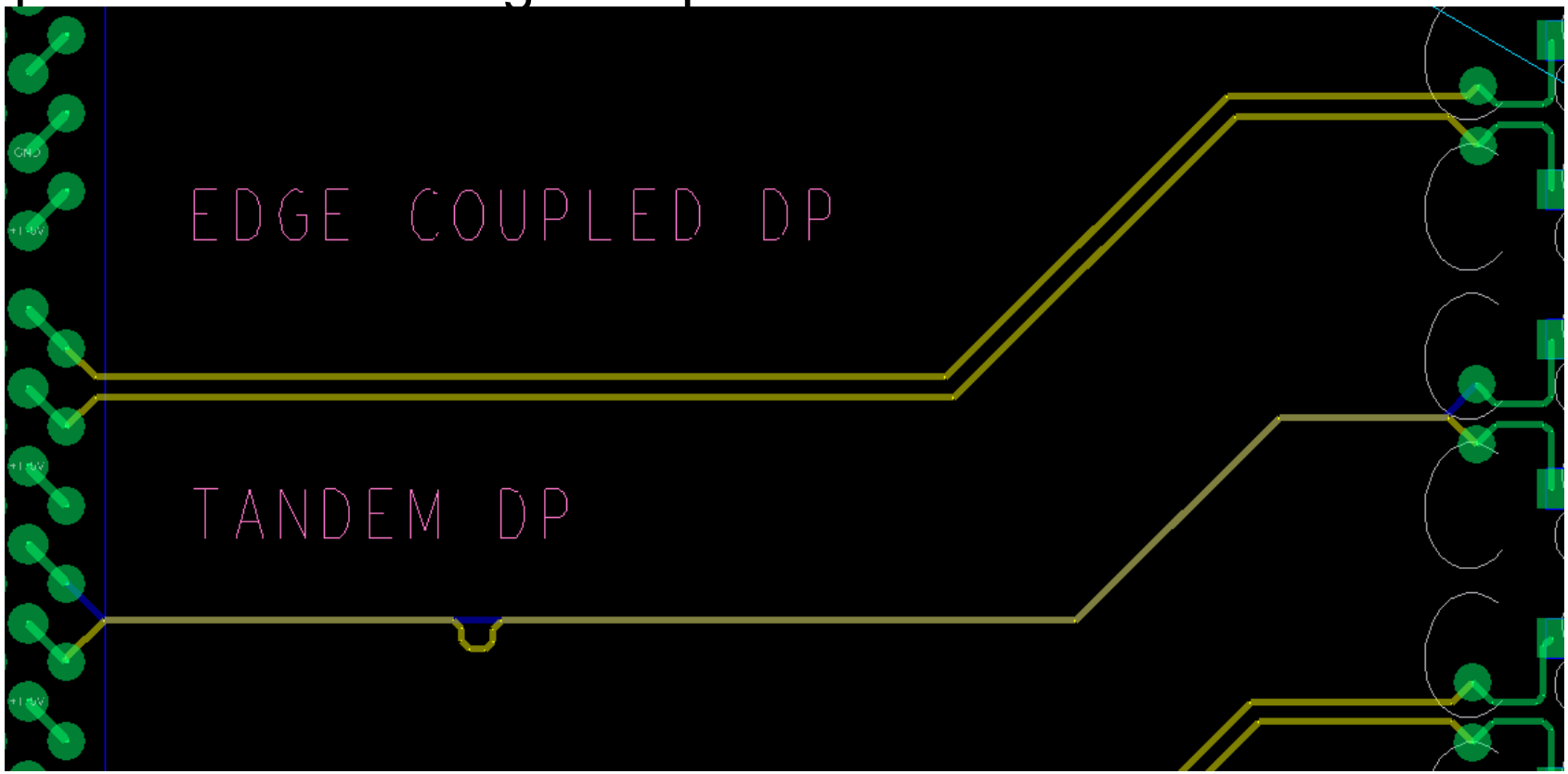


Diagonal Down



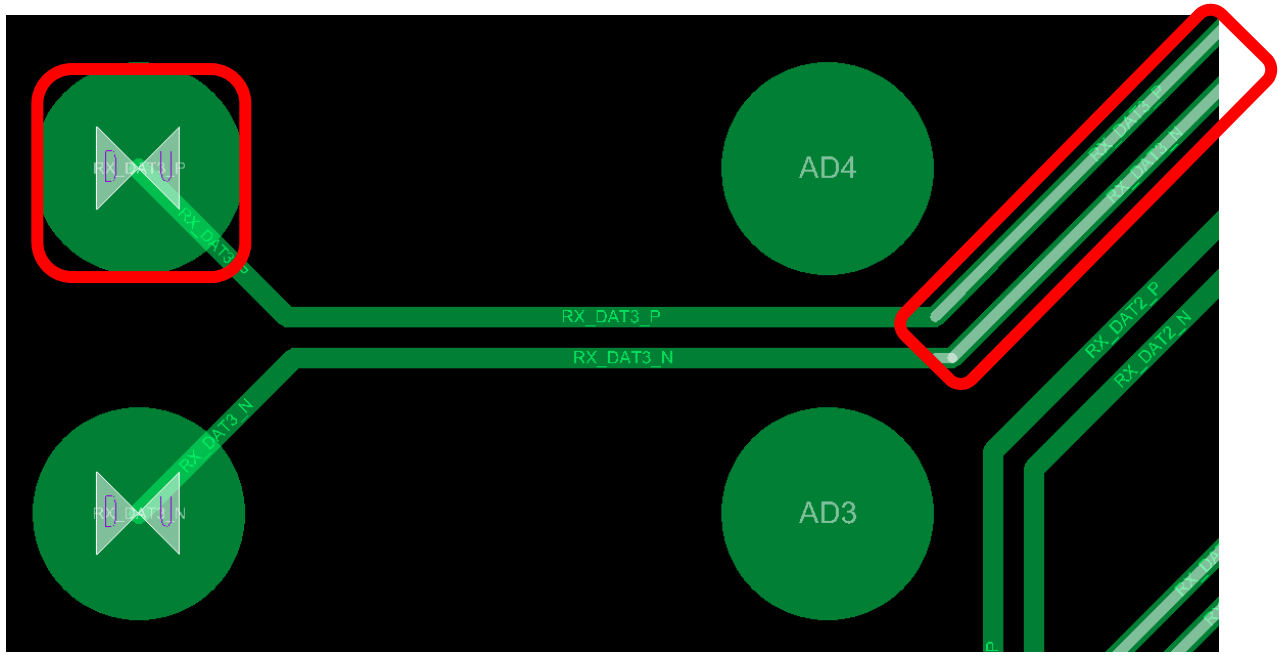
Differential Pairs Routing Options

- Once seeded, it is possible to route tandem differential pairs as well as edge coupled.



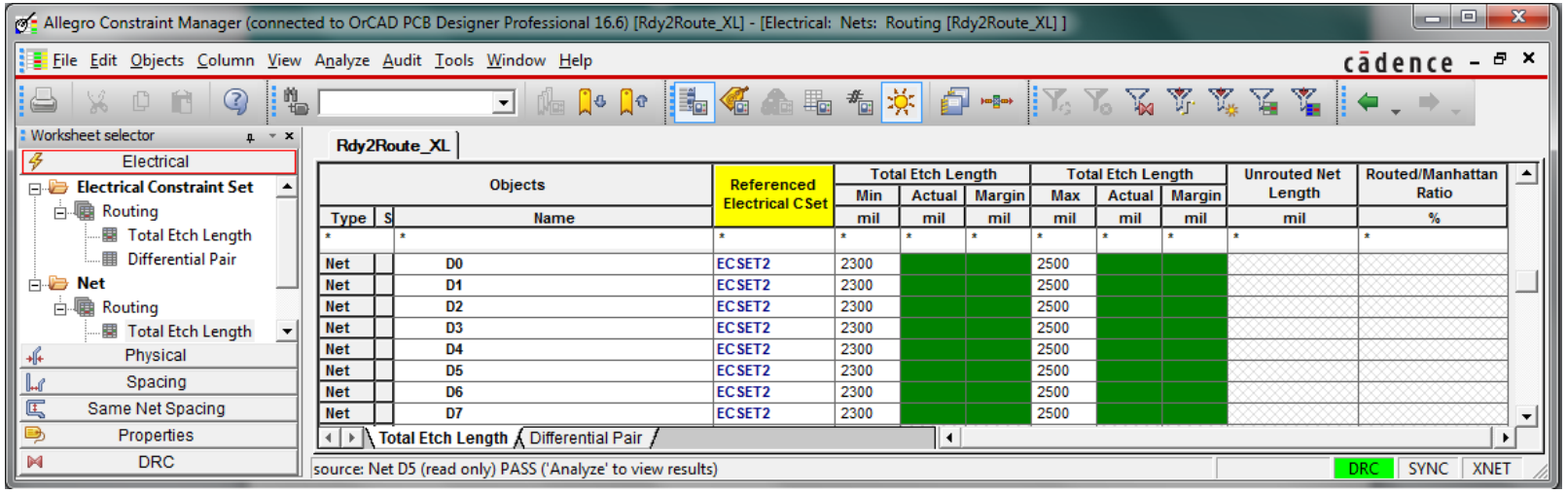
Working with Differential Pairs

- Max Uncoupled Length constraint violation Marker = DU
- Pseudo-segments graphically show uncoupling errors in the board
  - Once the length of uncoupled etch exceeds the set value, every segment that is uncoupled is highlighted in this way



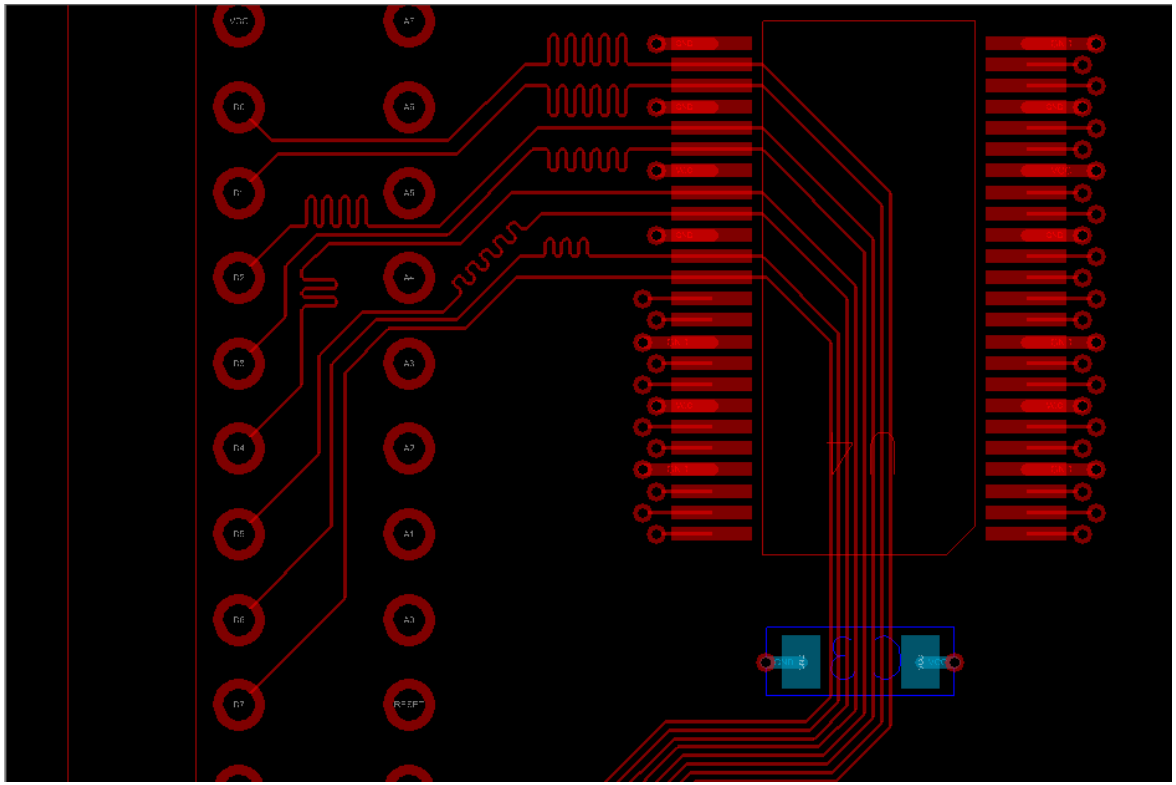
Routing Nets with Total Etch Length Constraints

- May be assigned to a Net, Xnet, Bus or Differential Pair
- Both Min and Max are etch length values with optional units
- If no units are specified, drawing units are assumed
- Either value is optional – May specify only Min, or only Max



Routing Nets with Total Etch Length Constraints: Delay Tune

- Use the Delay Tune function to add length
- May also be used to match the length of a group of nets



Constraint Resolution Physical

- Top displays element information
  - Description
  - X/Y location
  - Net name

- Bottom displays constraint rules
  - Constraint set name
  - Constraint set rules
  - Constraint values

Show Constraints

Constraint Hierarchy

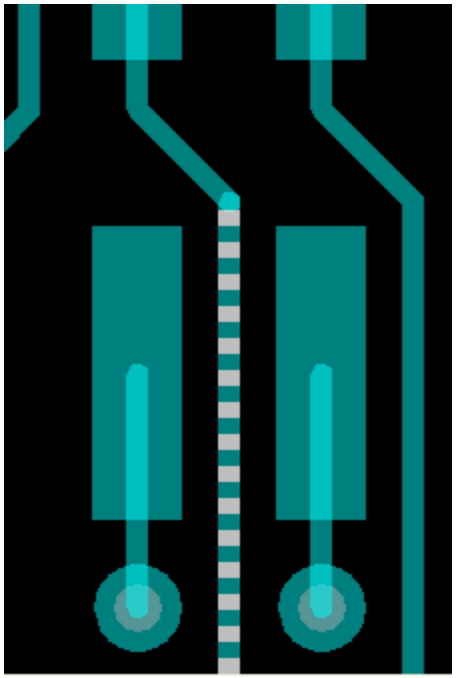
	Element 1	Element 2
Description	Vertical Line Segment "Ra3, Etch/Top"	
Location	(2100.00 2575.00)	
NetClass		
Bus		
DiffPair		
XNet		
Net	RA3	
PinPair		
NetClass-NetClass		
Region		

Segment width = 6.00 mils. Segment length = 300.00 mils.

Resolved Physical Constraints

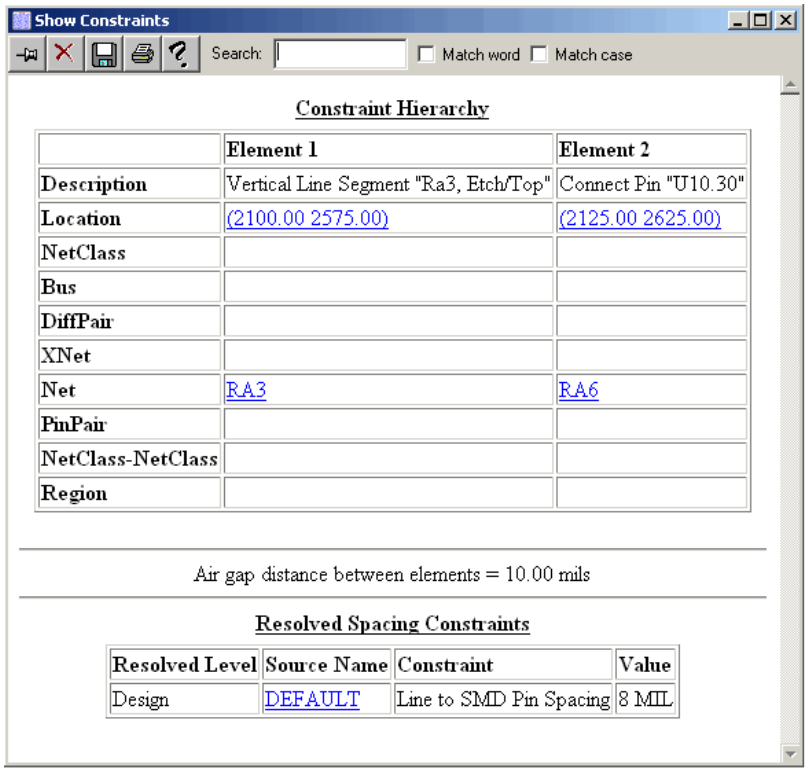
Resolved Level	Source Name	Constraint	Value
Net	MIN_LINE_WIDTH	Minimum Line Width	3 MIL
Design	DEFAULT	Minimum Neck Width	6 MIL
Design	DEFAULT	Maximum Neck Length	0 MIL
Design	DEFAULT	Maximum Line Width	0 MIL

Display > Constraint
Single select

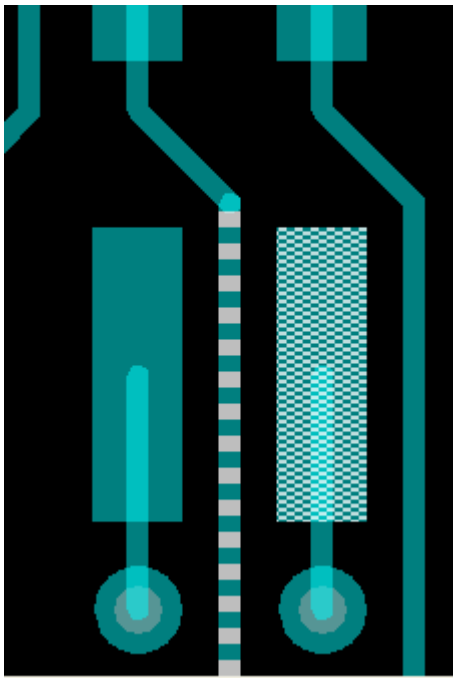


Constraint Resolution Spacing

- Top displays element information
  - Description
  - X/Y location
  - Net name
- Bottom displays constraint rules
  - Constraint set name
  - Constraint set rules
  - Constraint values



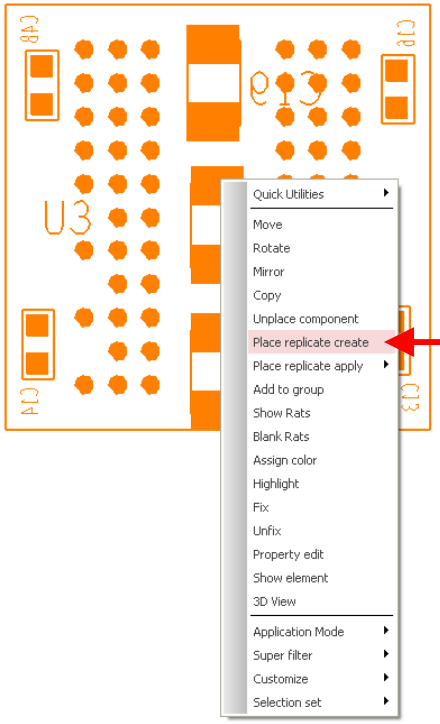
Display > Constraint
Drag Select



Design Reuse
Placement Replication

- Available in Placement Application Mode only
- Allows creation of seed circuits
- May be replicated
  - Within the current design
  - From one design to another
- May include:
  - Component Placement
  - Related Routing
  - Local Shapes
  - Reference Designator Placement

Design Reuse
Placement Replication

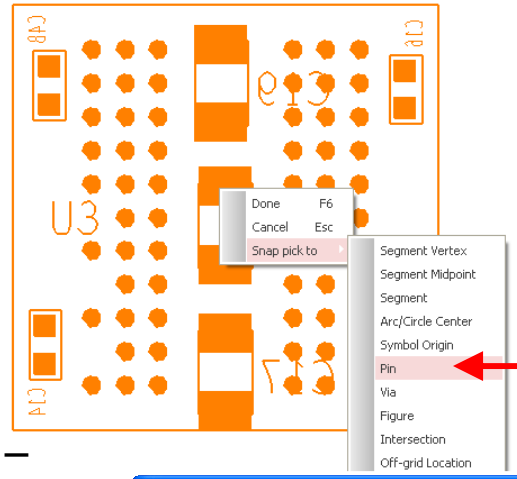


Step 1 and 2

Create original circuit and select components

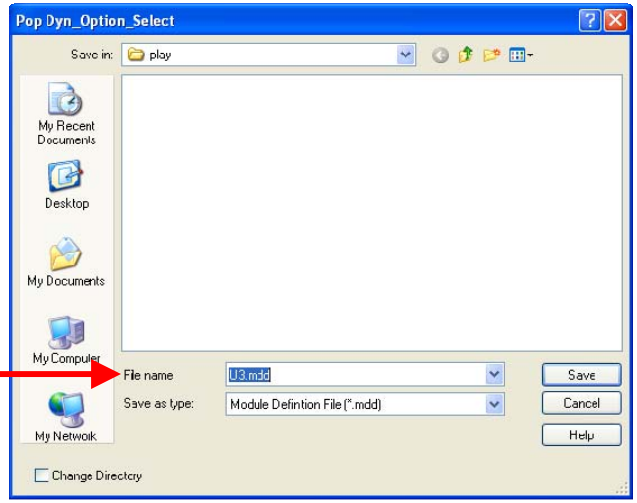
Step 3

Hover over a component and RMB – Place replicate create, then RMB - DONE



Step 4

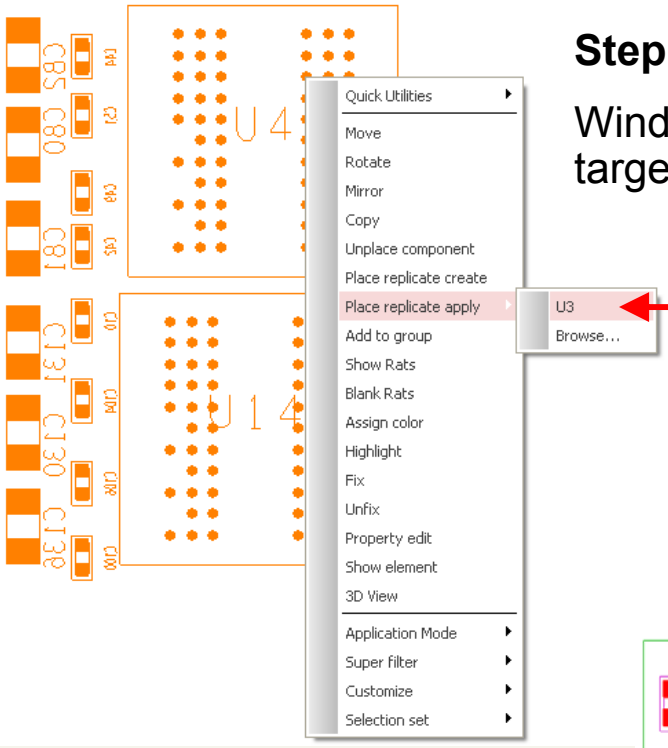
Hover over a pin and RMB – Snap pick to - Pin



Step 5

Enter a name for the Module Definition File and Save

Design Reuse
Placement Replication

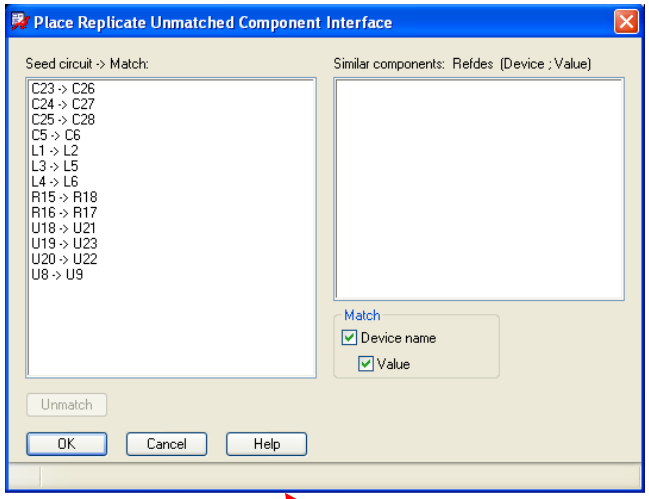


Step 1

Window - select targeted components

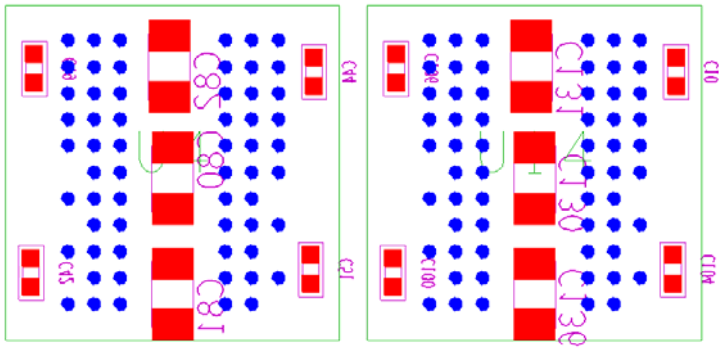
Step 2

Selected components a pin and RMB – Place replicate apply – module name



Step 3

Swap parts if needed



Step 4

Place replicated circuits

Demo Time!

- **Adding Properties in OrCAD Capture**
- **Assigning Differential Pairs in OrCAD Capture**
- **Passing Properties from OrCAD Capture to PCB Editor**
- **Placing Components in Rooms**
- **Import Technology Files**
- **Apply Differential Pair Constraints**
- **Routing Differential Pairs**
- **Routing Nets with Total Etch Length Constraints**
- **Placement Replication**