

# CAT4016

## 16-Channel Constant Current LED Driver

### Description

The CAT4016 is a 16 channel constant current driver for LED billboard and other general display applications. LED channel currents are programmed together via an external RSET resistor. Low output voltage operation on the LED channels as low as 0.4 V (for 2 to 100 mA LED current) allows for more power efficient designs.

A high-speed 4-wire serial interface of up to 25 MHz clock frequency controls each individual channel using a shift register and latch configuration. A serial output data pin (SOUT) allows multiple devices to be cascaded and programmed via one serial interface. The device also includes a blanking control pin (BLANK) that can be used to disable all channels independently of the interface.

Thermal shutdown protection is incorporated in the device to disable the LED outputs if the die temperature exceeds a set limit.

The device is available in the 24-lead SOIC, TSSOP, QSOP and the compact TQFN 4 x 4 mm packages.

### Features

- 16 Constant Current-sink Channels
- Serial Interface up to 25 MHz Clock Frequency
- 3 V to 5.5 V Logic Supply
- LED Current Range from 2 mA to 100 mA
- LED Current set by External RSET Resistor
- 300 mV LED Dropout at 30 mA
- Thermal Shutdown Protection
- Available in 24-lead SOIC, TSSOP, QSOP, and 4 x 4 mm TQFN Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

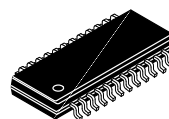
### Applications

- Billboard Display
- Marquee Display
- Instrument Display
- General Purpose Display

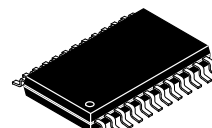


ON Semiconductor®

<http://onsemi.com>



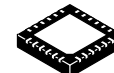
SOIC-24  
W SUFFIX  
CASE 751BK



TSSOP-24  
Y SUFFIX  
CASE 948AB

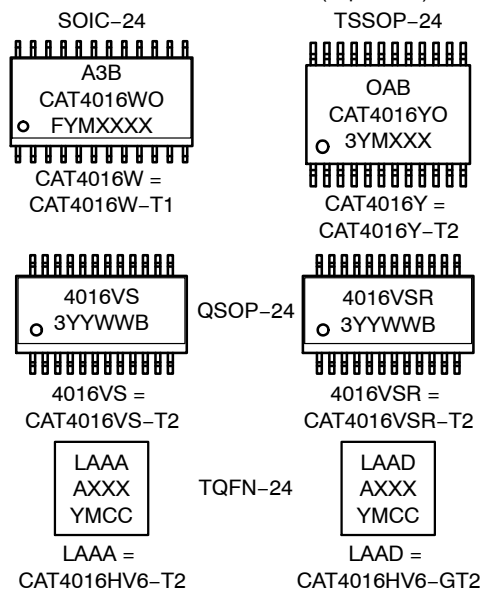


QSOP-24  
VS, VSR SUFFIX  
CASE 492AB



TQFN-24  
HV6 SUFFIX  
CASE 510AM

### MARKING DIAGRAMS (Top Views)



A = Assembly Location  
3 = Lead Finish - Matte-Tin  
B = Product Revision (Fixed as "B")  
O = Leave Blank  
F = Fab Code  
Y or YY = Production Year (Last 1 or 2 Digits)  
M = Production Month (1-9, A, B, C)  
WW = Production Week (01 - 52)  
CC = Country Code (Last Two Digits)  
XXX or XXXX = Last 3 or 4 Digits of Assembly Lot Number

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

# CAT4016

## PIN CONNECTIONS

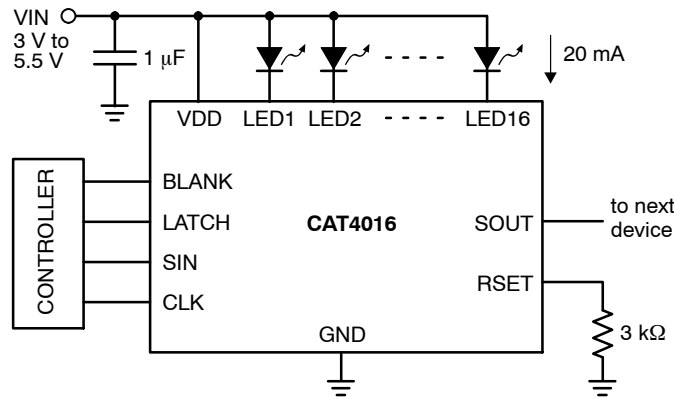
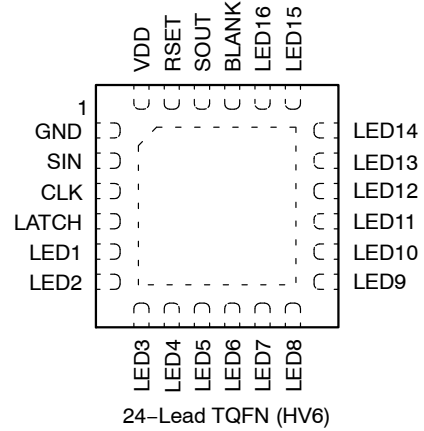
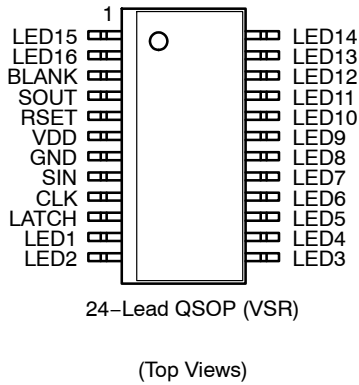
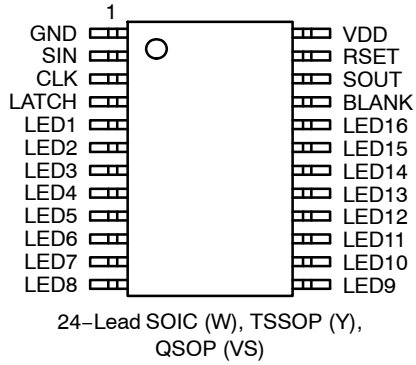


Figure 1. Typical Application Circuit

Table 1. ABSOLUTE MAXIMUM RATINGS

| Parameter   | Rating                           | Units |
|---|----------------------------------|-------|
| V <sub>DD</sub> Supply Voltage                            | 6                                | V     |
| Logic input/output voltage (SIN, SOUT, CLK, BLANK, LATCH) | -0.3 V to V <sub>DD</sub> +0.3 V | V     |
| LED <sub>n</sub> voltage                                  | 6                                | V     |
| DC output current on LED1 to LED16                        | 150                              | mA    |
| Storage Temperature Range                                 | -55 to +160                      | °C    |
| Junction Temperature Range                                | -40 to +150                      | °C    |
| Lead Soldering Temperature (10 sec.)                      | 300                              | °C    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. RECOMMENDED OPERATING CONDITIONS

| Parameter                        | Range      | Units |
|----------------------------------|------------|-------|
| V <sub>DD</sub>                  | 3.0 to 5.5 | V     |
| Voltage applied to LED1 to LED16 | 0.4 to 5.5 | V     |
| LED current RSET control range   | up to 100  | mA    |
| Ambient Temperature Range        | -40 to +85 | °C    |

# CAT4016

**Table 3. ELECTRICAL OPERATING CHARACTERISTICS**

( $V_{DD} = 5.0\text{ V}$ ,  $T_{AMB} = 25^{\circ}\text{C}$ , over recommended operating conditions unless specified otherwise.)

| Symbol                    | Name  | Conditions  | Min                     | Typ                 | Max                 | Units              |
|---------------------------|---|---|-------------------------|---------------------|---------------------|--------------------|
| <b>DC CHARACTERISTICS</b> |   |   |                         |                     |                     |                    |
| $I_{LED-ACC}$             | LED Current (any channel)   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 3\text{ k}\Omega$   | 18                      | 20                  | 22                  | mA                 |
|                           |   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 1.5\text{ k}\Omega$ | 36                      | 40                  | 44                  |                    |
|                           |   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 750\ \Omega$        |                         | 80                  |                     |                    |
| $I_{LED-MAT}$             | LED Current Matching<br>( $I_{LED} - I_{LEDAVR}$ ) / $I_{LEDAVR}$ | $V_{LED} = 1\text{ V}$ , $R_{SET} = 3\text{ k}\Omega$   |                         | $\pm 1.5$           |                     | %                  |
|                           |   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 1.5\text{ k}\Omega$ | -6.0                    | $\pm 1.5$           | +6.0                |                    |
|                           |   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 750\ \Omega$        |                         | $\pm 2.0$           |                     |                    |
| $\Delta I_{VDD}$          | LED current regulation vs. $V_{DD}$                               | $V_{DD}$ within 4.5 V and 5.5 V<br>LED current 30 mA    |                         | $\pm 0.1$           |                     | % / V              |
| $\Delta I_{VLED}$         | LED current regulation vs. $V_{LED}$                              | $V_{LED}$ within 1 V and 3 V<br>LED current 30 mA       |                         | $\pm 0.05$          |                     | % / V              |
| $I_{DDOFF}$               | Supply Current (all outputs off)                                  | $R_{SET} = 3\text{ k}\Omega$                            |                         | 3                   | 8                   | mA                 |
|                           |   | $R_{SET} = 750\ \Omega$                                 |                         | 8.5                 |                     |                    |
| $I_{DDON}$                | Supply Current (all outputs on)                                   | $R_{SET} = 3\text{ k}\Omega$                            |                         | 4                   | 9                   | mA                 |
|                           |   | $R_{SET} = 750\ \Omega$                                 |                         | 10                  |                     |                    |
| $I_{LKG}$                 | LEDn output Leakage   | $V_{LED} = 5\text{ V}$ , outputs off                    | -1                      |                     | 1                   | $\mu\text{A}$      |
| $R_{LATCH}$               | LATCH Pull-down Resistance  |   | 100                     | 180                 | 300                 | $\text{k}\Omega$   |
| $R_{BLANK}$               | BLANK Pull-up Resistance  |   | 100                     | 180                 | 300                 | $\text{k}\Omega$   |
| $V_{IH}$<br>$V_{IL}$      | Logic high input voltage<br>Logic low input voltage               |   | $0.7 \times V_{DD}$     |                     | $0.3 \times V_{DD}$ | V                  |
| $V_{HYS}$                 | Logic input hysteresis voltage                                    |   |                         | $0.1 \times V_{DD}$ |                     | V                  |
| $I_{IL}$                  | Logic Input leakage current<br>(CLK, SIN)                         | $V_I = V_{DD}$ or GND                                   | -5                      | 0                   | 5                   | $\mu\text{A}$      |
| $V_{OH}$<br>$V_{OL}$      | SOUT logic high output voltage<br>SOUT logic low output voltage   | $I_{OH} = -1\text{ mA}$<br>$I_{OL} = 1\text{ mA}$       | $V_{CC} - 0.3\text{ V}$ |                     | 0.3                 | V                  |
| $V_{RSET}$                | RSET Regulated Voltage  |   | 1.17                    | 1.20                | 1.23                | V                  |
| $T_{SD}$                  | Thermal Shutdown  |   |                         | 160                 |                     | $^{\circ}\text{C}$ |
| $T_{HYST}$                | Thermal Hysteresis  |   |                         | 20                  |                     | $^{\circ}\text{C}$ |

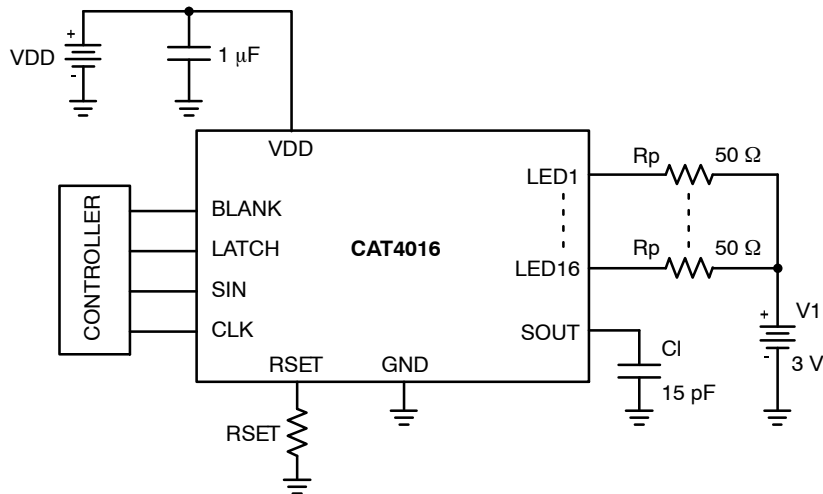
# CAT4016

**Table 4. TIMING CHARACTERISTICS**

(For  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $T_{AMB} = 25^\circ\text{C}$ , unless specified otherwise.)

| Symbol       | Name                                | Conditions                               | Min<br>(Note 1) | Typ<br>(Note 2) | Max<br>(Note 1) | Units |
|--------------|-------------------------------------|--|-----------------|-----------------|-----------------|-------|
| <b>CLK</b>   |                                     |  |                 |                 |                 |       |
| $f_{clk}$    | CLK Clock Frequency                 |  |                 |                 | 25              | MHz   |
| $t_{cwh}$    | CLK Pulse Width High                |  | 20              |                 |                 | ns    |
| $t_{cwl}$    | CLK Pulse Width Low                 |  | 20              |                 |                 | ns    |
| <b>SIN</b>   |                                     |  |                 |                 |                 |       |
| $t_{ssu}$    | Setup time SIN to CLK               |  | 4               |                 |                 | ns    |
| $t_{sh}$     | Hold time SIN to CLK                |  | 4               |                 |                 | ns    |
| <b>LATCH</b> |                                     |  |                 |                 |                 |       |
| $t_{lwh}$    | LATCH Pulse width                   |  | 20              |                 |                 | ns    |
| $T_{lh}$     | Hold time LATCH to CLK              |  | 4               |                 |                 | ns    |
| $T_{lsu}$    | Setup time LATCH to CLK             | Channel Stagger Delay                    | 800             |                 |                 | ns    |
| <b>LEDn</b>  |                                     |  |                 |                 |                 |       |
| $t_{ld}$     | LED1 Propagation delay              | LATCH to LED1 off/on                     |                 | 40              | 300             | ns    |
| $t_{ls}$     | LED Propagation delay stagger       | LED(n) to LED(n+1)                       |                 | 17              | 40              | ns    |
| $t_{lst}$    | LED Propagation delay stagger total | LED1 to LED16                            |                 | 250             |                 | ns    |
| $t_{bd}$     | BLANK Propagation delay             | BLANK to LED(n) off/on                   |                 | 60              | 300             | ns    |
| $t_{lr}$     | LED rise time (10% to 90%)          | Pull-up resistor = $50\ \Omega$ to 3.0 V |                 | 40              | 200             | ns    |
| $t_{lf}$     | LED fall time (90% to 10%)          | Pull-up resistor = $50\ \Omega$ to 3.0 V |                 | 30              | 250             | ns    |
| <b>SOUT</b>  |                                     |  |                 |                 |                 |       |
| $t_{or}$     | SOUT rise time (10% to 90%)         | $C_L = 15\text{ pF}$                     |                 | 5               |                 | ns    |
| $t_{of}$     | SOUT fall time (90% to 10%)         | $C_L = 15\text{ pF}$                     |                 | 5               |                 | ns    |
| $t_{od}$     | Propagation delay time SOUT         | CLK to SOUT                              | 8               | 15              | 25              | ns    |

1. All min and max values are guaranteed by design.
2.  $V_{DD} = 5\text{ V}$ , LED current 30 mA.



**Figure 2. Test Circuit for AC Characteristics**

# CAT4016

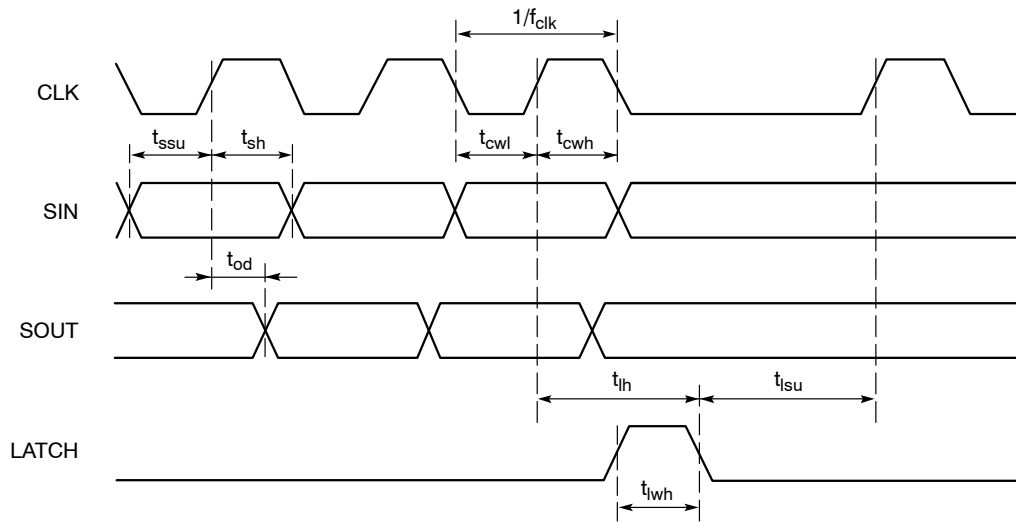


Figure 3. Serial Input Timing Diagram

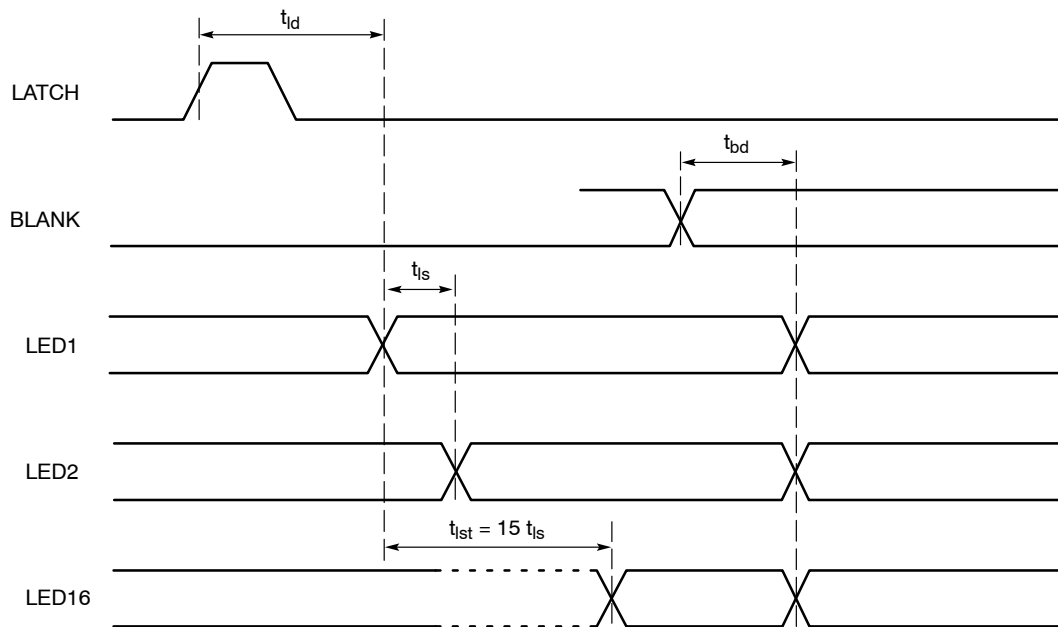


Figure 4. LED Output Timing Diagram

# CAT4016

## TYPICAL PERFORMANCE CHARACTERISTICS

( $V_{DD} = 5.0$  V, LED current 30 mA, all LEDs On,  $T_{AMB} = 25^{\circ}\text{C}$  unless otherwise specified.)

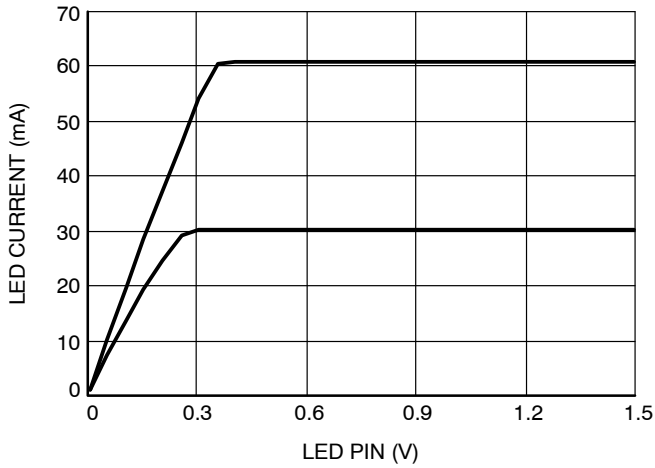


Figure 5. LED Current vs. LED Pin Voltage

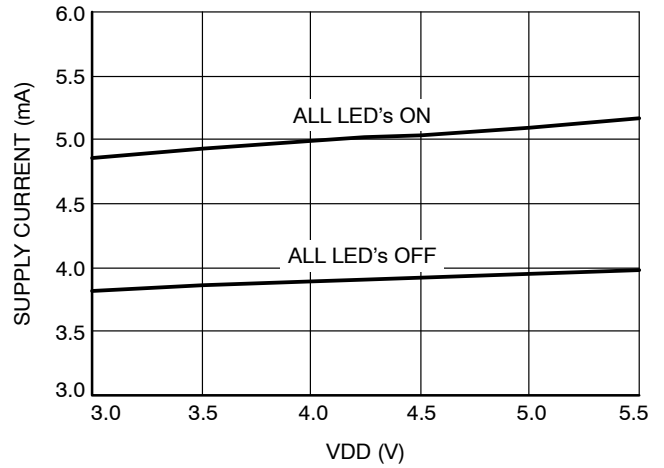


Figure 6. Supply Current vs. VDD Pin Voltage

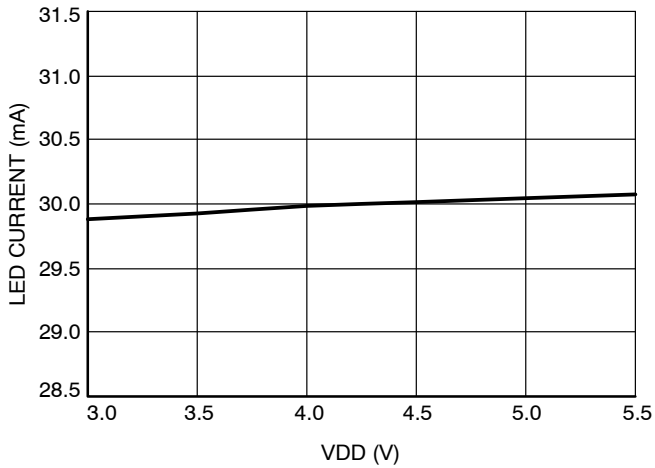


Figure 7. LED Current vs. VDD Pin Voltage

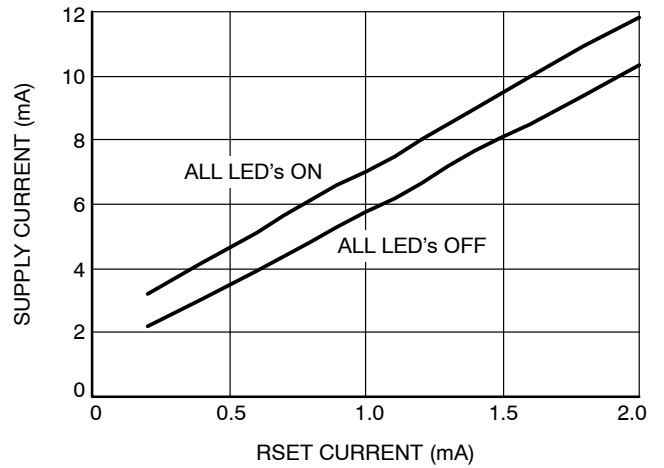


Figure 8. Supply Current vs. RSET Current

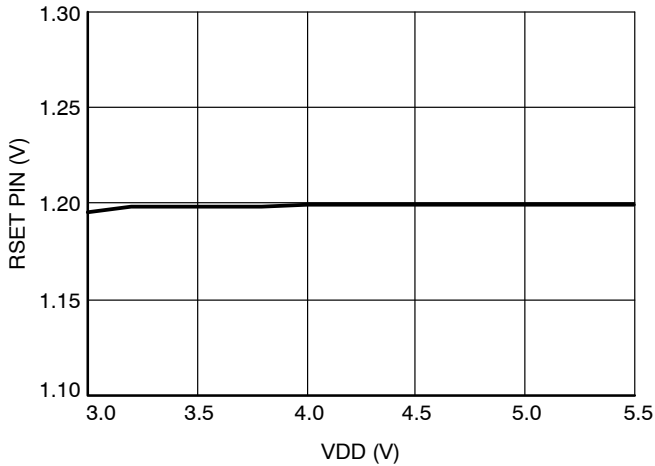


Figure 9. RSET Voltage vs. VDD Pin Voltage

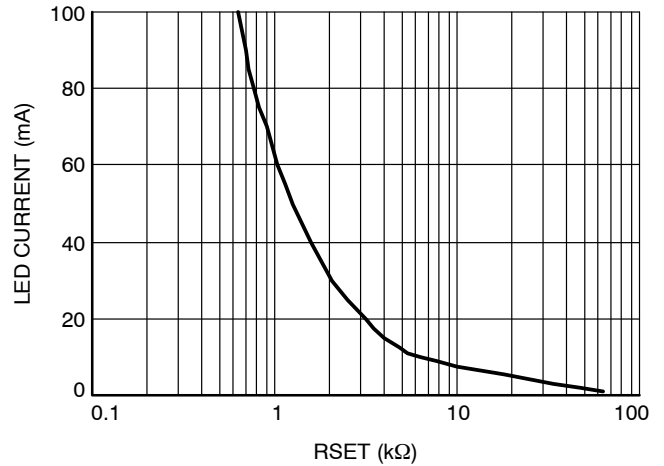


Figure 10. LED Current vs. RSET Resistor

# CAT4016

## TYPICAL PERFORMANCE CHARACTERISTICS

( $V_{DD} = 5.0$  V, LED current 30 mA, all LEDs On,  $T_{AMB} = 25^{\circ}\text{C}$  unless otherwise specified.)

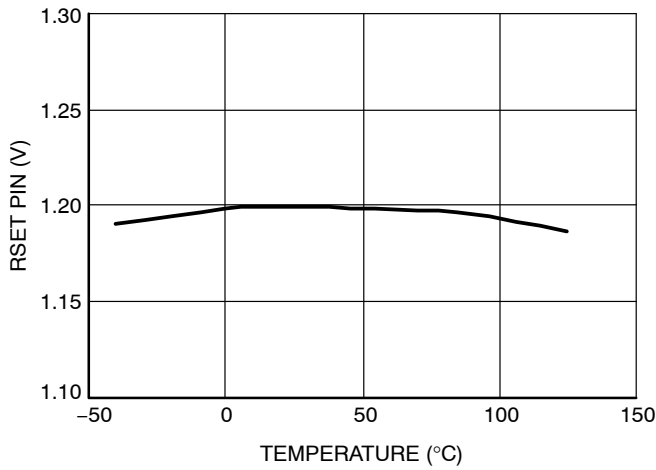


Figure 11. RSET Voltage vs. Temperature

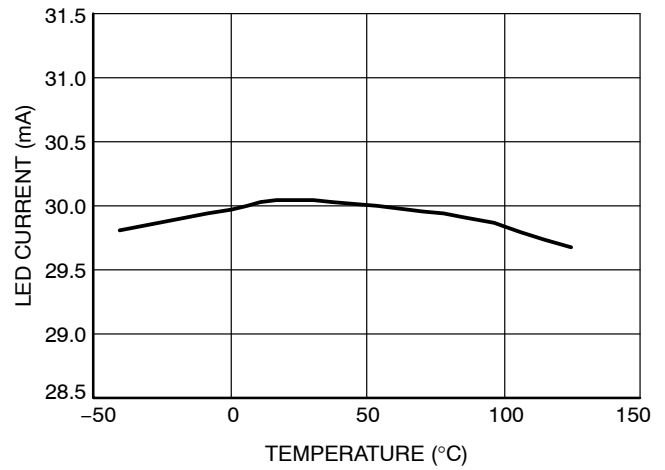


Figure 12. LED Current vs. Temperature

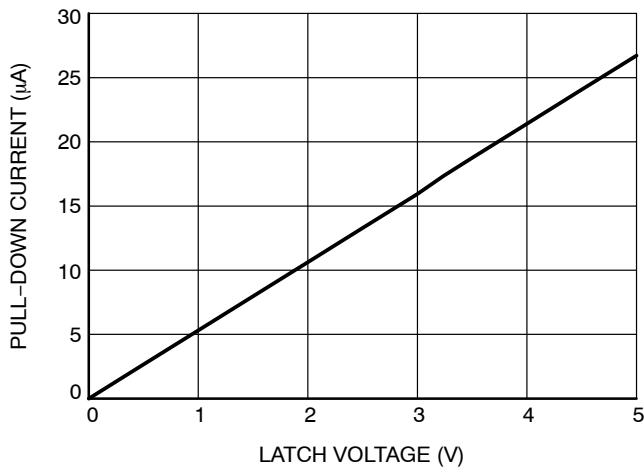


Figure 13. Internal Pull-Down Current (LATCH Pin)

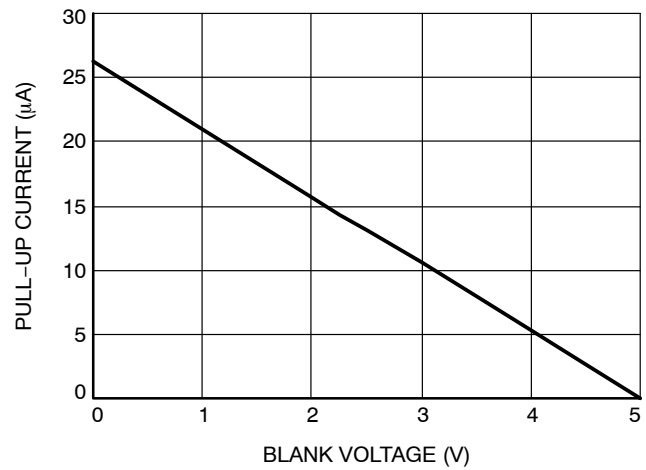


Figure 14. Internal Pull-Up Current (BLANK Pin)

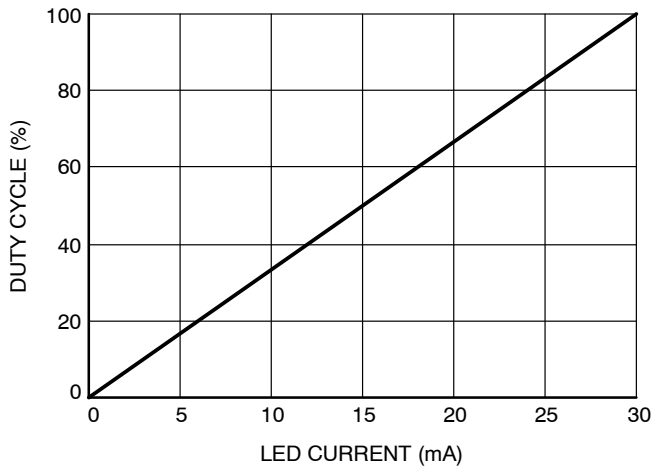


Figure 15. PWM Dimming on BLANK Pin (f = 10 kHz)

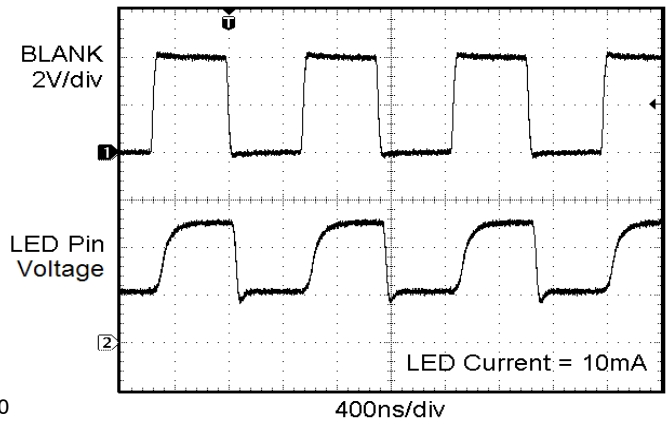


Figure 16. BLANK Transient Response

Table 5. PIN DESCRIPTION

| Name                    | Function                              |
|-------------------------|---------------------------------------|
| GND                     | Ground                                |
| SIN                     | Serial data input pin                 |
| CLK                     | Serial clock input pin                |
| LATCH                   | Latch serial data to output registers |
| LED1–LED16              | LED channel 1 to 16 cathode terminals |
| BLANK                   | Enable / disable all channels         |
| SOUT                    | Serial data output pin.               |
| RSET                    | LED current set pin                   |
| VDD                     | Positive supply Voltage               |
| TAB (TQFN package only) | Connect to GND on the PCB             |

**Pin Function**

**GND** is the ground reference pin for the device. This pin must be connected to the ground plane on the PCB.

**SIN** is the serial data input. Data is loaded into the internal register on each rising edge of CLK.

**CLK** is the serial clock input. On each rising CLK edge, data is transferred from SIN to the internal 16-bit serial shift register.

**LATCH** is the latch data input. On the rising edge of LATCH, data is loaded from the 16-bit serial shift register into the output register latch. On the falling edge, this data is latched in the output register and isolated from the state of the serial shift register.

**LED1 – LED16** are the LED current sink channels. These pins are connected to the LED cathodes. The current sinks drive the LEDs with a current equal to 50 times RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4 V.

**BLANK** is the LED channel enable and disable input pin. When low, LEDs are enabled according to the output latch register content. When high, all LEDs are off, while preserving the data in the output latch register.

**SOUT** is the serial data output of the 16-bit serial shift register. This pin is used to cascade several devices on the serial bus. The SOUT pin is then connected to the SIN input of the next device on the serial bus to cascade.

**RSET** is the LED current setting pin. A resistor is connected between this pin and ground. Each LED channel current is set to 50 times the current pulled out of the pin. The RSET pin voltage is regulated to 1.2 V.

**VDD** is the positive supply pin voltage for the entire device. A small 1 µF ceramic is recommended close to pin.



# CAT4016

## Block Diagram

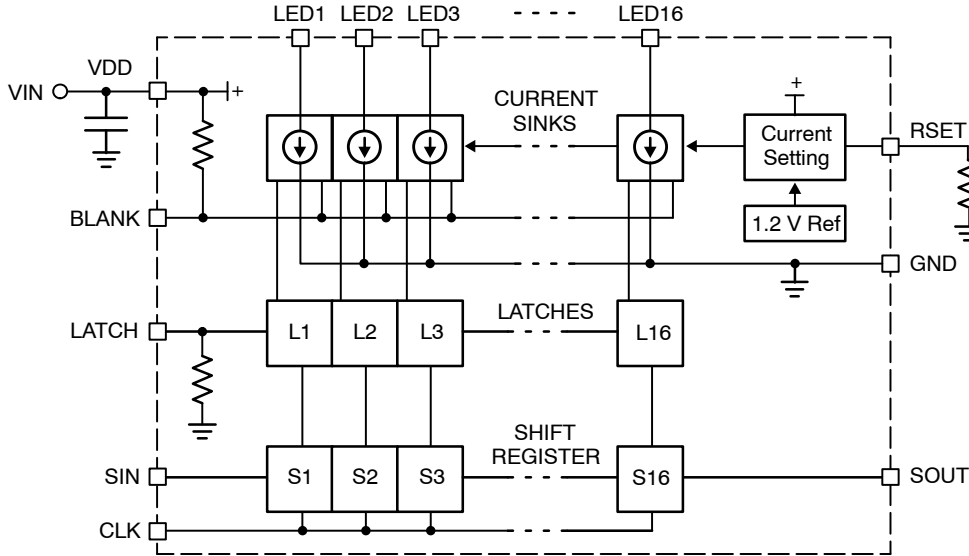


Figure 17. CAT4016 Functional Block Diagram

## Basic Operation

The CAT4016 uses 16 tightly matched current sinks to accurately regulate the LED current in each channel. The external resistor,  $R_{SET}$ , is used to set the LED channel current to 50 times the current in  $R_{SET}$ .

$$\text{LED current} = 50 \times \frac{1.2}{R_{SET}}$$

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a maximum dropout of 0.4 V for most current and supply voltage conditions. This helps improve the heat dissipation and efficiency of the LED driver.

Upon power-up, an under-voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the under-voltage lockout threshold has been reached the device can be programmed.

The driver delays the activation of each consecutive LED output channel by 17 ns (typical). Relative to LED1, LED2 is delayed by 17 ns, LED3 by 34 ns and LED16 by 250 ns typical. The delay is introduced when LATCH is activated. The delay minimizes the inrush current on the LED supply by staggering the turn on and off current spikes over a period of time and therefore allowing usage of smaller bypass capacitors.

Pull-up and pull-down resistors are internally provided to set the state of the BLANK and LATCH pins to the off-state when not externally driven.

## Serial Interface

A high-speed serial 4-wire interface is provided to program the state of each LED on or off. The interface contains a 16-bit serial to parallel shift register (S1-S16) and a 16-bit latch (L1-L16). Programming the serial to parallel register is accomplished via SIN and CLK input pins. On each rising edge of the CLK signal, the data from SIN is moved through the shift register serially. Data is also moved out of SOUT which can be connected to a next device if programming more than one device on the same interface.

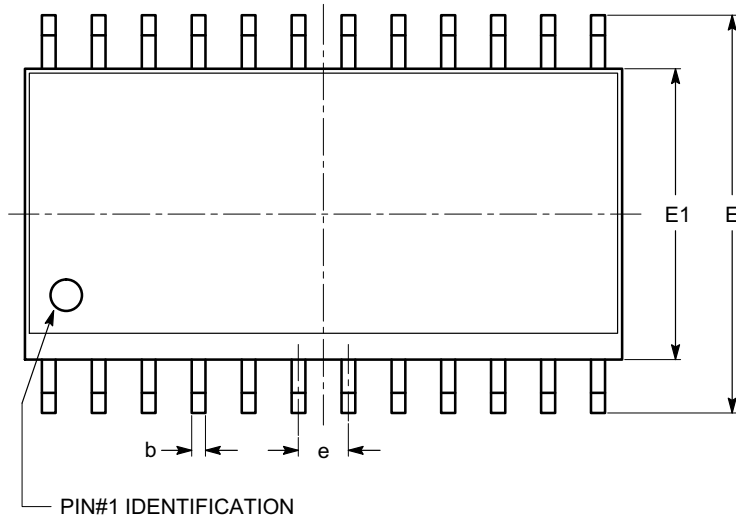
On the rising edge of LATCH, the data contents of the serial to parallel shift register is reflected in the latches. On the falling edge of LATCH, the state of the serial to parallel register at that particular time is saved in the latches and does not change irrespective of the contents of the serial to parallel register.

BLANK is used to disable all LEDs (turn off) simultaneously while maintaining the same data in the latch register. When low, the LED outputs reflect the data in the latches. When high, all outputs are high impedance (zero current).

# CAT4016

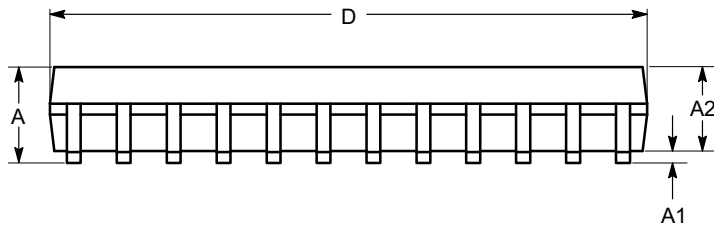
## PACKAGE DIMENSIONS

SOIC-24, 300 mils  
CASE 751BK-01  
ISSUE O

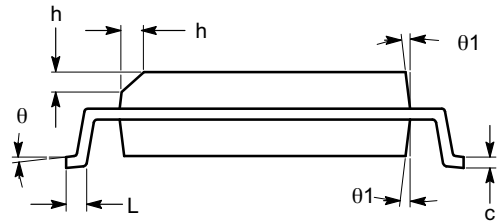


TOP VIEW

| SYMBOL     | MIN      | NOM | MAX   |
|------------|----------|-----|-------|
| A          | 2.35     |     | 2.65  |
| A1         | 0.10     |     | 0.30  |
| A2         | 2.05     |     | 2.55  |
| b          | 0.31     |     | 0.51  |
| c          | 0.20     |     | 0.33  |
| D          | 15.20    |     | 15.40 |
| E          | 10.11    |     | 10.51 |
| E1         | 7.34     |     | 7.60  |
| e          | 1.27 BSC |     |       |
| h          | 0.25     |     | 0.75  |
| L          | 0.40     |     | 1.27  |
| $\theta$   | 0°       |     | 8°    |
| $\theta 1$ | 5°       |     | 15°   |



SIDE VIEW



END VIEW

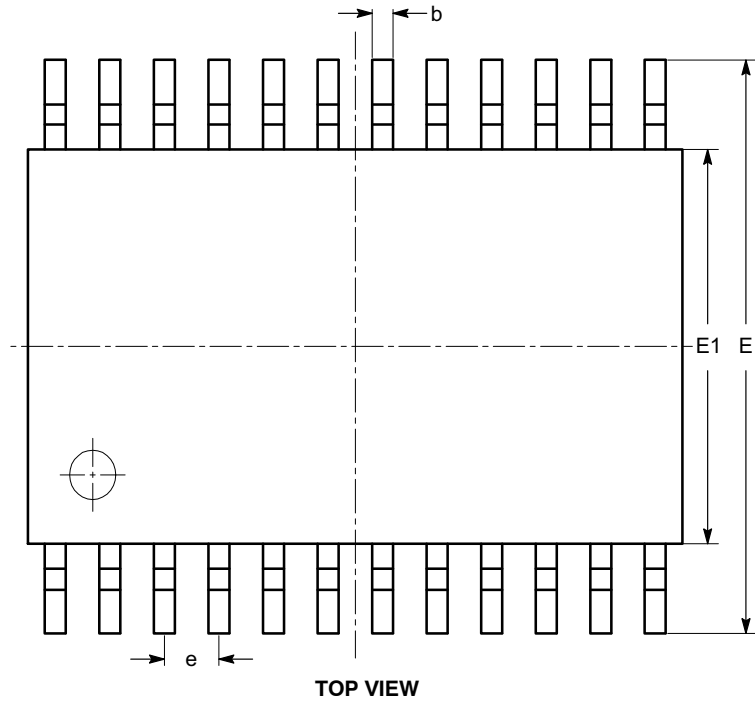
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

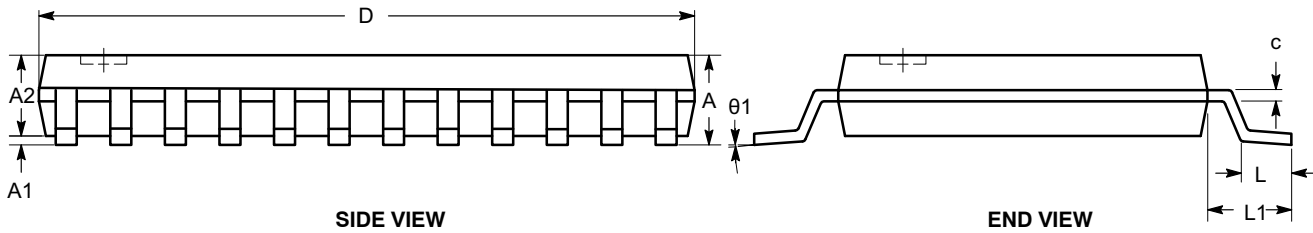
# CAT4016

## PACKAGE DIMENSIONS

TSSOP24, 4.4x7.8  
CASE 948AR-01  
ISSUE A



| SYMBOL   | MIN      | NOM  | MAX  |
|----------|----------|------|------|
| A        |          |      | 1.20 |
| A1       | 0.05     |      | 0.15 |
| A2       | 0.80     |      | 1.05 |
| b        | 0.19     |      | 0.30 |
| c        | 0.09     |      | 0.20 |
| D        | 7.70     | 7.80 | 7.90 |
| E        | 6.25     | 6.40 | 6.55 |
| E1       | 4.30     | 4.40 | 4.50 |
| e        | 0.65 BSC |      |      |
| L        | 0.50     | 0.60 | 0.70 |
| L1       | 1.00 REF |      |      |
| $\theta$ | 0°       |      | 8°   |



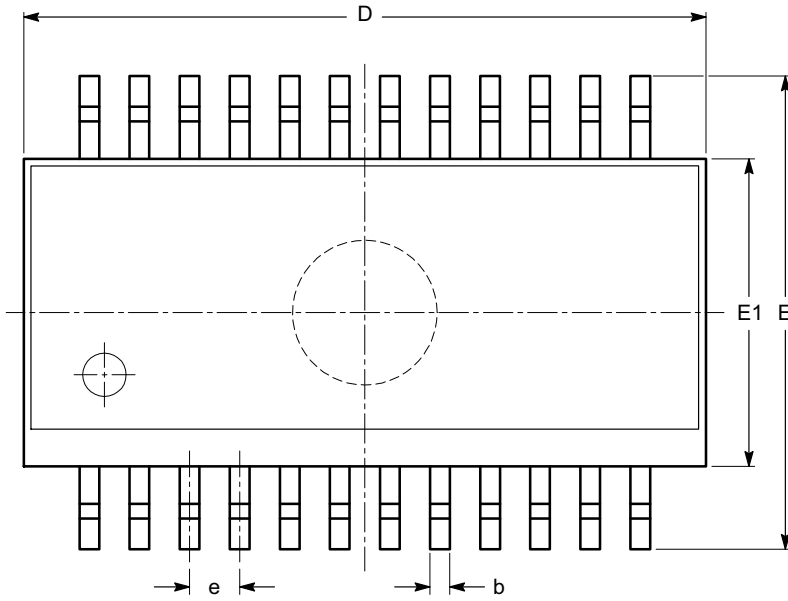
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

# CAT4016

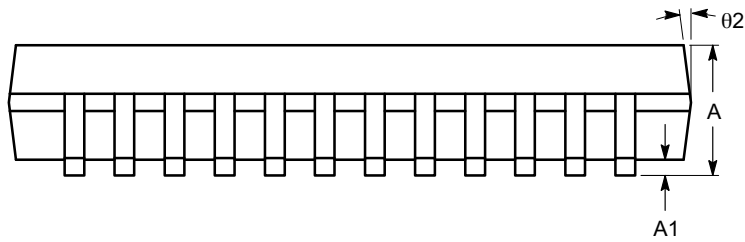
## PACKAGE DIMENSIONS

QSOP-24, 150 mils  
CASE 492AB-01  
ISSUE O

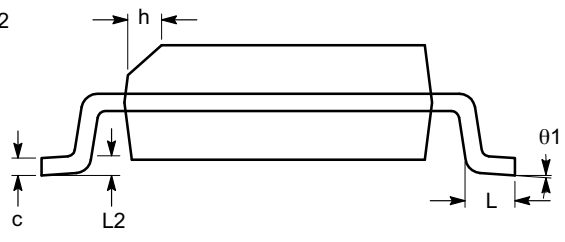


| SYMBOL     | MIN       | NOM | MAX  |
|------------|-----------|-----|------|
| A          | 1.37      |     | 1.73 |
| A1         | 0.10      |     | 0.25 |
| b          | 0.20      |     | 0.30 |
| c          | 0.19      |     | 0.25 |
| D          | 8.56      |     | 8.74 |
| E          | 5.82      |     | 6.19 |
| E1         | 3.81      |     | 3.98 |
| e          | 0.635 BSC |     |      |
| h          | 0.28      |     | 0.48 |
| L          | 0.41      |     | 0.86 |
| L2         | 0.254 BSC |     |      |
| $\theta 1$ | 0°        |     | 8°   |
| $\theta 2$ | 7° BSC    |     |      |

TOP VIEW



SIDE VIEW



END VIEW

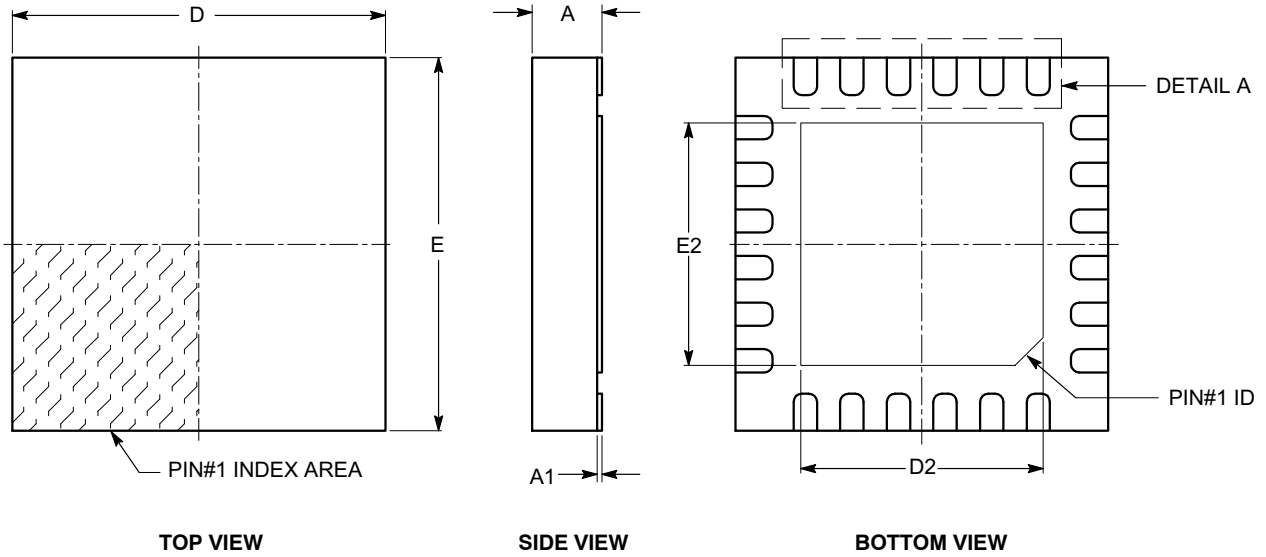
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-137.

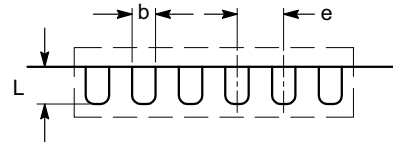
# CAT4016

## PACKAGE DIMENSIONS

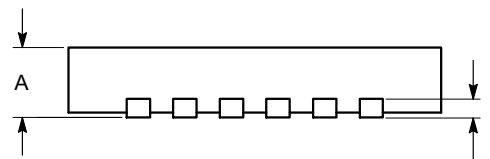
TQFN24, 4x4 AR  
CASE 510AM-01  
ISSUE O



| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      | 0.70     | 0.75 | 0.80 |
| A1     | 0.00     | -    | 0.05 |
| A3     | 0.20 REF |      |      |
| b      | 0.20     | 0.25 | 0.30 |
| D      | 4.00 BSC |      |      |
| D2     | 2.40     | -    | 2.90 |
| E      | 4.00 BSC |      |      |
| E2     | 2.40     | -    | 2.90 |
| e      | 0.50 BSC |      |      |
| L      | 0.30     | -    | 0.50 |



**DETAIL A**



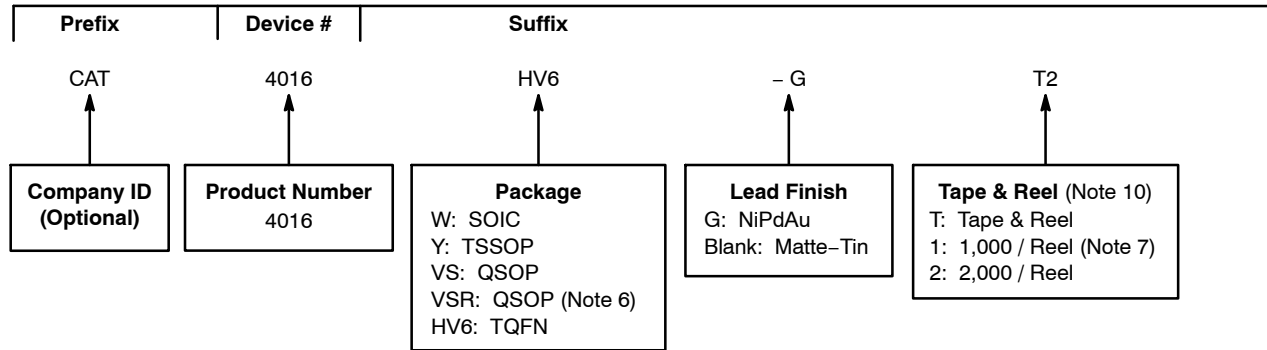
**FRONT VIEW**

**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-220.
- (3) Minimum space between leads and flag cannot be smaller than 0.15 mm.

# CAT4016


## Example of Ordering Information (Note 4)



**Table 6. ORDERING INFORMATION**

| Part Number    | Package          | Quantity per Reel | Package Marking |
|----------------|------------------|-------------------|-----------------|
| CAT4016W-T1    | SOIC24 (Note 8)  | 1,000             | CAT4016W        |
| CAT4016Y-T2    | TSSOP24 (Note 8) | 2,000             | CAT4016Y        |
| CAT4016VS-T2   | QSOP24 (Note 8)  | 2,000             | 4016VS          |
| CAT4016VSR-T2  | QSOP24 (Note 8)  | 2,000             | 4016VSR         |
| CAT4016HV6-T2  | TQFN24 (Note 8)  | 2,000             | LAAA            |
| CAT4016HV6-GT2 | TQFN24 (Note 9)  | 2,000             | LAAD            |

- All packages are RoHS-compliant (Lead-free, Halogen-free).
- The device used in the above example is a CAT4016HV6-GT2 (TQFN, NiPdAu, Tape & Reel, 2,000/Reel).
- For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
- Different pin outs, see page 2.
- SOIC package availability in 1,000/Reel. All other packages are 2,000/Reel.
- Matte-Tin Plated Finish (RoHS-compliant).
- NiPdAu Plated Finish (RoHS-compliant).
- For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative