ZR32112

1288x1032 Digital Image Sensor

Description

The PixelCam™ ZR32112 is a high-performance CMOS image sensor for digital still and video camera products.

With its *Distributed-Pixel Amplifier*™ design the pixel response is independent of its distance from the CDS circuitry. This unique architecture results in an extremely uniform pixel array. The result is a sensor with extremely low "fixed-pattern noise" without the need for off-chip "background frame subtraction" circuitry.

The bank of analog front-end circuits quantize each pixel to 10 bit resolution. This highly parallel approach eases speed requirements on individual analog circuits and reduces overall power consumption. Separate programmable Red, Green and Blue PGA circuitry enables analog-domain color balance.

The flexibility of the ZR32112 output image format permits the trade-off between resolution and frame rate. The output window size may be reduced to increase the frame rate. The output may also be sub-sampled to scan the entire array at reduced resolution and high frame rate. The image output may also be horizontally "mirrored" and vertically "flipped".

Ordering Information

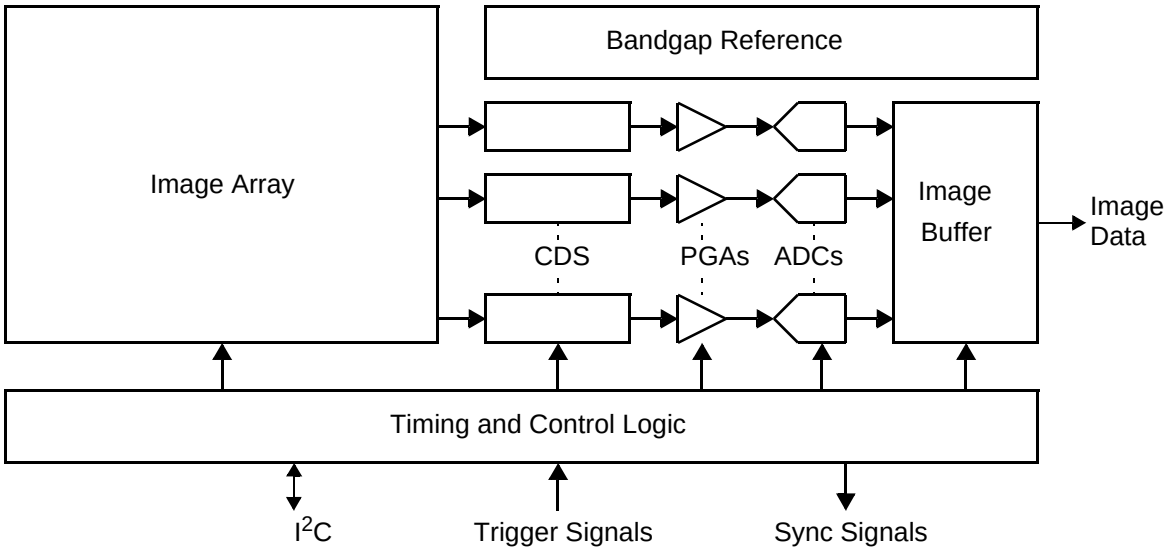
Product	Package	Order Number
ZR32112 Color	44 LCC	ZR32112-PLC
ZR32112 Monochrome	44 LCC	ZR32112-MLC

Features

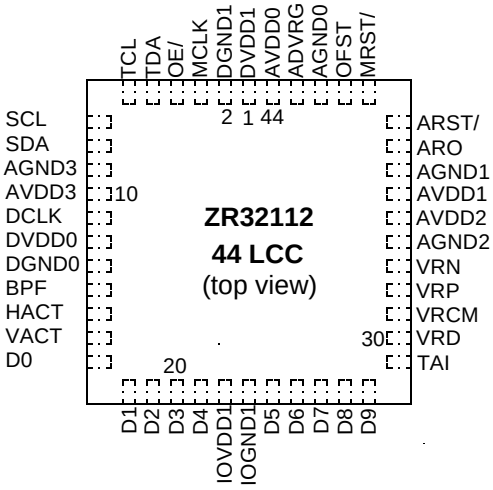
- No Dark Frame Subtraction Required
- Still Frame and Video Modes
- Analog Color Balance PGA
- Programmable Exposure Control
- Movable & Sizable Output Window
- Mirrored and Flipped Scan Modes
- Decimation by 2 or 4 Subsampling
- Optically Black Reference Pixels
- I^2C Control Interface
- Single Voltage Power Supply
- Internally Generated Reference Voltages

Key Specifications

Active Resolution	1288 x 1032
Array Diagonal	12.3mm
Pixel Pitch	7.5um x 7.5um
Color Filter Array	RGB Bayer
Scanning Mode	Progressive
Maximum Pixel Rate	16MHz
Full Frame Rate	9.3 fps (1280x1024)
Decimate by 2 Frame Rate	32.4 fps (640x480)
Decimate by 4 Frame Rate	102 fps (322x258)
Dynamic Range	66dB
R, G and B PGA Gain	0 to 14dB
ADC Resolution	10 bits
Supply Voltage	3.3V
Power Dissipation	260mW



Pin Descriptions



NAME	PIN	TYPE	DESCRIPTION
Supply Signals			
AVDD0, AVDD1, AVDD2, AVDD3	44, 36, 35, 10	IN	Analog Supply Pins.
AGND0, AGND1, AGND2, AGND3	42, 37, 34, 9	OUT	Analog Ground Pins.
DVDD0, DVDD1	12, 1	IN	Digital Supply Pin.
DGND0, DGND1	13, 2	OUT	Digital Ground Pin.
IOVDD0	22	IN	Digital I/O Supply Pins.
IOGND0	23	OUT	Digital I/O Ground Pins.
Output Pixel Data Signals			
D0, D1, ..., D9	17, 18-21, 24-28	OUT	Pixel Output Data Bits 0 (LSB), to 9 (MSB).
Timing and Control Signals			
MCLK	3	IN	Master Clock. Clocks all of the ZR32112's internal state machines.
MRST/	40	IN	Master Reset. Active low device reset. Must be driven low for at least two MCLK periods after powerup.
ARO	38	IN	Array Read Out. Begins readout of pixel values in Still Frame mode. Should be held low in Video Mode.
ARST/	39	IN	Array Reset. Stops the current frame readout, automatically switches the ZR32112 into Still Frame Mode, resets pixel values, and starts integration for a new frame. Should be held high in Video Mode.
OE/	4	IN	Pixel Data Output Enable. 0=enabled; 1=tri-stated
DCLK	11	OUT	Data Output Clock. Same Frequency as MCLK, with internal signal delays matched to D0-D9, BPF, HACT, and VACT.
BPF	14	OUT	Black Pixel Flag. Asserted when output is an optically black pixel.
HACT	15	OUT	Horizontal Active. High during active pixel output.
VACT	16	OUT	Vertical Active. High during image frame output.
Configuration Register I^2C Signals			
SCL	7	IN	I^2C Serial Clock. SCL maximum frequency is $f_{MCLK}/4$.
SDA	8	IN/OUT	I^2C Serial Data. (open collector, bi-directional)
OFST	41	IN	I^2C Base Address Offset. 0=I^2C base address is 60h; 1=I^2C base address is 62h.
Analog Reference Signals			
VRP	32	OUT	Voltage Reference Positive. Bypass to AVDD with a 0.1uF.
VRN	33	OUT	Voltage Reference Negative. Bypass to VRP with 0.1uF.
VRCM	31	OUT	Voltage Reference Common Mode. Bypass to AGND with 0.1uF.
ADVRG	43	IN	Reset Ground Reference. Normally connected to AGND.
VRD	30	IN	Pixel Reset Voltage Reference. Normally connected to AVDD.
Production Test Signals and N.C. Pins			
TDA	5	IN	Test Serial Data Input Signal. Connect to Ground.
TCL	6	IN	Test Serial Data Clock Signal. Connect to Ground.
TAI	29	IN	Analog Input Test Signal. Connect to AGND.

Electrical Characteristics

Absolute Maximum Ratings

VDD Supply Voltage	-0.3V to 7.0V
DC Voltage at any input pin	-0.3V to VDD+0.3V
DC Current at any input pin	-10mA to +10mA
Storage Temperature	-40C to +125C
Max Solder Temperature (less than 10 minutes)	230C

Recommended Operating Conditions

VDD Supply Voltage	3.0V to 3.6V
Temperature	0C to 70C

Note: VDD represents any supply voltage (AVDD, DVDD, or IOVDD). Voltages are relative to GND (AGND, DGND, or IOGND, respectively.)

Pixel Array Characteristics. Room Temp. VDD=3.3V, f_{MCLK}=16MHz unless stated otherwise.

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Total Resolution	Total array size including black pixels			1304 x 1032		pxls x pxls
Active Resolution	Total R, G and B pixels			1288 x 1032		pxls x pxls
Black Pixels	Black, Optically Shielded Pixels.	Optically Shielded on the ZR32112-PLC (color) Unshielded on the ZR32112-MLC (mono)		16		pxls / line
Pixel Pitch	Sensor Element Area			7.5 x 7.5		µm x µm
FF-M	Fill Factor for the ZR32112-MLC			51		%
FF-C	Fill Factor for the ZR32112-PLC			63		%
DRK	Mean Dark Signal Accumulation	Dark Condition[1], Full Frame Exposure[2], Includes Offset.		38	80	codes
SENS-M	ZR32112-MLC Monochrome Sensitivity	Noise based ISO-Sensitivity (ISO 12232: 1998(E))		TBD		ISO
SENS-C	ZR32112-PLC Color Sensitivity	Noise based ISO-Sensitivity (ISO 12232: 1998(E))		TBD		ISO
SAT	Saturation Level			1023		codes
Noise	Temporal Noise			0.40	TBD	codes
Single Pixel Dynamic Range	Ratio of pixel saturation level to temporal noise.			66		dB

1. A mechanical shutter is closed so there is no illumination on the sensor array.
2. Video mode, with a full frame exposure (i.e. Reg 12h = 03h, Reg 13h = FFh), 107ms with a 16MHz MCLK.

Analog Front End Performance Characteristics. Room Temp. VDD=3.3V, f_{MCLK}=16MHz unless stated otherwise.

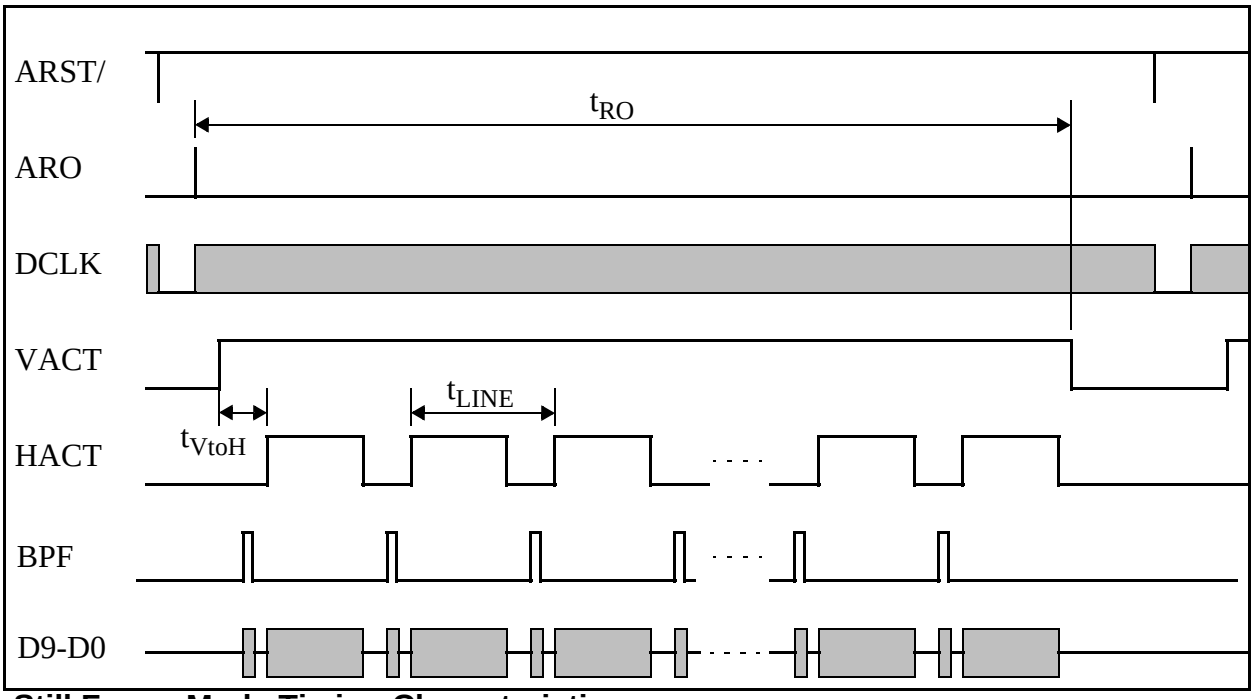
SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
VRCM	Common mode reference output voltage			AVDD2 /2		V
VRP	Positive reference output voltage			VRCM + 0.5		V
VRN	Negative reference output voltage			VRCM - 0.5		V
PGA_{RES}	PGA Control Resolution			6		Bits
A_{PGAmin}	Minimum PGA gain	Minimum Gain[1]		1		V/V
A_{PGAmax}	Maximum PGA gain	Maximum Gain[2]		5		V/V
A_{PGAERR}	PGA gain error	maximum error at any gain		0.5		%
ADC Resolution	ADC Resolution with no missing codes			10		bits
ADC input range	ADC full scale voltage: VRP - VRN.			1		V
ADC DNL	ADC worst case differential non-linearity			+0.85 -0.85		LSB
ADC INL	ADC worst case integral non-linearity			+TBD -TBD		LSB
Min Gain Offset Error	Analog positive signal offset with min gain.	Dark Condition[3], Short Exposure[4], Minimum Gain	12	20	28	codes
Max Gain Offset Error	Analog positive signal offset with max gain.	Dark Condition, Short Exposure, Maximum Gain	26.5	38.5	50.5	codes

1. PGA gain of 1V/V. Reg 14h = Reg 15h = Reg 16h = 00h.
2. PGA gain of 5V/V. Reg 14h = Reg 15h = Reg 16h = 3Fh.
3. A mechanical shutter is closed so there is no illumination on the sensor array.
4. Video mode, with two lines of exposure (i.e. Reg 12h = 03h, Reg 13h = FAh)

DC Electrical Characteristics. Room Temp. VDD=3.3V, f_{MCLK}=16MHz unless stated otherwise.

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
IA	Analog supply current			70	75	mA
ID	Digital supply current			5	7.5	mA
IA_{PD}	Power down analog supply current			12	16.8	mA
ID_{PD}	Power down digital supply current			3.7	5.7	mA
VIH	Input high voltage		0.98	1.1		V
VIL	Input low voltage			2.2	2.32	V
IL	Input leakage current			0.1		µA
C_{IN}	Input capacitance			5		pF
VOH	Output high voltage	IL = TBD	TBD			V
VOL	Output low voltage	IL = TBD			TBD	V

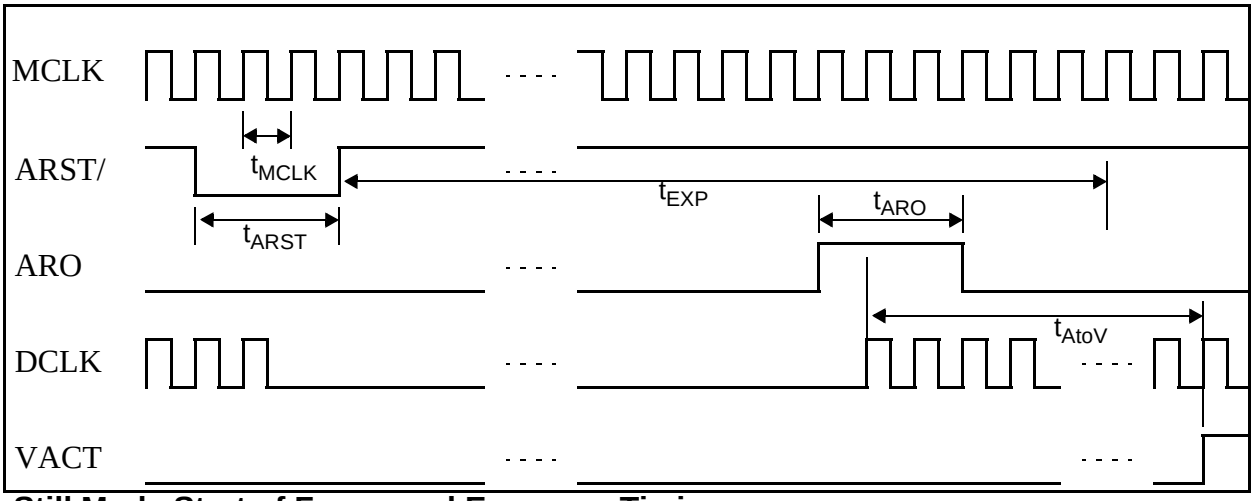
AC Timing Characteristics



Still Frame Mode Timing Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{LINE}	Line Time	Decimation Disabled Decimate by 2 mode Decimate by 4 mode		1664 960 608		t_{MCLK}
t_{RO}	Read Out Time			LINES + 2		t_{LINE}
LINES	Number of Lines in Frame	Decimation Disabled Decimate by 2 mode Decimate by 4 mode		8 4 2		Height[1]
Height	Height of output window (value in register 09h)		0		129	
t_{RO}	Read Out Time	Full Frame (1288x1032) Full Frame - Dec by 2 Full Frame - Dec by 4		80.9 23.4 7.45		ms
t_{VtoH}	VACT rising edge to first HACT rising edge			1		t_{LINE}

1. The number of lines per frame (LINES) is equal to 2, 4, or 8 times the Height value in register 09h, depending on the Decimation mode.



Still Mode Start of Frame and Exposure Timing

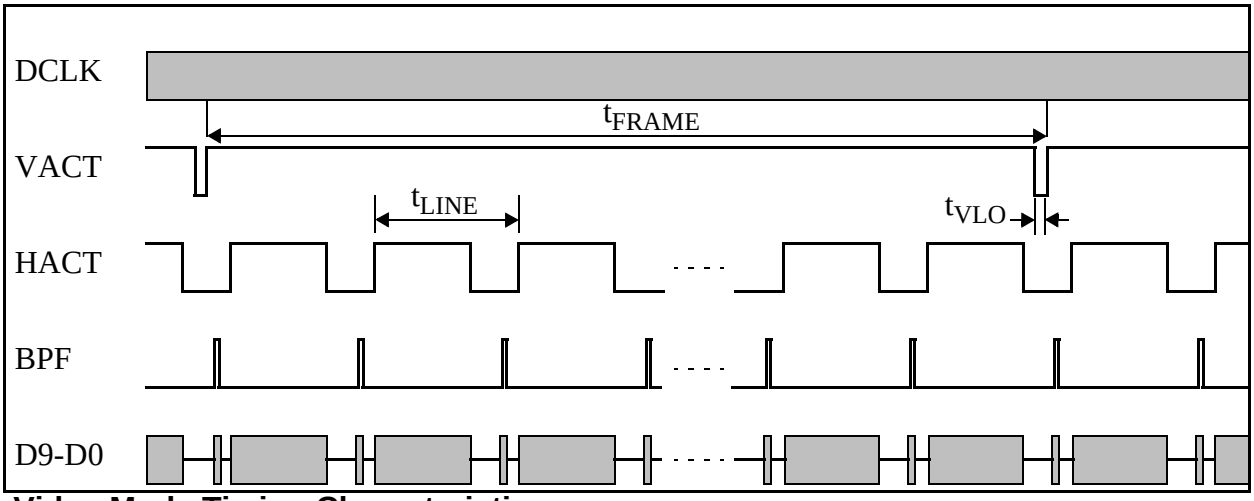
SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{MCLK}	MCLK period		62.5		1000	ns
t_{ARST}	ARST/ Pulse Width		2	8		t_{MCLK}
t_{ARO}	ARO Pulse Width		2			t_{MCLK}
t_{EXP}[1]	Exposure Time	Delay from ARST/ to ARO determines the exposure time.				
t_{AtoV}	ARO latched by MCLK to VACT rising edge			240		t_{MCLK}

1. In Still mode, exposure on all lines begins on the rising edge of ARST/. t_{EXP} is the exposure time of the first line. t_{EXP} ends 112 MCLK periods after ARO is latched by MCLK. For all lines to have an equal exposure, a mechanical shutter should be closed, or the source illumination should be turned off before the end of t_{EXP}, and remain so until the end of the frame readout. Note that 112 MCLK periods is insignificant compared to all but the shortest exposure times, and therefore the ARO pulse can typically be considered the end of the exposure time.

Shutter Timing

In still mode, the ZR32112 image array is sensitive to light during frame readout. The array must not be exposed to light during readout to avoid uneven exposure. The first line of the frame is sampled 112 MCLK periods after ARO goes high. Therefore, if a mechanical shutter is being used, it should be completely closed no later than 112 MCLK periods after ARO goes high.

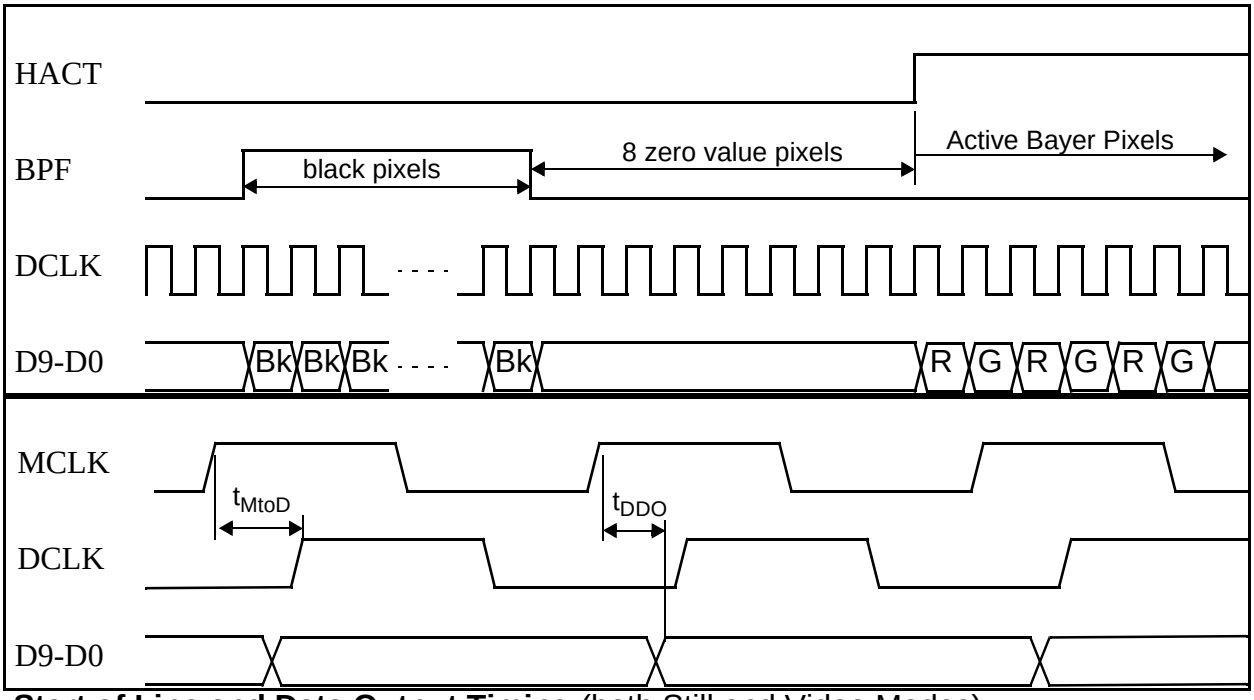
Most mechanical shutters take several milliseconds to completely close. The system's timing must be designed to accommodate the shutter close time before ARO is pulsed. In some cases, especially in bright light conditions with short exposure times, the shutter timing should be designed to begin closing even before the start of integration (i.e. before the ARST/ low pulse).



Video Mode Timing Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{LINE}	Line Time	Decimation Disabled Decimate by 2 mode Decimate by 4 mode		1664 960 608		t_{MCLK}
t_{FRAME}	Frame to Frame period			LINES		t_{LINE}
LINES	Number of Lines per Frame	Decimation Disabled Decimate by 2 mode Decimate by 4 mode		8 4 2		Height[1]
Height	Height of Output Window (value in register 09h)		1		129	
t_{VLO}	VACT Low Time between Frames			1		t_{MCLK}
t_{FRAME}	Frame to Frame period	Full Frame (1288x1032) Full Frame - Dec by 2 Full Frame - Dec by 4		107 30.9 9.8		ms

1. The number of lines per frame (LINES) is equal to 2, 4, or 8 times the Height value in register 09h, depending on the Decimation mode.



Start of Line and Data Output Timing (both Still and Video Modes)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
BLK[1]	Number of Shielded, Optically Black Pixels	Decimation Disabled Decimate by 2 mode Decimate by 4 mode		16 8 4		Pixels
t_{MtoD}[2]	MCLK to DCLK delay			14		ns
t_{DDO}	MCLK to Data Output delay			10		ns
t_{MCLK}	MCLK period		62.5		1000	ns

1. On every row of the array, eight optically black reference pixels are physically located immediately to the left of the active pixels, and eight are located immediately to the right. Before the active pixels of each row are read out, the left side black pixels are read out followed the right side black pixels. Either 2, 4, or 8 of the left side and 2, 4 or 8 of the right side black pixels are read out, depending on the decimation mode. The BPF signal is asserted by the ZR32112 during black pixel readout.
2. DCLK is shown as active high (i.e. register 02, bit 0 = 0) in the diagram above. If DCLK is active low (i.e. register 02, bit 0 = 1), there is a delay of t_{MtoD} from the rising edge of MCLK to the *falling* edge of DCLK.

Register Descriptions

The ZR32112's control registers are accessed via an I^2C interface. The ZR32112's I^2C slave address is 60h if the OFST signal is pulled low and 62h if OFST is pulled high. The maximum I2C clock frequency, f_{SCL}, is one fourth of the applied MCLK frequency ($f_{MCLK}/4$).

A ZR32112 I^2C register write consists of a seven bit Part ID plus write bit (60h or 62h), an eight bit register address, then an eight bit data value. Each successive byte after a data value on the I^2C bus, without a stop condition, will cause the ZR32112 to automatically increment the register address by one and will be read from or written to the next higher address location.

A ZR32112 I^2C register read consists of a seven bit Part ID plus write bit (60h or 62h), and an eight bit register address followed by a stop condition. Then a seven bit Part ID plus read bit (61h or 63h). The next byte clocked out of the ZR32112 will be the value stored in the register previously addressed.

ADDRESS (Hex)	REGISTER DESCRIPTION	DEFAULT (Hex)
Part ID and Mode Registers		
00	Part Identification Number (read only)	30
01	Functional Modes	30
02	Signal Polarity and Data Format Modes	03
03	Register Update Mode	03
Output Window Size and Location Registers		
04	Start of Output Window Column Number (high byte)	00
05	Start of Output Window Column Number (low byte)	00
06	Start of Output Window Row Number (high byte)	00
07	Start of Output Window Row Number (low byte)	00
08	Width (number of columns) of Output Window	A1
09	Height (number of rows) of Output Window	81
Exposure Time and Gain Control Registers		
12	Video Mode Exposure Time (MSBs)	07
13	Video Mode Exposure Time (LSBs)	FF
14	Red Channel PGA gain	00
15	Green Channel PGA gain	00
16	Blue Channel PGA Gain	00

Address 00h - Part Identification Number (read only)

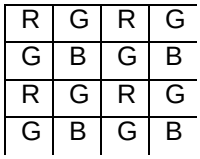
BIT(s)	FUNCTION	DESCRIPTION
7-0	Part ID	Production Version = 30h

Address 01h - Functional Modes Register

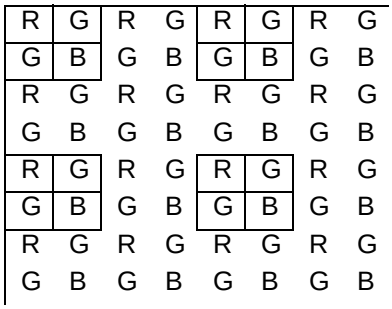
BIT(s)	FUNCTION	DESCRIPTION
7	Ramp Out	0=Normal Imaging Mode Output 1=Digitally Generated Test Ramp Output (each pixel's value is equal to the 10 LSBs of its column number)
6	Reserved	
5	Red Pixel Registration	0=Force Output to Start With Red Pixel (by automatically incrementing the start of row and column number if necessary) 1=Start Output With Any Color Pixel
4	Horizontal Direction	0=Output Columns Left to Right 1=Output Columns Right to Left
3	Vertical Direction	0=Output Rows Top to Bottom 1= Output Rows Bottom to Top
2	Decimation Size	0=Decimate by 2 - Output One Column/Row Pair, then Skip One Column/Row Pair 1=Decimate by 4 - Output One Column/Row Pair, then Skip Three Col-umn/Row Pairs
1	Decimation Enable	0=Decimation Disabled - Output Every Pixel 1=Decimation Enabled - Output Only One of Two or One of Four Column/Row Pairs
0	Mode	0=Still Frame Mode 1=Video Mode

Red Pixel Registration automatically changes the first row and/or column read out from the array if the currently programmed readout direction (bits 4 and 5 of register 01) is not set such that the first pixel readout is red. It is important to note that the red pixel registration setting will not change the output window width or height (registers 08 and 09). Care should be taken that resultant readout window does not extend beyond the limits of the physical array.

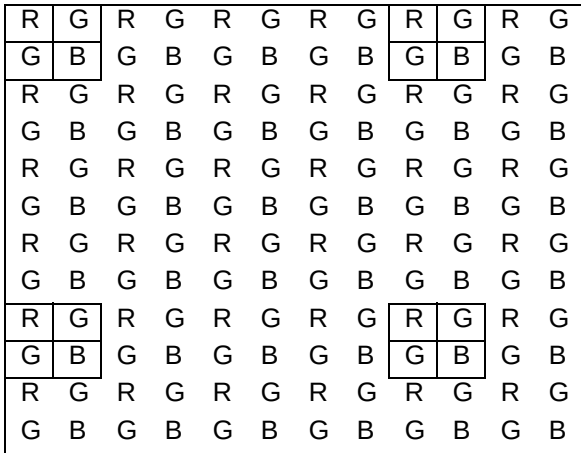
Decimation Disabled



Decimate by 2



Decimate by 4



Still Frame Mode is used to capture a single, simultaneously exposed frame. When programmed in still frame mode, the ZR32112 waits for the assertion of the array reset signal, ARST/, to begin a frame. As soon as ARST/ is returned to its inactive state, the integration of light begins across the entire active array. The data output clock, DCLK, stops and the ZR32112 waits for the assertion of the array read out signal, ARO. Once ARO is asserted, DCLK starts up and after 240 MCLK cycles VACT is asserted by the ZR32112 and the frame read out begins.

Video Mode is used to capture multiple frames with a programmable exposure time. Video mode uses an electronic rolling shutter and continuously outputs data frames. Each line, or row, of sensor elements is exposed for the programmed exposure time (registers 12h and 13h) before it is read out from the array.

Address 02h - Signal Polarity and Data Format Register

BIT(s)	FUNCTION	DESCRIPTION
7	OE Control	0=D9-D0 Outputs Enabled by OE/ signal 1=Outpus Enabled by Bit 6
6	Output Enable	0=D9-D0 Outputs Disabled 1=Outputs Enabled
5	Reserved	Set to zero for normal operation.
4	Reserved	Set to zero for normal operation.
3	VACT Polarity	0=VACT is Active High 1=VACT is Active Low
2	HACT Polarity	0=HACT is Active High 1=HACT is Active Low
1	Data Format	0=Inverted MSB - output codes range from 1000000001b for dark up to 0111111111b at full exposure. 1=Unipolar Image Data - output codes range from 0000000001b for dark up to 1111111111b at full exposure.
0	DCLK Polarity	0=DCLK is Active High 1=DCLK is Active Low

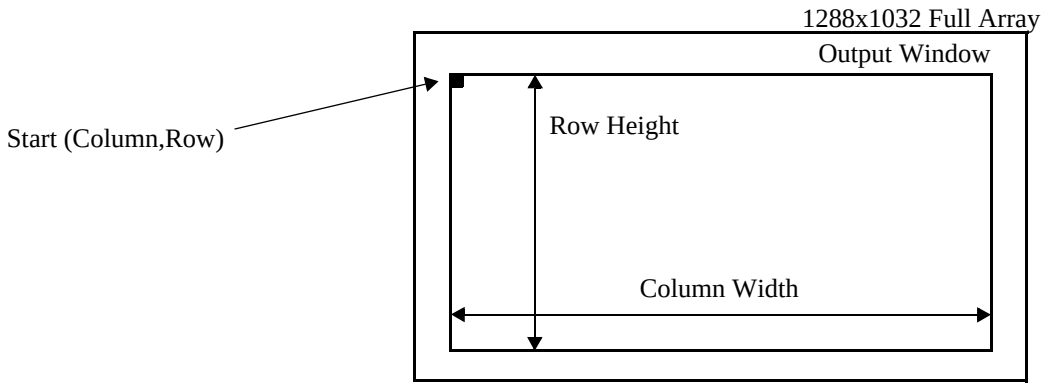
Address 03h - Register Update Mode

BIT(s)	FUNCTION	DESCRIPTION
7-2	Don't Care	
1,0	Update Mode	X0=I^2C writes to Registers 04h to 16h will not take effect until this register is changed. 01=I^2C writes to Registers 04h to 16h will take effect at the end of the current video frame (when VACT goes low). 11=I^2C writes to Registers 04h to 16h will take effect immediately.

Addresses 04h to 09h - Output Window Size and Location

Programming the Output Window size and location registers establishes a rectangular area, or sub-frame, of pixels within the entire active array that will be output on data pins D9-D0.

ADDR	BIT(s)	FUNCTION	DESCRIPTION
04	7-0	Start Column	Start Of Output Window Column Number (High Byte)
05	7-0	Start Column	Start Of Output Window Column Number (Low Byte)
06	7-0	Start Row	Start Of Output Window Row Number (High Byte)
07	7-0	Start Row	Start Of Output Window Row Number (Low Byte)
08	7-0	Width	Column Width of the Output Window. The number of columns in the Output Window will be 8, 4, or 2 times the value in this register depending on whether the Decimation mode disabled, decimated by 2 or decimated by 4, respectively.
09	7-0	Height	The Row Height of the Output Window. The number of rows (or lines) in the Output Window will be 8, 4, or 2 times the value in this register depending on whether the decimation mode disabled, decimated by 2 or decimated by 4, respectively.



Writing the Default Register Values

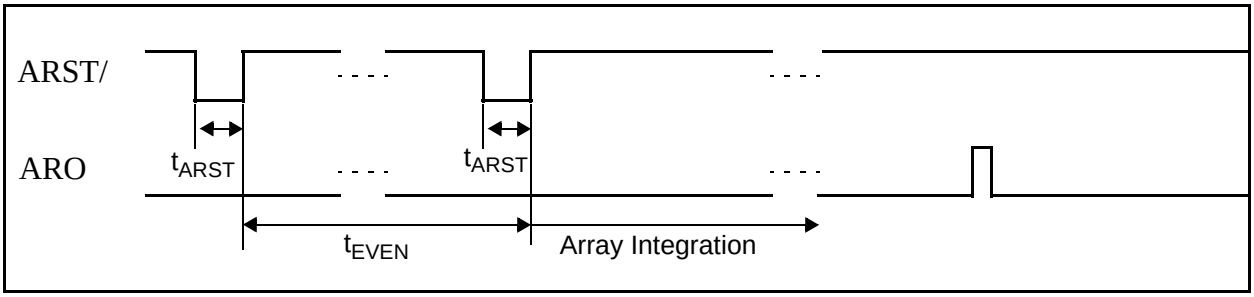
After Powering up the ZR32112, the master reset signal, MRST/, must be driven low for at least 2 MCLK periods and returned high. After resetting the ZR32112, write appropriate values to *all* registers. The recommended default values are listed in the table below. The registers with addresses greater than 16h are write only and are used primarily for PixelCam production testing. PixelCam recommends that only the default values be written to these registers.

Note: All values listed below are in hexadecimal.

Address	Default	Address	Default	Address	Default	Address	Default
User Registers (read/write) – should be written to values appropriate for the application							
1	30	2	3	3	3	4	0
5	0	6	0	7	0	8	A1
9	81	12	4	13	FE	14	0
15	0	16	0				
Test Registers (write only) – must be written to default values							
20	80	21	0	22	0		
80	1	81	0	82	A	83	C
86	2	87	1F	88	1	89	7
8A	1F	8B	C	8C	3	8D	1F
8E	8	8F	1F	90	A	91	11
92	8	93	1F	94	6	95	A
96	1F	97	1	98	F	99	0
9A	1F	9B	2	9C	F	9F	7
A0	1F	A1	1	A2	A	A3	F
A4	17	A5	0	A6	1F	A7	F
A8	A	A9	F	AA	17	AB	2
AC	1F	AD	7	AE	0	AF	3
B0	17	B3	C	B4	1F	B5	0
B6	0	B7	0	B8	0	B9	0
BA	0	BB	0	BC	1		

Still Mode Timing for Best Performance

When switching from one mode to another (e.g. decimated by two to decimation disabled) before capturing a still mode frame, the lines in the array may have been previously exposed to very different lighting conditions. To evenly reset and expose all lines in the array for a still frame capture, a double pulse on ARST/, as shown below, may be used. If different lines were exposed very unevenly in the previous frame, and double pulsing on ARST/ is not used, individual lines may have responses that vary by as much as 20mV (~20 10 bit LSBs).



SYMBOL	DESCRIPTION	Value for Best Performance
t_{ARST}	ARST/ low pulse width	8 MCLK periods
t_{EVEN}	Delay time from first ARST/ pulse to second ARST/ pulse to guarantee even array reset and exposure	>15 ms

Addresses 12h (coarse) and 13h (fine) - Video Mode Exposure Time

ADDR	BIT(s)	FUNCTION	DESCRIPTION
12	7-3	Don't Care	
12	2-0	Exposure	Exposure Time In Video Mode (MSBs)
13	7-0	Exposure	Exposure Time In Video Mode (LSBs)

The **Exposure Time** setting controls the integration time for the sensor elements of each row, or line, in video mode. The sensor elements of each line integrate light for a programmable number of line times (t_{LINE}) before their values are read out from the array. The integration, or exposure time can be programmed to be from one line time up to the total number of lines per frame (LINES). The exposure time is maximized and equal to the frame time when the 11 bit exposure value in registers 12h and 13h is 7FFh. The exposure time is equal to:

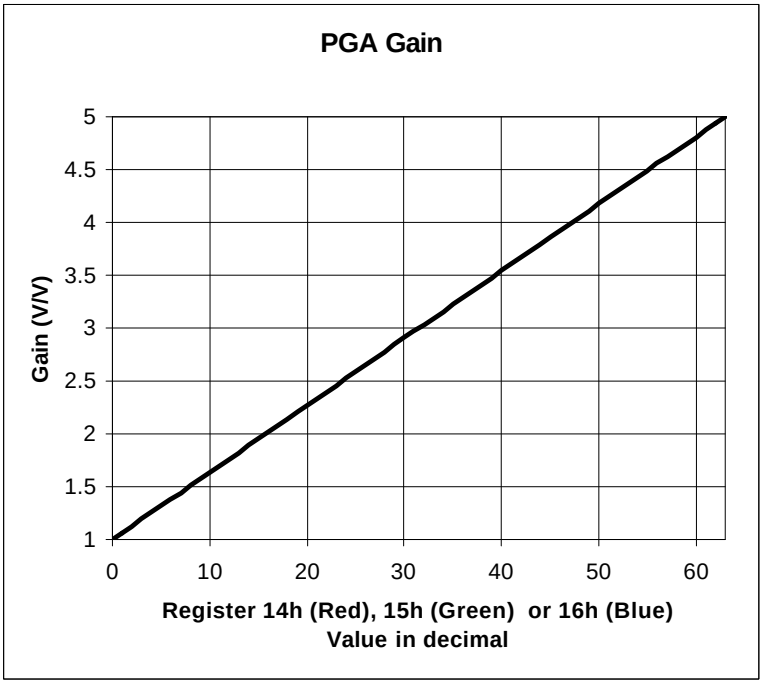
$$t_{EXP} = (EXP \cdot EXP_{min}) * t_{LINE}$$

where EXP is the 11 bit value in registers 12h and 13h and EXP_{min} is the minimum EXP value that will result in zero lines of exposure time. (EXP_{min} = 7FF - LINES)

*For the definition of t_{LINE} and LINES, see the **Video Mode Timing Characteristics** table on page 7.*

Addresses 14h, 15h and 16h - Red, Green and Blue PGA Gain Settings

BIT(s)	FUNCTION	DESCRIPTION
7-6	Don't Care	
5-0	Analog Gain	Analog Gain Linearly Adjusted From 1V/V (0dB) at 00h To 5V/V (14dB) at 3Fh. The analog gain is: 1 + 63/4 * bits[5-0] V/V.



Physical Dimensions