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Design of Prototype Scientific CMOS Image Sensors

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ABSTRACT

We present the design and test results of a prototype 4T CMOS image sensor fabricated in 0.18-µm technology featuring 20 different 6.5 µm pixel pitch designs. We review the measured data which clearly show the impact of the pixel topologies on sensor performance parameters such as conversion gain, read noise, dark current, full well capacity, non-linearity, PRNU, DSNU, image lag, QE and MTF. Read noise of less than 1.5e- rms and peak QE greater than 70%, with microlens, are reported.

Keywords: Scientific CMOS image sensors, high-speed imager, low readout noise, 4T pixel design

1. INTRODUCTION

Major technical advances have been reported recently in CMOS image sensor technology including the development of advanced digital/analog circuit designs and improvements in device fabrication technologies. Imager performance parameters such as sensitivity, noise, speed and power have shown substantial improvements [1][2][3]. However, many commercially available products do not meet the demanding requirements of advanced scientific applications in terms of noise, speed, and power.

As part of our internal product development process for a new scientific-grade CMOS image sensor which is intended to address the performance limitations outlined above, Fairchild Imaging is performing an extensive, multi-phase investigation on the impact of circuit architecture and pixel topology on key sensor performance parameters such as read noise, dark current, image lag, full well capacity, quantum efficiency (QE), and modulation transfer function (MTF). Our goals are to debug and optimize critical elements of the design on prototype devices, demonstrate the desired performance, and validate the product sensor specifications.

We focus on a 0.18-µm 4T CMOS image sensor (CIS) process technology which supports dual voltage operation: 1.8V for the high-speed digital logic circuitry and 3.3V for the analog components. The basic 4T pixel architecture consists of a pinned photodiode, a reset transistor, a transfer gate to move charge from the photodiode to the floating diffusion sense node, a source follower transistor, and a row select transistor.

In the first phase of the project, our goals were to evaluate various pixel design parameters, determine how they influence the imaging properties of the sensor, and develop low noise high speed column parallel readout circuitry with integrated correlated double sampling (CDS). The prototype sensor included 36 different pixel designs with variations intended to optimize full well capacity, read noise, dark current, lag and MTF.

In the second phase, the key design goals included further performance optimization of the pixel and the low noise column parallel amplifier design. Then in the third phase of the project, the best performing pixel designs will be implemented in an area array format and integrated with low noise 12-bit column parallel analog-to-digital converters. The completed sensor will provide complete digital input control and digital pixel data. Our primary design goals are to demonstrate a sensor design which will satisfy the requirements for sensitivity, noise and speed in advanced scientific applications.

To date, we have completed the first two phases of the project, and the results of the first phase were reported last year [4]. In the first prototype sensor, we measured read noise as low as 1.9 e^- rms at 30 Mpixels/sec and a dark current density less than 11 pA/cm^2 at 30ºC. The measured full well capacity was 1.4 ke^- in high gain mode and 30 ke^- in low

gain mode, respectively. In this paper, we present the results of the second phase of the project. We review the architecture of the prototype sensor, the pixel design considerations, then present the characterization test results. Finally, we discuss our current work in-progress.

2. IMAGE SENSOR DESIGN

2.1. Device Architecture

The prototype sensor, shown in Figure 1, contains 20 different pixel designs arranged in blocks of 16 columns by 240 rows for a total imaging array of 320(H) x 240(V). All of the pixels share a common x-y pitch of 6.5 µm. The overall die dimensions are 5 mm x 5 mm.

The sensor features a split readout scheme in which the odd columns are read out on the top, and the even columns are read out on the bottom of the array. This arrangement provides a column amplifier pitch of 13 µm, which alleviates the constraints on the layout of the column level amplifiers. The column level amplifier features two gain stages: low gain (23 µV/e^-) and high gain (700 µV/e^-). The amplifier gain is controlled externally. The maximum total output data rate of the sensor is 30 Mpixels/sec per output port.

Separate power supplies are used for the pixel core, analog output amplifier, pad ring, and digital shift registers. A common ground is used for the entire chip.

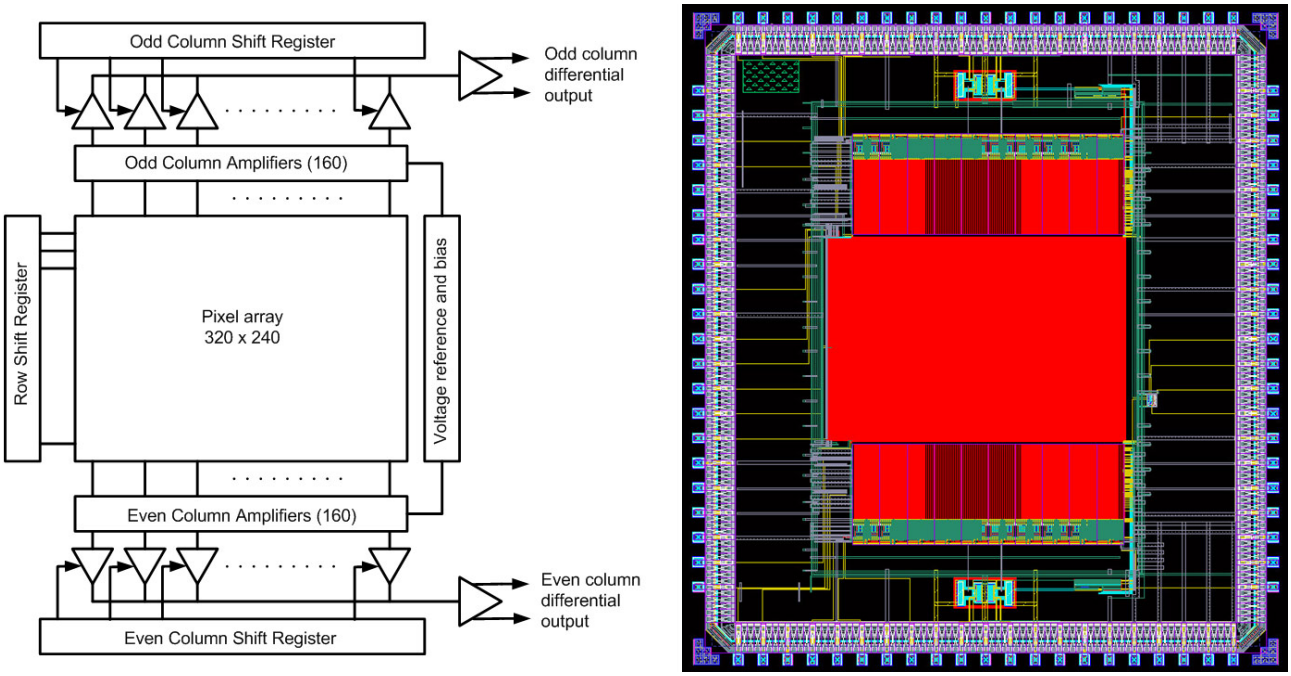

Figure 1. Prototype sensor architecture and chip layout

2.2. Device Operation

The sensor is designed to operate in rolling shutter mode [5]. The readout timing diagram is shown in Figure 2, an uncorrected video frame capture image is shown in Figure 3, and the analog readout chain is schematically illustrated in Figure 4. The row shift register selects one row of pixels at a time. The row period is typically 64 µs, and during this time, the sense node in the selected pixel is reset via PIX_RESET, the reset voltage is sampled, via S1_IN, and stored, then the transfer gate is turned on, via PIX_TX, to transfer the accumulated charge in the pinned photodiode to the floating diffusion sense node. The resulting signal voltage is then sampled, via S2_IN, and stored. The sampled reset and signal voltages are multiplexed and read out pseudo differential for kT/C noise cancellation with CDS. Moreover, the reset and signal voltages stored on capacitors in the column level amplifiers, are scanned out by the column shift

register to the differential analog output ports. The row shift register then selects the next row and the readout sequence is repeated. The integration time of the sensor is determined by the period of PIX_TX.

The signals involved in the pixel readout function include the row shift register clock, ROW_CLK, the digital input for the row shift register, ROW_IN, the pixel reset signal, PIX_RESET, the pixel transfer gate, PIX_TX, the column level amplifier reset signal, CA_RESET, the pixel reset voltage sample signal, S1_IN, the pixel signal voltage sample signal, S2_IN, the column shift register clock, CSR_CLK, and finally the digital input for the column shift register, CSR_IN.

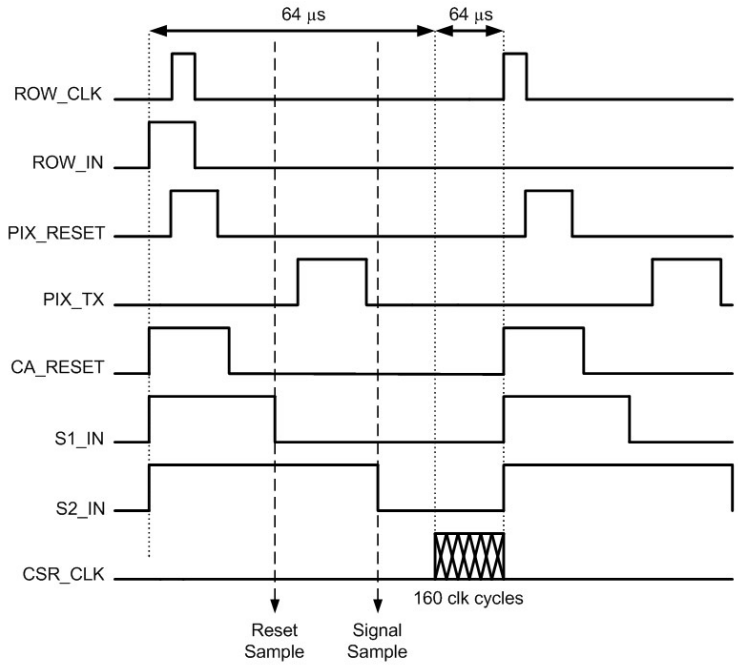

Figure 2. Pixel readout timing diagram (30 frames/sec)

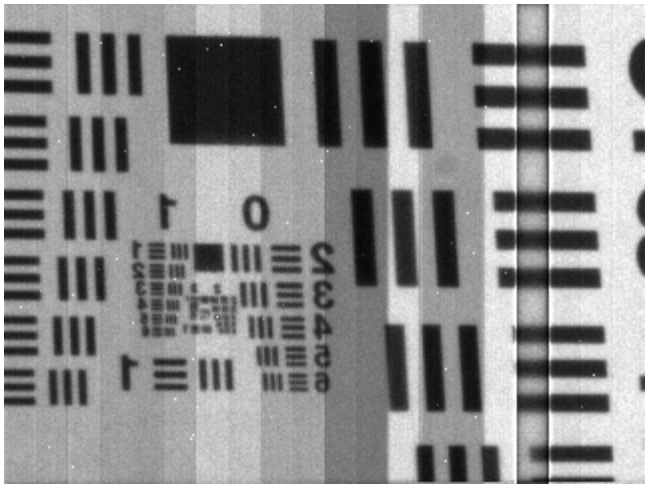

Figure 3. Captured frame from 30 fps video showing the variations in the 20 pixel groups

The column level amplifier architecture is shown in Figure 4. The column level amplifiers feature two gain states: 1X (low gain) and 32X (high gain). The gain of each column amplifier is determined by the ratio of the input capacitor (C1) and the feedback capacitor. The pixel reset voltage is stored on C1, the column amplifier reset voltage is stored on Cs1,

and the final amplifier pixel signal voltage is stored on Cs2. This allows us to remove the kT/C noise from the pixel and from the column level amplifier via dual CDS.

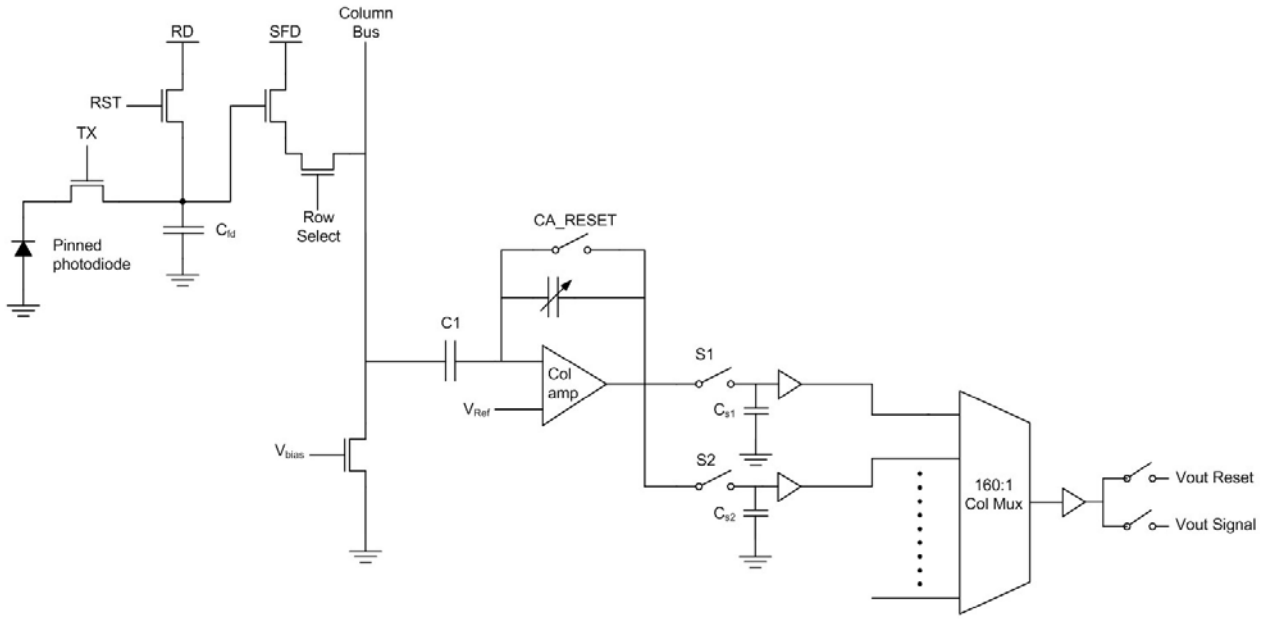

Figure 4. Analog readout signal chain

2.3. Pixel design

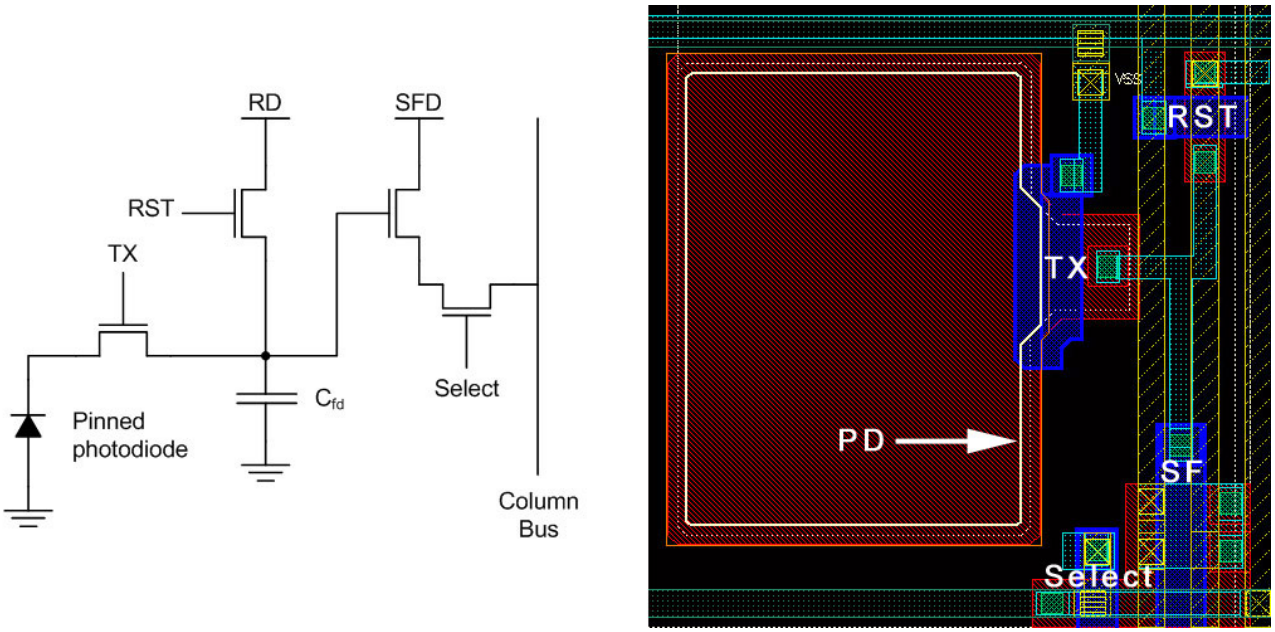

Figure 5. Simplified schematic of a 4T pixel and a sample pixel layout

A simplified schematic of the pixel and a sample pixel layout are shown in Figure 5. We designed 20 different pixel variations to evaluate the impact of the pixel topology on its performance. In a 4T pixel, the complete transfer of signal charge from the pinned photodiode to the floating sense node, is critical to the pixel performance in terms of noise and image lag [6]. The potential profile under the transfer gate must be properly tailored to establish the proper barrier

height between the photodiode and the floating diffusion node to achieve full charge transfer when the transfer gate is high. The relative position and the geometry of the n-type diffusion layer of the pinned photodiode, combined with the shape and size of the transfer gate directly affect key device characteristics such as noise, dark current, and image lag.

A cross-sectional SEM micrograph of a sample pixel design is shown in Figure 6.

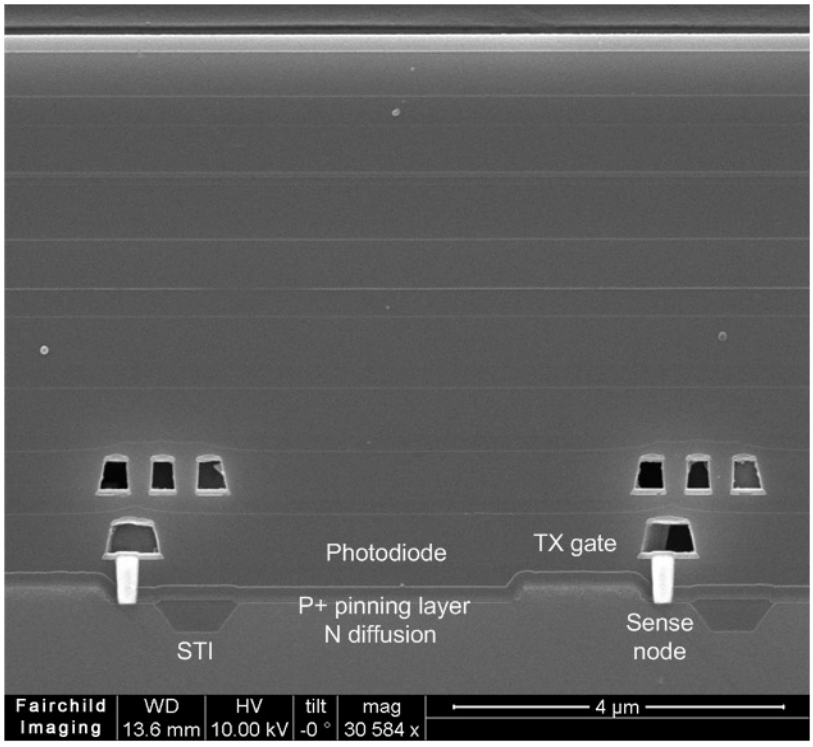

Figure 6. SEM cross-section of Fairchild Imaging 6.5 µm 4T pixel

3. MEASUREMENT RESULTS

3.1. Test methodology

Multiple samples of the prototype sensors were characterized independently in a dedicated test camera using a test methodology which is based on the photon transfer method, and the final reported values are based on the average of the collected data. Each test sample was tested for conversion gain, full well capacity, dark current, response non-linearity, lag and QE. Prior to data analysis, median filtering was performed to remove the hot pixels from the measured data.

1. All of the characterization tests were performed in high gain mode.
2. Multiple dark exposures at different integration times were performed to estimate dark current, dark current non-uniformity (DSNU), and read noise.
3. The photon transfer method was used to estimate conversion gain, full well capacity, non-linearity, photo-response non-uniformity (PRNU).
4. The quantum efficiency of each pixel group was measured, between 400 nm and 800 nm, using a monochromator with a tungsten light source and a calibrated photodiode.
5. Lag measurements were performed using 8 dark frames and 8 light frames with the pixels exposed to a blue LED light source to full saturation.
6. MTF measurements have not been completed for all of the pixel groups, however, preliminary results from the better performing pixel groups indicate that the MTF measured at the Nyquist frequency is better than 0.4 at 550 nm. The implemented MTF test procedures conform with the ISO 12233 test standard.

The final measured results, comparing the performance of each pixel group, are shown next.

3.2. Conversion gain

The slope of the photon transfer curve for each pixel group is shown in Figure 7. The conversion gain in µV/e^- is obtained by dividing the system gain (0.3 mV/DN) by the reciprocal of the slope. The conversion gain of pixel group # 16, for example, with a slope of 2.7 DN/e^- is therefore 810 µV/e^-.

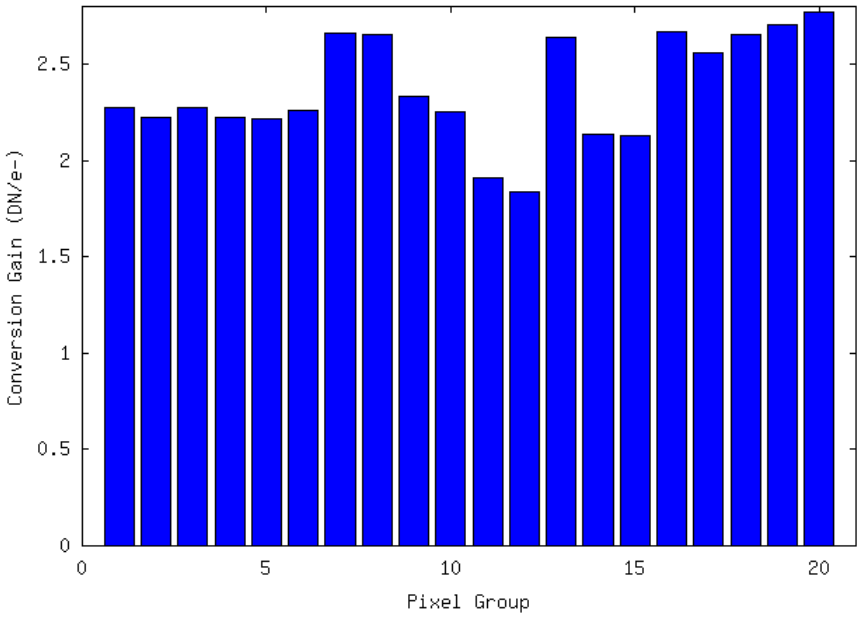

Figure 7. Conversion gain of the different pixel groups

3.3. Read noise

The read noise is measured with correlated double sampling with a line time of 64 µs, for an output rate of 65 frames per second. The read noise for each different pixel group is shown in Figure 8.

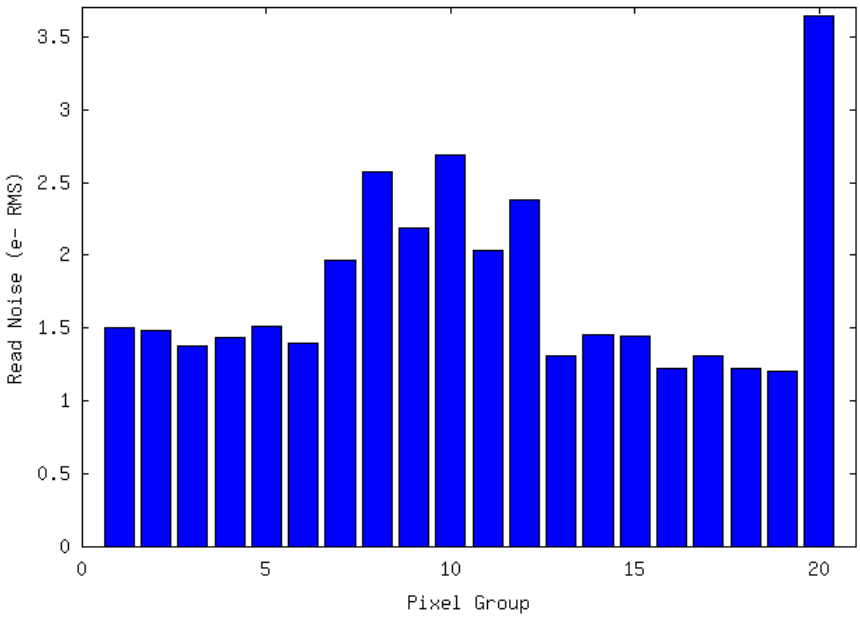

Figure 8. Readout noise of the different pixel groups

3.4. Dark current

Measured at ambient temperature, the dark current in the well-designed pixels, group #16 for example, is about 18 e^- /pixel/sec which is equivalent to a dark current density of 6.8 pA/cm^2. The groups of pixels which exhibit negative dark current figures suffer from excessive lag, resulting in the anomalous results. The data is plotted in Figure 9.

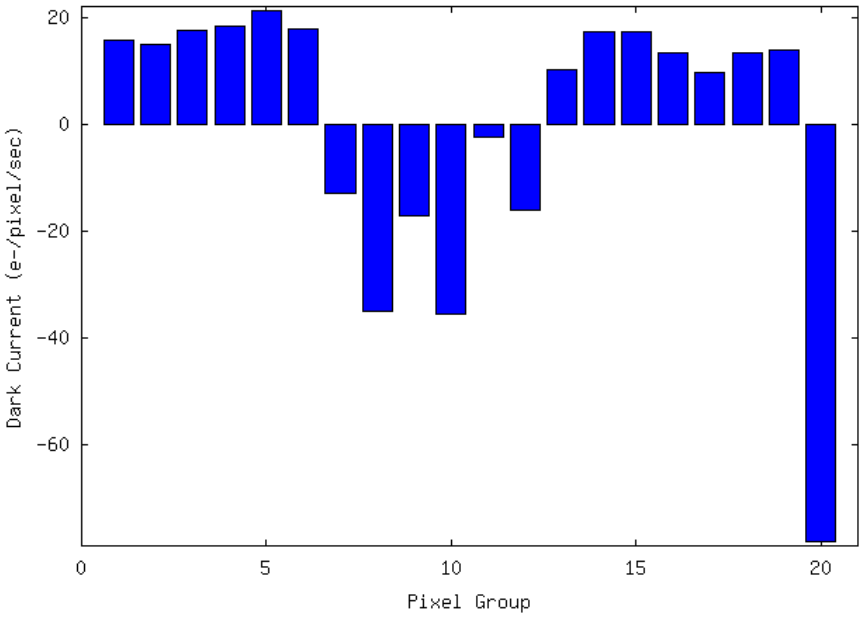

Figure 9. Dark current of the different pixel groups

3.5. Full well capacity

In high gain mode, the full well capacity is between 1100 e^- and 1500 e^-, as shown in Figure 10.

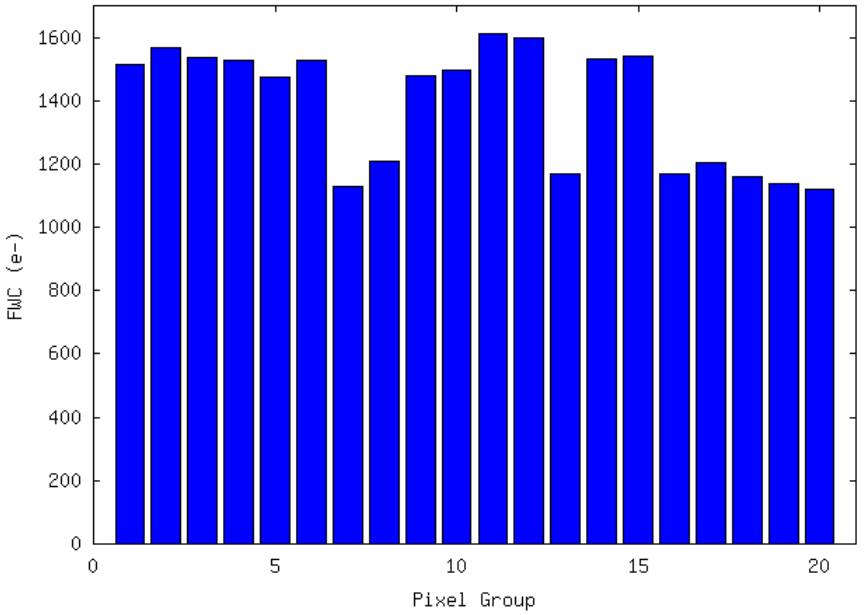

Figure 10. Full well capacity of the different pixel groups

3.6. Image lag

A large image lag results in irregular results in noise, dark current and QE measurements. The design and proper alignments of the implant layers in the photodiode region, the size and geometry of the transfer gate have a large impact on image lag, as illustrated in Figure 11. Pixel groups 7-12 and 20 suffer from excessive lag and are not usable.

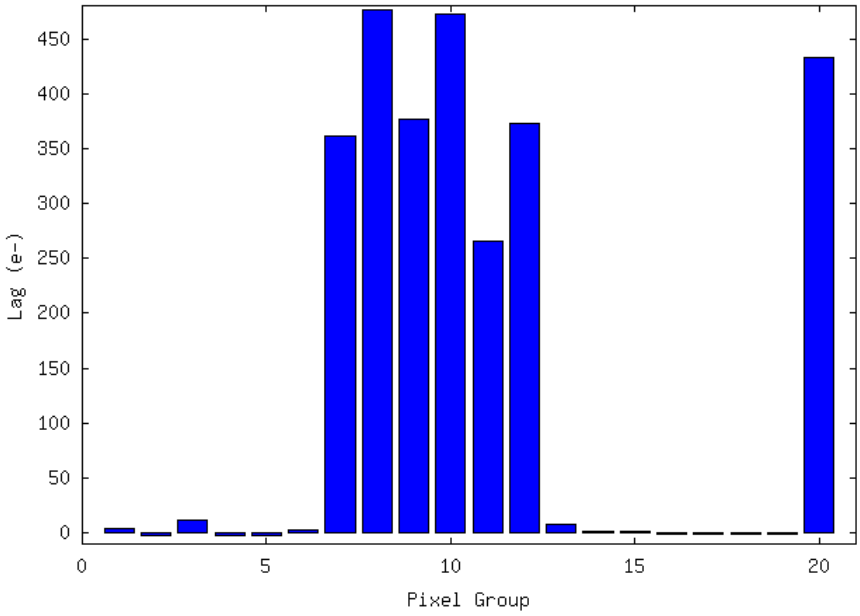

Figure 11. Image lag of the different pixel groups

3.7. Quantum Efficiency

The QE curves, shown in Figure 12, were obtained from devices which featured microlenses. Observed benefits of the microlenses include an increase in the quantum efficiency, as well as smoother QE curves with minimal spectral ripples.

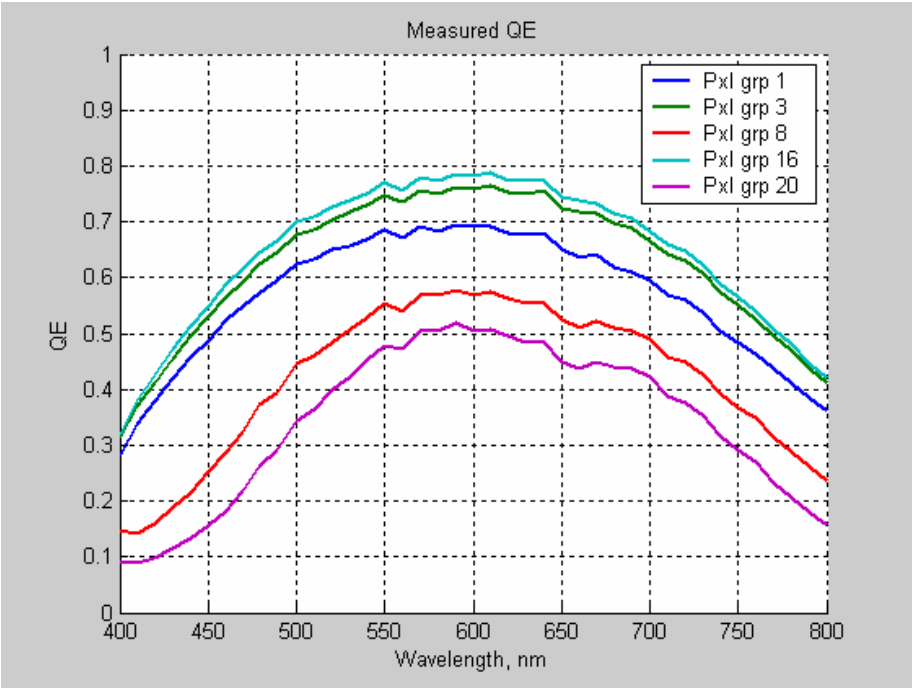

Figure 12. Measured quantum efficiency of 5 pixel groups (with microlens)

4. WORK IN-PROGRESS

Following the characterization of the prototype device described in this paper, we have completed the design and released for fabrication, a more advanced prototype sensor which features 8 variations of a 5T pixel design with global shutter capability and column level amplifiers with four gain stages and on-chip single slope analog to digital converters (ADC). The device is designed for very high speed operation and includes high-speed transceiver logic (HSTL) I/O structures.

5. CONCLUSIONS

The completion of this phase of the project provided us with a more complete understanding of the 0.18-µm CIS process capabilities and its limitations. We achieved significant improvements in performance compared to the original prototype sensor design:

- read noise is lower by 40%,
- dark current is reduced by almost 50%,
- quantum efficiency is improved by 37%, and
- MTF is significantly improved.

The characterization data helped us identify the key design parameters which impact the sensor performance. The data clearly underscore the fact that image lag is very sensitive to the pixel design and must be prevented to avoid undesirable results. We also verified that the read noise is closely related to the size of the source follower transistor. In terms of the pixel design, the knowledge we gained from this phase helps establish a solid foundation for the development of high-performance commercial products.

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