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Low-Light-Level CMOS Image Sensor For Digitally Fused Night Vision Systems

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ABSTRACT

In this paper we present a VNIR solid state sensor technology suitable for next generation fused night vision systems. This technology is based on a highly optimized low power 0.18um CMOS image sensor (CIS) process. We describe a 320(H) x 240(V) pixel prototype sensor based on this technology. The sensor features 5T pixels with pinned photodiodes on a 6.5µm pitch with integrated micro-lens. The 5T pixel architecture enables both correlated double sampling (CDS) and a lateral anti-blooming drain. The measured peak quantum efficiency of the sensor is greater than 50% at 600nm, and the read noise is less than 1e- RMS at room temperature. The sensor does not have any multiplicative noise. The full well capacity is greater than 40ke-, the dark current is less than 3.8pA/cm^2 at 20ºC, and the MTF at 77 lp/mm is 0.4 at 600nm. The sensor also achieves an intra-scene linear dynamic range of greater than 90dB (30000:1) at room temperature.

Keywords: CMOS image sensor, Low noise, low dark current, wide dynamic range, night vision

1. INTRODUCTION

Next generation night vision systems will use fused infra-red (IR) and visible/near infra-red (VNIR) sensors to produce multi-spectral imagery for both local and remote viewing by soldiers, firefighters, and search and rescue teams [1,2]. Currently there are several solutions for uncooled digital IR sensors that meet the size, weight, power, cost, and performance requirements for this application. A typical example is VOx based micro-bolometer IR sensors. Currently the gold standard for VNIR sensors is the GENIII night vision tube. Although these tubes achieve a very high level of performance with minimal power dissipation, they cannot be used in fused night vision systems because they do not produce digital data. Several different VNIR sensor technologies are being actively investigated to remedy this problem. Although the most popular technologies are electronic image intensified sensors [3,4], CMOS image sensors (CIS) offer many advantages for this application. Some of these advantages include: high MTF, high reliability, small size, low weight, low-cost system on chip integration, day night color imaging, and imaging out to 1.1 µm. Moreover, the spectral range of silicon allows the use of covert LED illumination outside the range of standard GaAs photo-cathodes, and imaging of 1.06 µm illumination sources.

In this paper we present a VNIR solid state sensor technology suitable for next-generation fused night vision systems. This technology is based on a highly optimized low power 0.18um CMOS image sensor (CIS) process. We describe a 320(H) x 240(V) pixel prototype sensor based on this technology. The sensor features 5T pixels with pinned photodiodes on a 6.5µm pitch with integrated micro-lens. The 5T pixel architecture enables both correlated double sampling [5] and a lateral anti-blooming drain [6]. The measured peak quantum efficiency of the sensor is greater than 50% at 600nm, and the read noise is less than 1e- RMS at room temperature. The sensor does not have any multiplicative noise. The full well capacity is greater than 40ke-, the dark current is less than 3.8pA/cm2 at 20ºC, and the MTF at 77 lp/mm is 0.4 at 600nm. The sensor also achieves an intra-scene linear dynamic range of greater than 90dB (30000:1) at room temperature.

The prototype chip has on-chip dual column level amplifiers and 11-bit single slope analog to digital converters (ADC) for high speed readout and wide optical dynamic range. The dual column level amplifier/ADC pairs have independent gain settings, and the final image is reconstructed by combining pixel readings from both the high and low gain readout channels to achieve a wide intra-scene dynamic range. The bandwidths of the column level amplifiers and ADCs are programmable to optimize the sensor read noise for the selected sensor frame rate. The sensor can operate up to a line rate of 9us or a frame rate of 462Hz. The high speed digital readout electronics allow pixels to be scanned out at up to 287MHz.

The remainder of the paper is organized as follows: in Section 2 the sensor operation, architecture, and circuitry are described, in Section 3 the measurement methods and results are presented, and finally in Section 4 we conclude the paper.

2. SENSOR OPERATION

Figure 1 shows the image sensor block diagram. The image sensor consists of an array of 320(H) x 240(V) 6.5µm x 6.5µm pixels, row and column shift registers, 320 high gain and low gain column level amplifiers and 640 11-bit single slope ADCs, a high speed 22-bit digital readout multiplexer, bias generators, and a bandgap based proportional to absolute temperature (PTAT) sensor. The image sensor operates at pixel rates up to 287 MHz and uses standard 1.8V HSTL I/Os for clock and data signals.

The sensor array consists of eight different pixel types, arranged in 8 columns of 40(H) x 240(V) pixels. Each pixel type has different photodiode and transfer gate sizes. These pixel variations were designed to determine the optimal pixel for low light level applications. Micro-lenses are used on all of the pixels. Some of the sensors also have Bayer pattern RGB color filter arrays [7]. Figure 2 shows a simplified schematic of the 5T pinned photodiode pixel. The charge transfer transistor connected to “TX1” is used to move charge from the pinned photodiode to the floating diffusion node. The source follower transistor size was optimized to minimize read out noise [8]. The reset transistor forces the floating diffusion node to “Vrst” when “reset” is high. When “word” is high the source follower is connected to the bit line and the voltage on the floating diffusion is readout. The transistor connected to TX2 functions as a voltage controlled anti-blooming drain and a global reset device.

The row shift register is located at the left side of the chip. The row shift register selects one row of pixels at a time by enabling the “word” line in a given row. During that time, the floating diffusion node in the selected pixel is reset, the reset voltage is read out then the transfer gate is turned on, via TX1, and the integrated charge on the pinned photo-diode is transferred to the floating diffusion node. The signal voltage on the floating diffusion node is read out again. The reset and signal voltages are initially stored on sampling capacitors of both column level amplifiers (high gain and low gain); then the analog data is transferred to a double buffered analog memory (capacitor bank). Then the analog data (stored in the capacitor bank) is digitized using dual 11-bit single slope ADCs. Using the column shift register the double buffered digital data is read out of the sensor. Afterward, the next row is selected and the read out processes continues in a similar fashion. The photodiode inside each pixel starts integration once the transfer gate is turned off. In this scheme, each row of pixels will have the same length of integration time, but a different start and ending time, therefore this scheme is called “rolling shutter”.

The sensor has a 22-bit digital output port operating at up to 287 MHz. The digital data at the column is transferred to the output pins using a two level 320:1 digital multiplexer. Note that each pixel is simultaneously readout twice, once through a high gain amplifier and once through a low gain amplifier. Both the high gain amplifier and the low gain amplifier outputs are digitized to 11 bits. The maximum frame rate of the sensor is limited by the settling time of the column amplifiers, i.e. 9us. The maximum frame rate of the sensor is 462 frames per second.

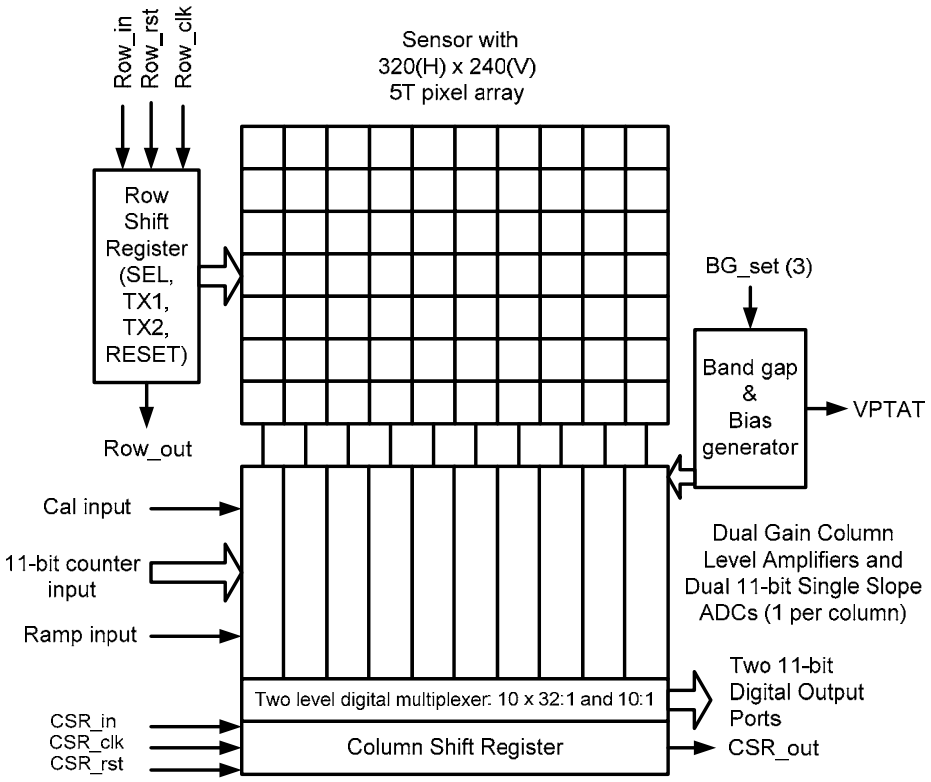

Figure 1. Sensor Block Diagram

Separate power supplies are used for pixel core, analog amplifiers and ADC, pad ring, and digital circuitry. Common ground is used in the entire chip. A power down pin is used to shut down all the bias and analog circuits. Internally, one reference circuit generates a 100uA bias current which in turn generates different bias voltages for column amplifiers and the pixel array.

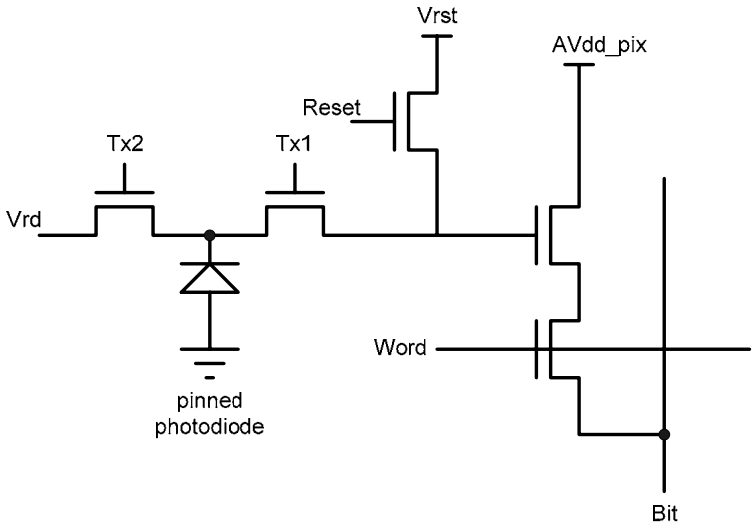

Figure 2. 5T Pixel Schematic

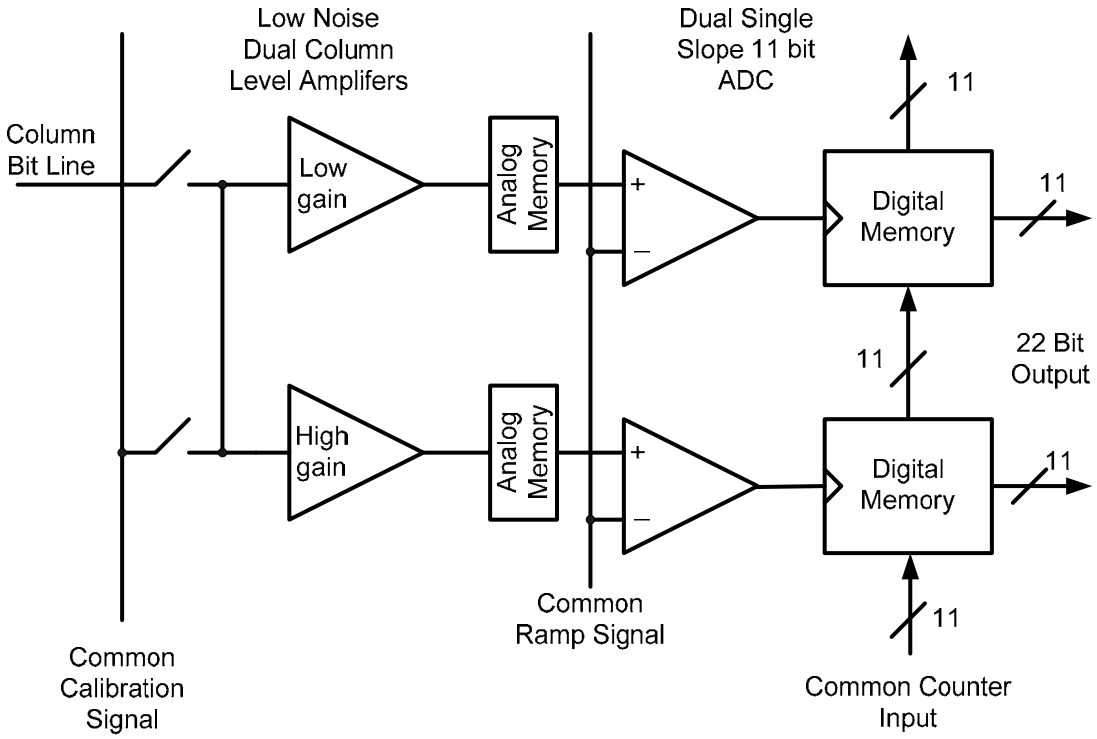

Figure 3. Column level amplifier and ADC block diagram

Figure 3 shows the amplifier and ADC architecture used in each column of the sensor. This architecture was selected to minimize the read noise and maximize the dynamic range simultaneously. There are two amplifiers per column with fixed gains of 30x and 1x respectively. These gain values were selected to minimizing the dip in the sensor SNR when the user switches between the high gain data and the low gain data. Each column also contains two 11-bit single slope ADCs. The amplifier outputs and the ADC outputs are double buffered to maximize the line rate of the sensor. Each column has a reference input that can be multiplexed into the circuit to aid in correcting column level gain and offset fixed pattern noise. The 320 columns are divided to 10 segments, each segment has 32 columns.

3. RESULTS

Most of the performance parameters were estimated using a pixel level photon transfer based method [9]. These performance metrics include conversion gain, read noise, full well capacity, linearity, pixel response non-uniformity, dark current, dark current non-uniformity and fixed pattern noise. The QE was estimated using the method described in [10], and the MTF was estimated using the ISO12233 standard. Since the sensor array is composed of eight different pixel types most of the figures in this section display eight different values or functions. Pixel type 7 has the best overall performance, and therefore some of the figures only display data from these pixels. All of the data was collected using a line time of 64us, and integration time was varied based on the measurement. The sensor temperature was not controlled, but it was measured for each data set. Sample captured images from a sensor featuring a uniform array of pixel type 7 are shown in Figure 4.

The conversion gain of the high gain output is shown in Figure 5 and the conversion gain of the low gain output is shown in Figure 6. Note that the ratio between high gain and low gain outputs is about 32 to 1, and the design goal was 30 to 1. In addition, all of the pixel types have approximately the same conversion gain. This was expected since the size of the floating diffusion node and the source follower transistor were held constant across all pixel types.

The read noise of the high gain output is show in Figure 7, and the read noise of the low gain output is shown in Figure 8. The read noise of each pixel is individually estimated using 100 frames, and the statistics are calculated pixel by pixel. Moreover, the standard deviation of the read noise represents the pixel to pixel variation. When the read noise is dominated by the pixel source follower and transfer gate 1/f and RTS noise the standard deviation of the read noise is on the same order as the mean value. Conversely, if the read noise is dominated by the white and 1/f noise in the column amplifiers then the standard deviation is much lower than the mean value. The high gain output read noise distribution of pixel 7 is shown in Figure 9, and the low gain read noise distribution of pixel 7 is shown in Figure 10.

The sensors dark current at 20°C is shown in Figure 11. Although the n region of the pinned photodiode and the size of the transfer gate were varied significantly from pixel type to pixel type the dark current stayed relatively constant. This implies that the dark current is not an edge or depletion based effect. The dominant leakage component is likely caused by carrier diffusion from the undepleted region of the pixel [11]. Figure 12 shows the dark current distribution of pixel 7 at 37.5°C. The dark current doubling rate is about 7°C at room temperature.

The full well capacity of the sensor is shown in Figure 13. The full well capacity of the sensor is defined as the number of electrons that can be collected before the sensor response has more than a 2% non-linearity. The pinned photodiodes in pixels 1 through 4 have a much smaller n region than pixels 5 through 8. Therefore, as expected the full well capacity of each pixel is almost linearity related to the size of the pinned photodiode n region. The dynamic range of pixel 7, i.e. the full well capacity divided by the mean high gain read noise, is about 35,000:1.

The quantum efficiency (QE) of the sensor, defined as the number of electrons collected divided by the number of incident photons, is shown in Figure 14. The number of incident photons was calculated based on 6.5µm x 6.5µm pixel area.

The modulation transfer function (MTF) of the sensor is shown in Figure 15. The upper function is the vertical MTF and lower function is the horizontal MTF. The pixel has a metal aperture to protect the readout electronics and this causes the MTF to be different in the vertical and the horizontal directions. Note that the MTF was measured with a 0.26 NA diffraction limited microscope lens. The sensor MTF was determined by de-convolving the lens MTF from the measured system MTF.

The limiting resolution of this sensor could not be directly measured due to the array of different pixels used on this device, but Figure 16 shows the limiting resolution of a similar device with a single pixel type. The measurements were performed at NVESD with a 100% contrast 1951 USAF resolution target and a 2856K black body light source.

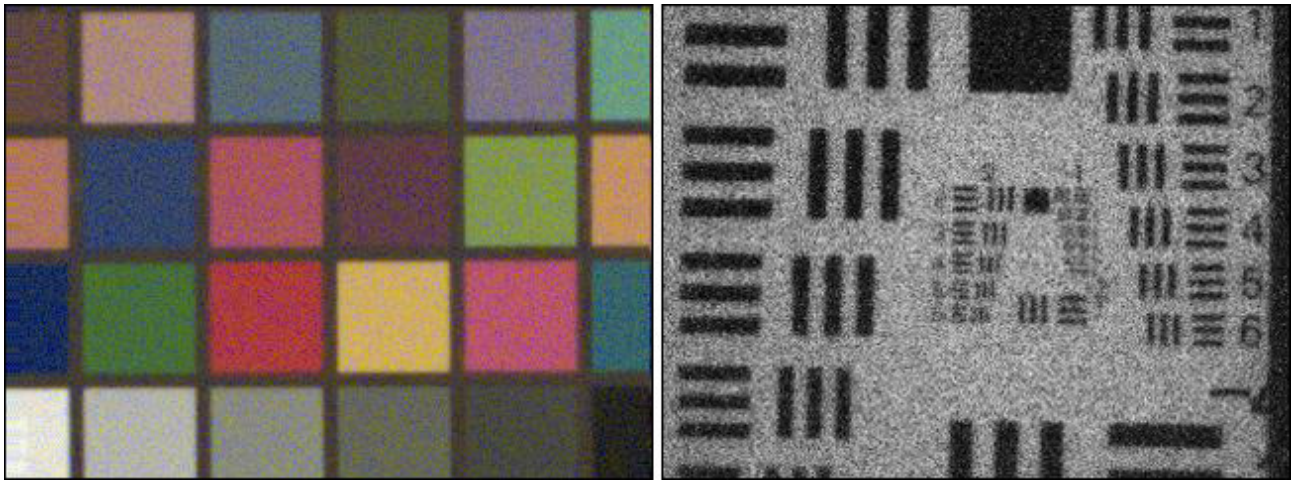

Figure 4. Images captured with a similar sensor with RGB filters of the Macbeth color chart under low light, and without color filters, of the USAF target under 1/4-moon equivalent illumination

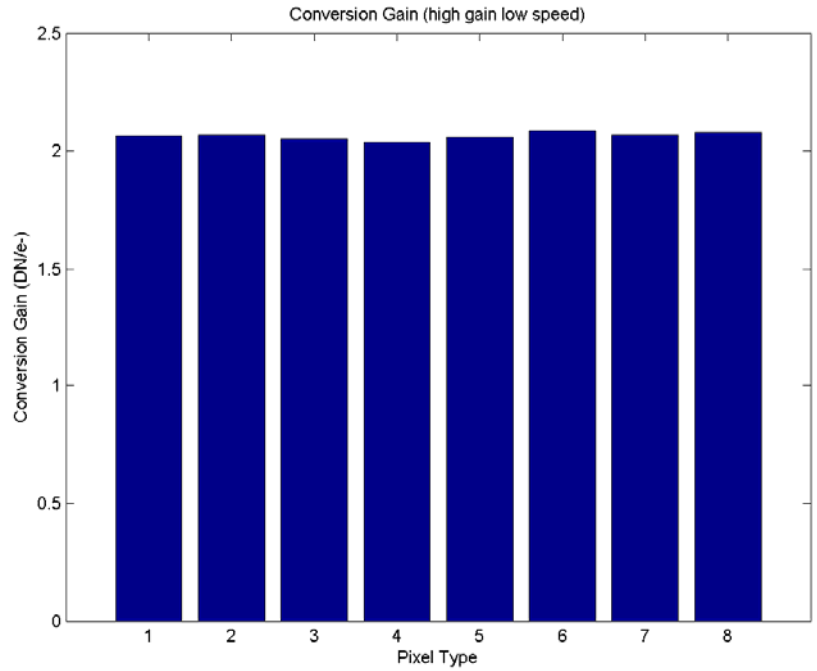

Figure 5. High gain channel conversion gain of each pixel type

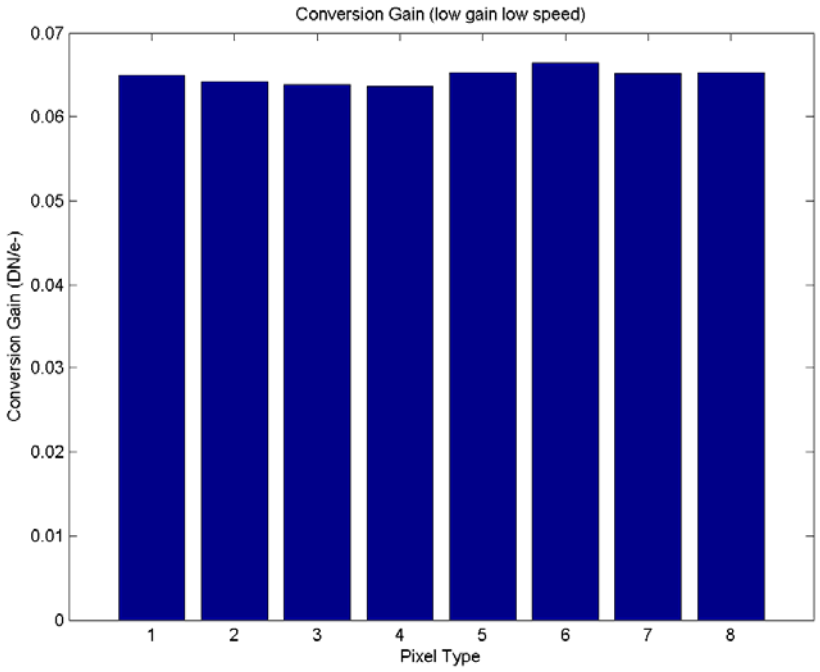

Figure 6. Low gain channel conversion gain of each pixel type

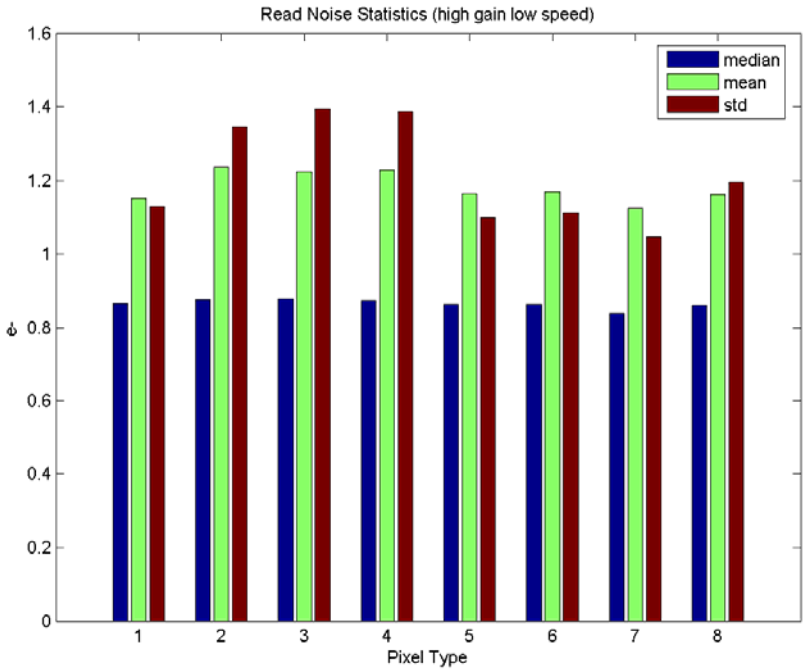

Figure 7. High gain channel read noise of each pixel type

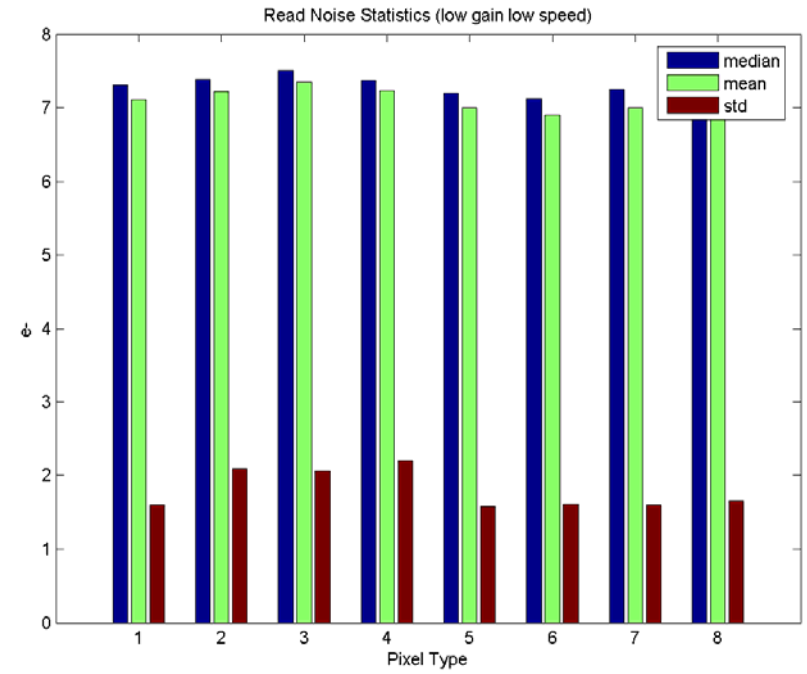

Figure 8. Low gain channel read noise of each pixel type

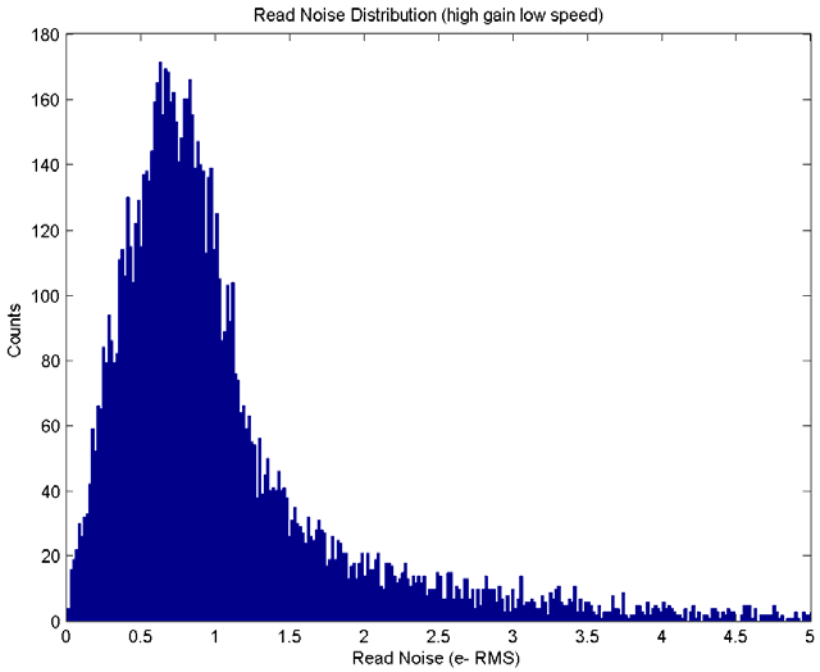

Figure 9. High gain channel read noise distribution of pixel 7

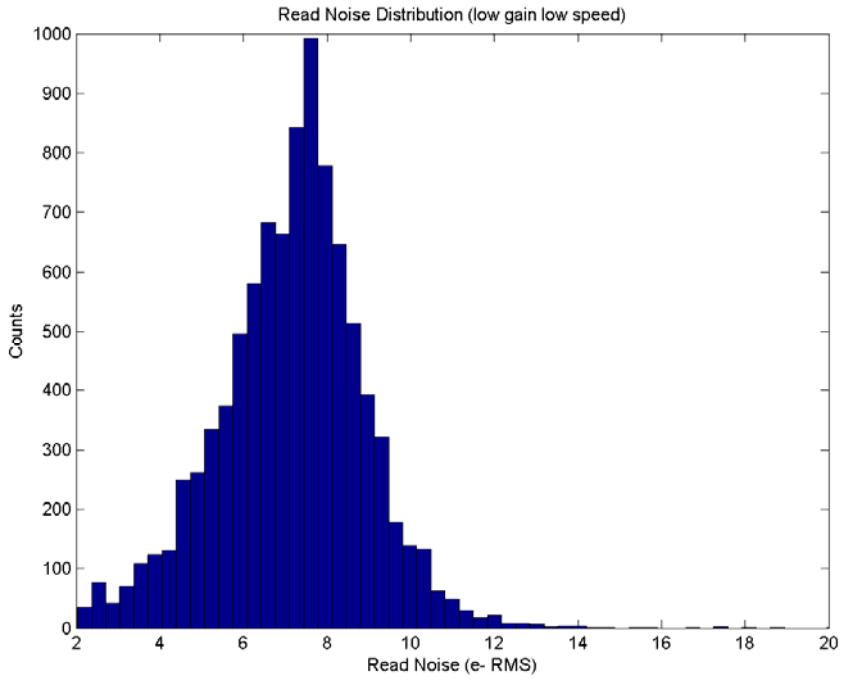

Figure 10. Low gain channel read noise distribution of pixel 7

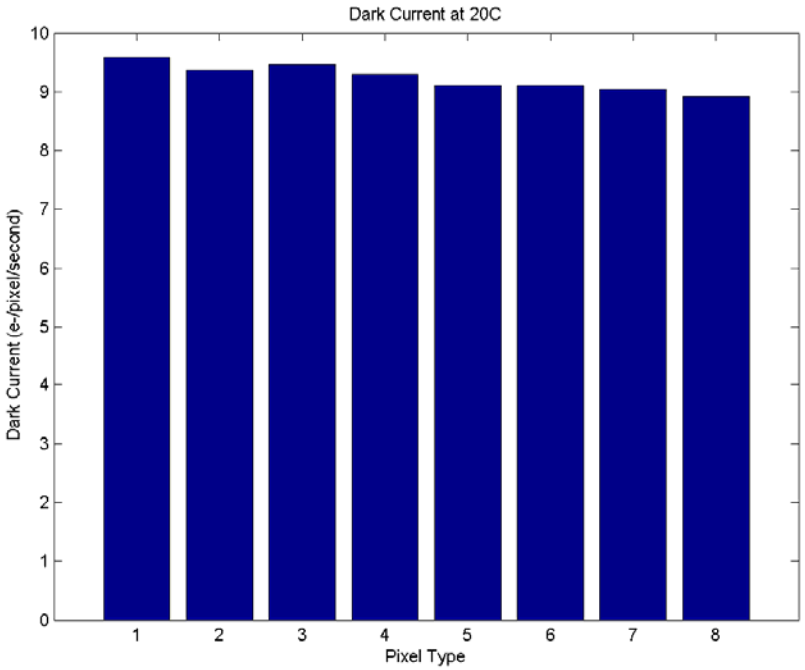

Figure 11. Dark current of each pixel type at 20ºC

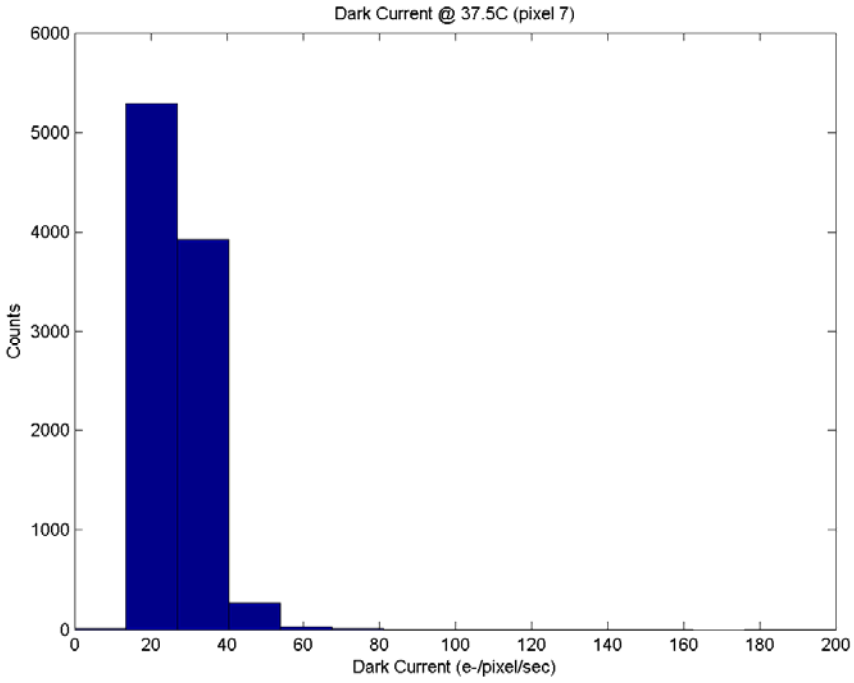

Figure 12. Dark current distribution of pixel 7 at 37.5ºC

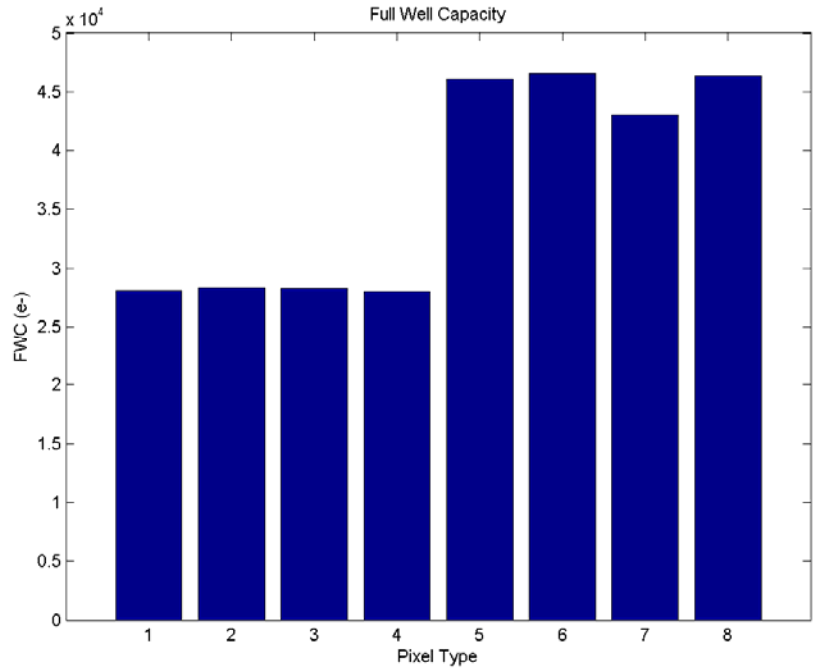

Figure 13. Full well capacity of each pixel type

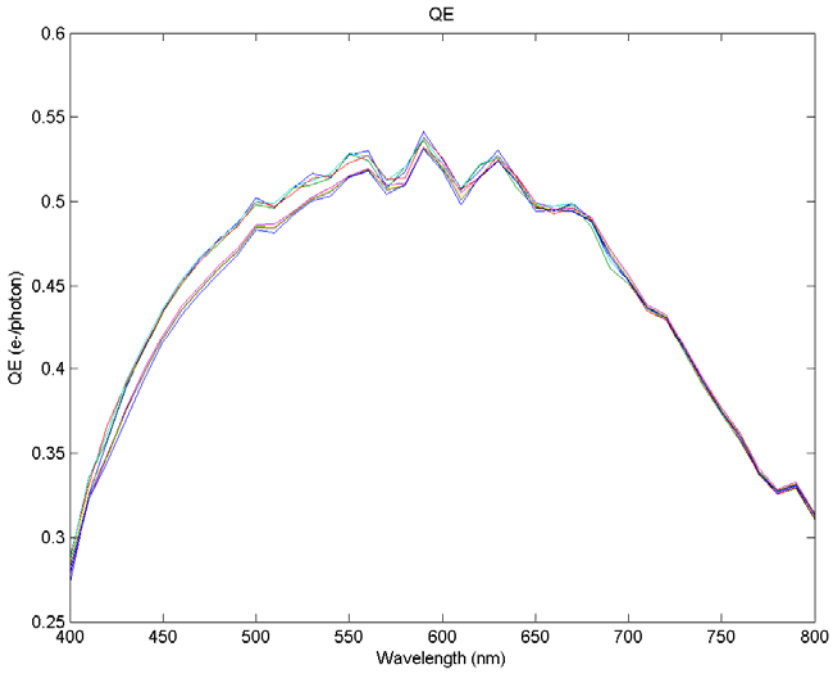

Figure 14. Measured QE of each pixel type

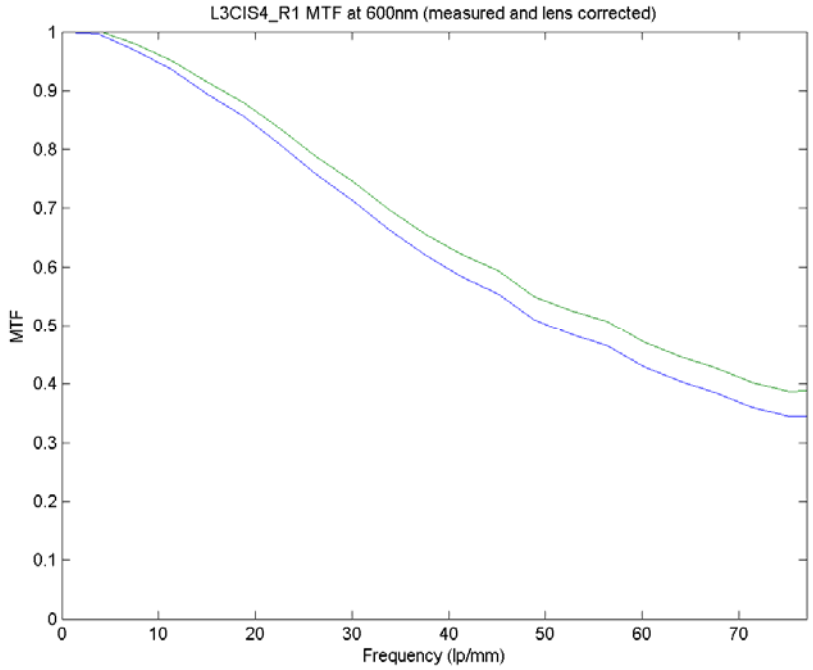

Figure 15. Measured MTF of pixel 7 at 600 nm (green line is vertical MTF and blue line is horizontal MTF)

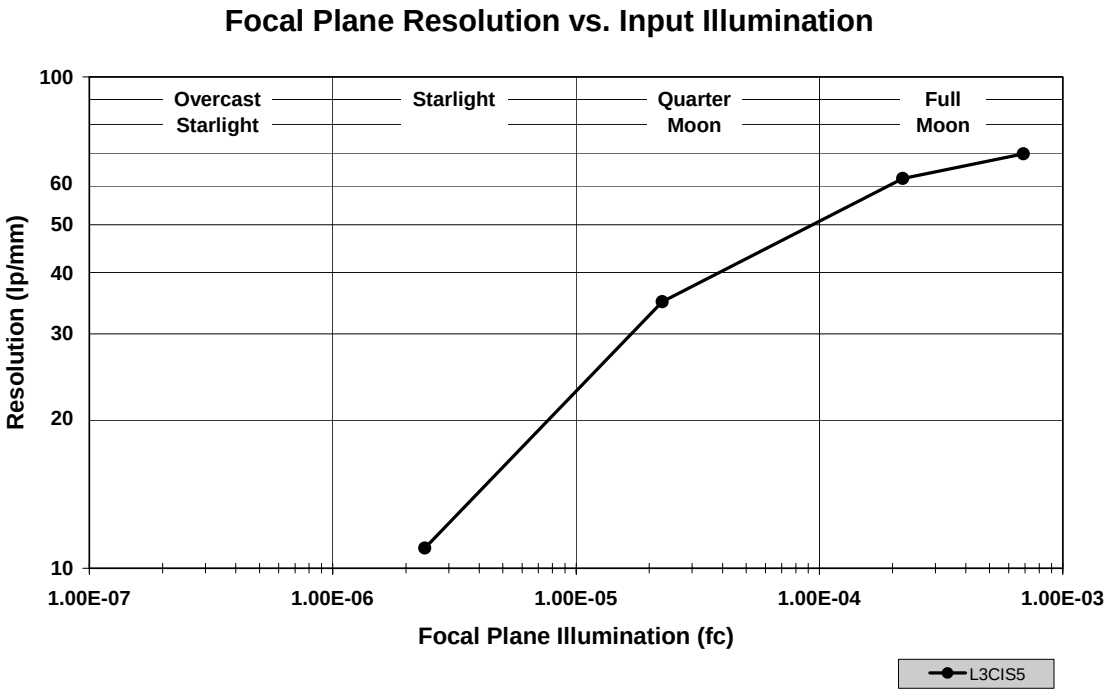

Figure 16. Measured limiting resolution of similar sensor with uniform pixel type

4. CONCLUSIONS

We have presented a CMOS image sensor with dual column level amplifiers and 11-bit ADCs. This sensor achieves a median read noise of 0.8e- RMS, a dynamic range greater than 30,000:1, a peak QE greater than 50%, and an MTF at 600nm of approximately 40%. This sensor can be used in both day and night environments. In addition, it can be integrated with color filter arrays to provide day night color. Although it is not as sensitive as a GEN III tube under overcast starlight, it does offers a wider dynamic range, no halo or blooming, color, higher reliability, smaller size, lower weight, and lower cost. Finally, when integrated in a fused night vision system the sensor's limitations at the lowest light levels are supplemented by the IR channel making this sensor an excellent fit for the next generation of fused day night military vision systems.

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