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Application Note 7526

Single Channel MicroFET™ 3x2 Power MOSFET Recommended Land Pattern and Thermal Performance

Roman Gurevich , Scott Pearson , Ray Poremba

Introduction

Fairchild 's new MicroFET™ 3x2 package with exposed drain pad provides a true surface-mount alternative that greatly improves thermal characteristics, high current handling capability and low on-resistance. These devices are intended for applications where a miniaturized package is required. This application note discusses pin-outs, land pattern and thermal performance for the single pad MicroFET.

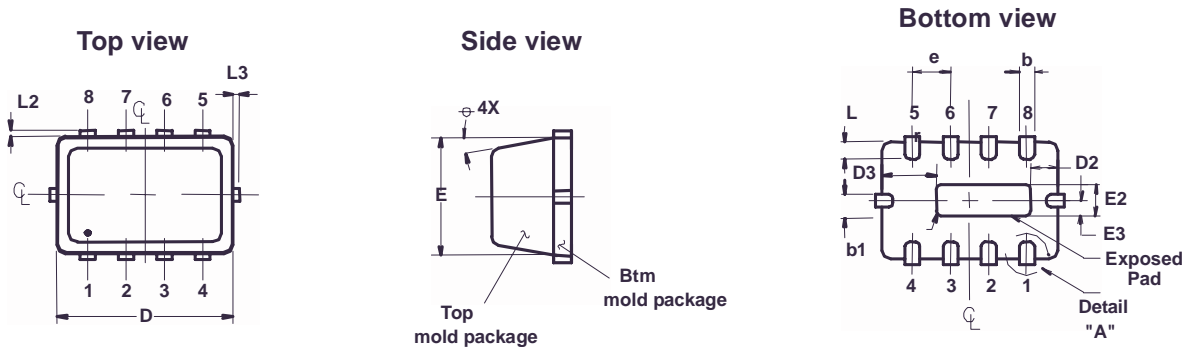
Pin-out

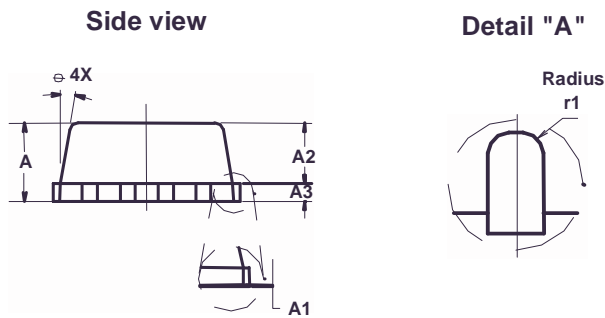
Figure 1 shows the MicroFET™ 3x2 package and pin-out assignment for the single P-channel device. Thermal paths are kept to a minimum by two means. First, the use of a leadless package reduces thermal resistance relative to a leaded package. Second, a thermal pad underneath the package permits an optimal package cooling interface to the PCB.



Figure 1. Single MicroFET™ 3x2-8

MicroFET™ Single Package Dimensions





MicroFET 3x2 single pad land pattern recommendation

The basic land pattern layout and dimensions are shown in Figure 2. This land pattern was designed according to application note 7525.

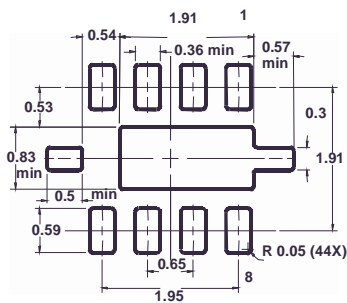


Figure 2. Recommended land pattern

Dimensions

SYMBOL	MILLIMETERS		NOTES
	MIN	MAX	
A	0.80	1.00	1
A1	0.00	0.05	1
A2	0.65	0.75	1
A3	0.15	0.25	1
b	0.12	0.28	1
b1	0.17	0.30	1
D	2.90	3.10	1
E	1.90	2.10	1
D2	0.46	0.61	1
E2	0.45	0.60	1
D3	0.91	1.07	1
E3	0.15	0.35	1
e	0.65 BSC		1
L	0.21	0.37	1
L2	0.00	0.10	1
L3	0.00	0.10	1
N	8		4
r	0.127 BSC		1
r1	0.127 BSC		1
∅	0°	12°	

NOTES:

1. All dimensions are in mm.
2. Package outline exclusive of mold flash & metal burr.
3. Package outline inclusive of plating.
4. N is the total number of terminals.
5. Package surface finishing of Ra 0.4 um max.

Thermal Performance

Junction-to-Case Thermal Resistance (the Package Performance)

Thermal performance for the single MicroFET 3x2-8 package is measured as junction-to-case thermal resistance, in which the "case" is the center drain pad of the device. The junction-to-case thermal resistance for this device is typically 4.5 °C/W, with a maximum thermal resistance of approximately 6.0 °C/W. This data compares favorably with another surface mount package the SO-8. For example, the junction-to-case thermal resistance for the typical SO-8 package is 22 °C/W typical and 25 °C/W maximum. Figure 3 demonstrates the comparison between MicroFET 3x2 and SO-8 package's sizes.

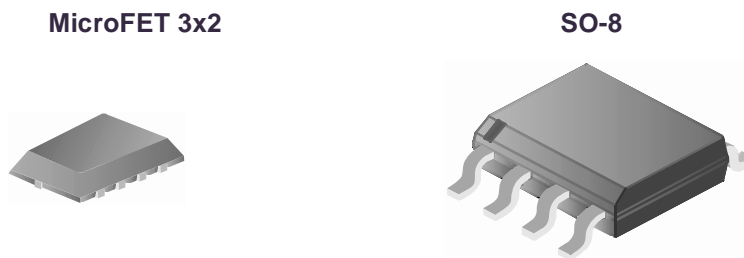


Figure 3. Relative Package Size

Junction-to-Ambient Thermal Resistance

The typical junction-to-ambient thermal resistance for the single MicroFET 3x2 package is 58 °C/W steady state and about 65 °C/W maximum for the 1in² copper area. Figure 4 illustrates MicroFET 3x2 single thermal performance.

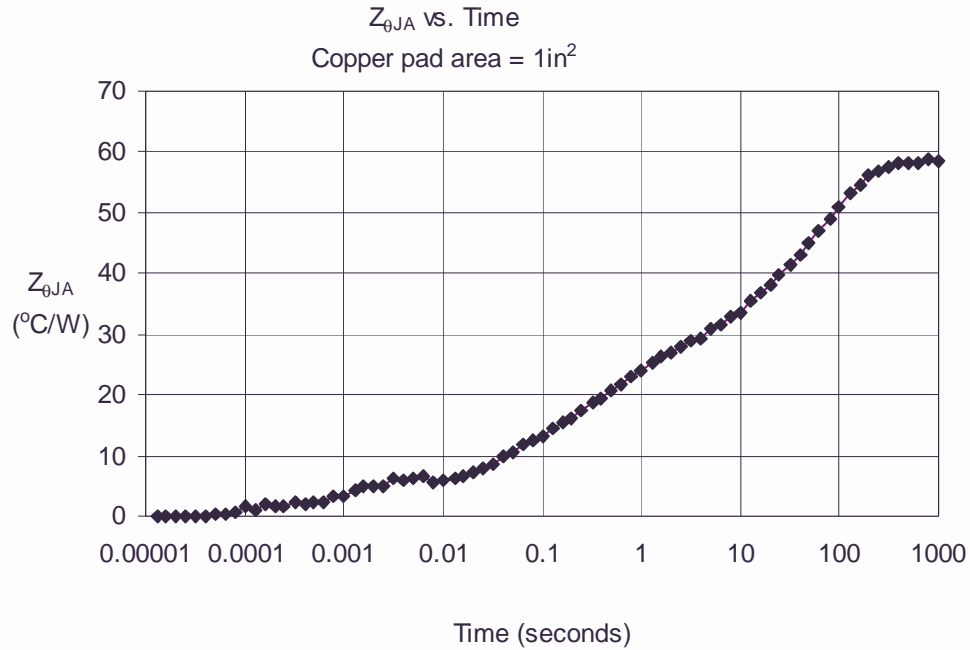


Figure 4. Thermal Impedance of single MicroFET 3x2

For comparison the junction-to-ambient thermal resistance for the typical SO-8 package is 68 °C/W typical and 75 °C/W maximum for the 1in² copper area. The power dissipation for the SO-8 package is 1.7 W for the 1in² copper area at 150 °C. For the MicroFET 3x2 single package the power dissipation is 2.23 W for the 1in² copper area at 150 °C.

The results indicate significantly better thermal performance for the MicroFET 3x2 package - much smaller package has greater thermal characteristics.

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