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DC Electrical Characteristics of MM74HC High-Speed CMOS Logic

Fairchild Semiconductor
 Application Note 313
 Larry Wakeman
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DC Electrical Characteristics of MM74HC High-Speed CMOS Logic

The input and output characteristics of the MM74HC high-speed CMOS logic family were conceived to meet several basic goals. These goals are to provide input current and voltage requirements, noise immunity and quiescent power dissipation similar to CD4000 and MM74C metal-gate CMOS logic and output current drives similar to low power Schottky TTL. In addition, to enable merging of TTL and HC-CMOS designs, the MM74HCT sub family differs only in their input voltage requirements, which are the same as TTL, to ease interfacing between logic families.

In order to familiarize the user with the MM74HC logic family, its input and output characteristics are discussed in this application note, as well as how these characteristics are affected by various parameters such as power supply voltage and temperature. Also, for those users who have been designing with metal-gate CMOS and TTL logic, notable differences and features of high-speed CMOS are compared to those logic families.

A Buffered CMOS Logic Family

The MM74HC is a "buffered" logic family like the CD4000B series CMOS. Buffering CMOS logic merely denotes designing the IC so that the output is taken from an inverting buffer stage. For example, the internal circuit implementation of a NAND gate would be a simple NAND followed by two inverting stages. An unbuffered gate would be implemented as a single stage. Both are shown in *Figure 1*. Most MSI logic devices are inherently buffered because they are inherently multi-stage circuits. Gates and similar small circuits yield the greatest improvement in performance by buffering.

There are several advantages to buffering this high-speed CMOS family. By using a standardized buffer, the output characteristics for all devices are more easily made identical. Multi-stage gates will have better noise immunity due to the higher gain caused by having several stages from input to output. Also, the output impedance of an unbuffered gate may change with input logic level voltage and input logic combination, whereas buffered outputs are unaffected by input conditions.

Finally, single stage gates implemented in MM74HC CMOS would require large transistors due to the large output drive requirements. These large devices would have a large input capacitance associated with them. This would affect the speed of circuits driving into an unbuffered gate, especially when driving large fanouts. Buffered gates have small input transistors and correspondingly small input capacitance.

One may think that a major disadvantage of buffered circuits would be speed loss. It would seem that a two or three stage gate would be two to three times slower than a buffered one. However, internal stages are much faster than the output stage and the speed lost by buffering is relatively small.

The one exception to buffering is the MM74HCU04 hex inverter which is unbuffered to enable its use in various linear and crystal oscillator applications.

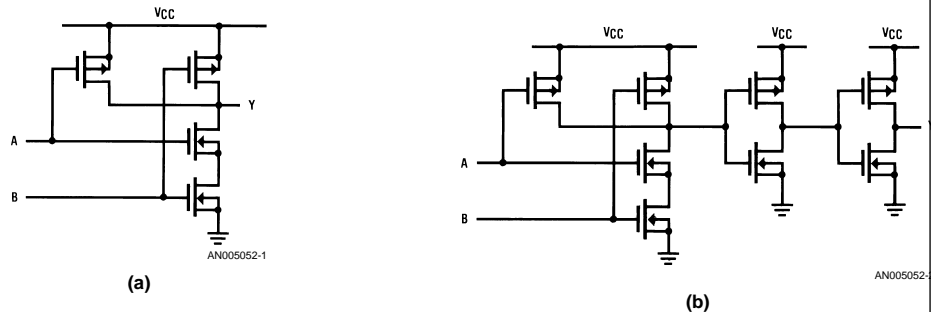


FIGURE 1. Schematic Diagrams of (a) Unbuffered and (b) Buffered NAND Gate

CMOS Input Voltage Characteristics

As mentioned before, MM74HC standard input levels are similar to metal-gate CMOS. This enables the high-speed logic family to enjoy the same wide noise margin of CD4000 and MM74C logic. With $V_{CC}=5V$ these input levels are 3.5V for minimum logic "1" (V_{IH}) and 1.0V for a logic "0" (V_{IL}). The output levels when operated at $V_{CC}=5V \pm 10\%$ and worst case input levels, are specified to be $V_{CC}-0.1$ or 0.1V. The output levels will actually be within a few millivolts of either V_{CC} or ground.

When operated over the entire supply voltage range, the input logic levels are: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. *Figure 2* illustrates the input voltage levels and the noise margin of these circuits over the power supply range. The shaded area indicates the noise margin which is the difference between the input and output logic levels. The logic "1" noise margin is 29% of V_{CC} and the logic "0" noise margin is 19% of V_{CC} . Also shown for comparison are the 74LS input levels and noise margins over their supply range.

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These input levels are specified on individual data sheets at $V_{CC}=2.0V, 4.5V, 6.0V$. At 2.0V the input levels are not quite $0.7(V_{CC})$ and $0.2(V_{CC})$ as at low voltages transistor turn on thresholds become significant. This is shown in Figure 2.

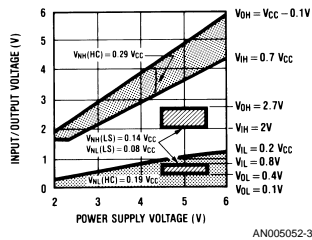


FIGURE 2. Worst Case Input and Output Voltages Over Operating Supply Range for "HC" and "LS" Logic

The input and output logic voltages and their behavior with temperature variation is determined by the input to output transfer function of the logic circuit. Figure 3 shows the transfer function of the MM74HC00 NAND gate. As can be seen, the NAND gate has V_{CC} and ground output levels and a very sharp transition at about 2.25V. Thus, good noise immunity is achieved, since input noise of a volt or two will not appear on the output. The transition point is also very stable with temperature, drifting typically 50 or so millivolts over the entire temperature range. As a comparison, the transfer function for a 74LS00 is plotted in Figure 4. LSTTL output transitions at about 1.1V and the transition region varies several hundred millivolts over the temperature range. Also, since the transition region is closer to the low logic level, less ground noise can be tolerated on the input.

In typical systems, noise can be capacitively coupled to the signal lines. The amount of voltage coupled by capacitively induced currents is dependent on the impedance of the output driving the signal line. Thus, the lower the output impedance the lower the induced voltage. High-speed CMOS offers improved noise immunity over CD4000 in this respect because its output impedance is one tenth that of CD4000 and so it is about 7 times less susceptible to capacitively induced current noise.

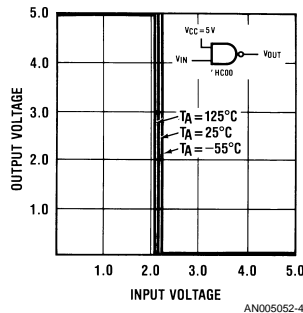


FIGURE 3. Input/Output Transfer Characteristics for (a) HC00

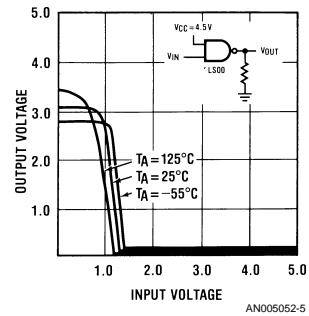


FIGURE 4. Input/Output Transfer Characteristics for (b) LS00 Nand Gate

The MM74HCT sub-family of MM74HC logic provides TTL compatible input logic voltage levels. This will enable TTL outputs to be guaranteed to correctly drive CMOS inputs. An incompatibility results because TTL outputs are only guaranteed to pull to a 2.7V logic high level, which is not high enough to guarantee a valid CMOS logic high input. To design the entire family to be TTL compatible would compromise speed, input noise immunity and circuit size. This sub-family can be used to interface sub-systems implemented using TTL logic to CMOS sub-systems. The input level specifications of MM74HCT circuits are the same as LSTTL. Minimum input high level is 2.0V and the maximum low level is 0.8V using a $5V \pm 10\%$ supply.

A fairly simple alternative to interfacing from LSTTL is to tie a pull-up resistor from the TTL output to V_{CC} , usually 4–10 k Ω . This resistor will ensure that TTL will pull up to V_{CC} . (See Interfacing MM74HC High-Speed CMOS Logic application note.)

High-Speed CMOS Input Current and Capacitance

Both standard "HC" and TTL compatible "HCT" circuits maintain the ultra low input currents inherent in CMOS circuits when CMOS levels are applied. This current is typically less than a nanoamp and is due to reverse leakages of the input protection diodes. Input currents are so small that they can usually be neglected. Since CMOS inputs present essentially no load, their fanout is nearly infinite.

Each CMOS input has some capacitance associated with it, as do TTL inputs. This capacitance is typically 3–5 pF for MM74HC, and is due to package, input protection diode, and transistor gate capacitances. Capacitance information is given in the data sheets and is measured with all pins grounded except the test pin. This method is used because it yields a fairly conservative result and avoids capacitance meter and power supply ground loops and decoupling problems. Figure 5 plots typical input capacitance versus input voltage for HC-CMOS logic with the device powered on. The small peaking at 2.2V is due to internal Miller feedback capacitance effects.

When comparing MM74HC input currents to TTL logic, 74LS does need significantly more input current. LSTTL requires 400 μA of current when a logic low is applied and 40 μA in the high state which is significantly more than the worst case 1 μA leakage that MM74HC has.

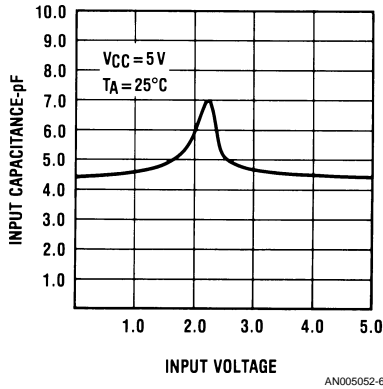


FIGURE 5. Input Capacitance vs. Input Voltage for a Typical Device

MM74HC Power Supply Voltage and Quiescent Current

Figure 6 compares the operating power supply range of high-speed CMOS to TTL and metal-gate CMOS. As can be seen, MM74HC can operate at power supply voltages from 2–6V. This range is narrower than the 3–15V range of CD4000 and MM74C CMOS. The narrower range is due to the silicon-gate CMOS process employed which has been optimized to attain high operating frequencies at $V_{CC}=5\text{V}$. The 2–6V range is however much wider than the 4.5V to 5.5V range specified for TTL circuits, and guaranteeing operation down to 2V is useful when operating CMOS off batteries in portable or battery backup applications.

The quiescent power supply current of the high-speed CMOS family is very similar to CD4000 and MM74C CMOS. When CMOS circuits are not switching there is no current path between V_{CC} and ground, except for leakage currents which are typically much less than 1 μA . These are due to diode and transistor leakages.

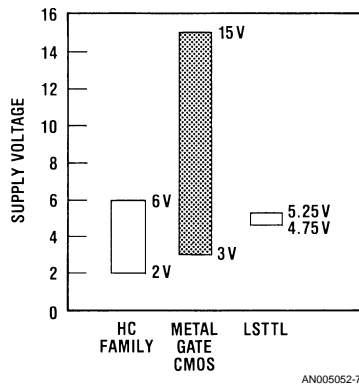


FIGURE 6. Comparison of Supply Range for "HC", "LS" and Metal-Gate

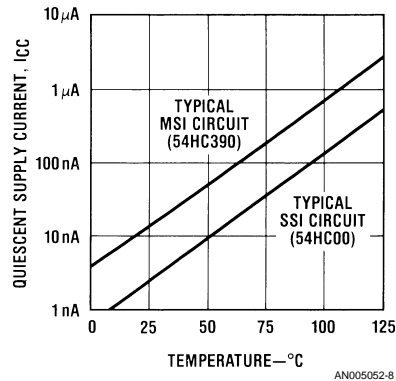


FIGURE 7. Typical Quiescent Supply Current Variation with Temperature

Figure 7 illustrates how this leakage increases with temperature by plotting typical leakage current versus temperature for an MSI and SSI device. As a result of this temperature dependence, there is a set of standardized I_{CC} specifications which specify higher current at elevated temperatures. A summary of these specifications are shown in Table 1.

TABLE 1. Standardized I_{CC} Specifications for MM74HC Logic at 25°C, 85°C and 125°C at $V_{CC}=6.0\text{V}$

Temperature	Gates	Flip-Flops	MSI
25°C	2 μA	4 μA	8 μA
85°C	20 μA	40 μA	80 μA
125°C	40 μA	80 μA	160 μA

Output Characteristics

One of the prime advantages of MM74HC over metal-gate CMOS (besides speed) is the output drive current, which is about ten times CD4000 or MM74C logic. The larger output current enables high-speed CMOS to directly drive large fanouts of 74LS devices, and also enables HC-CMOS to more easily drive large capacitive loads. This improvement in output drive is due to a variety of enhancements provided by the silicon-gate process used. The basic current equation for a MOSFET is:

$$I = (\text{Beta})(\text{Width}/\text{Length})((V_g - V_t)V_d - 0.5(V_d^2))$$

Where V_g is the transistor gate voltage, V_t is the transistor threshold voltage, and V_d is the transistor drain voltage which is equivalent to the circuit output voltage. This CMOS process, when compared to metal-gate CMOS, has increased transistor gains, Beta, and lower threshold voltages, V_t . Also, improved photolithography has reduced the transistor lengths, and wider transistors are also possible because of tighter geometries.

Figure 8 compares the output high and low current specifications of MM74HC, 74LS and metal-gate CMOS for standard device outputs. High-speed CMOS has worst case output low current of 4 mA which is similar to low power Schottky TTL circuits, and offers symmetrical logic high and low currents as well. In addition, CMOS circuits whose functions

make them ideal for use driving large capacitive loads have a larger output current of 6 mA. For example, these bus driver outputs are used on the octal flip-flops, latches, buffers, and bidirectional circuits.

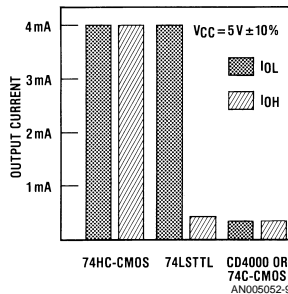
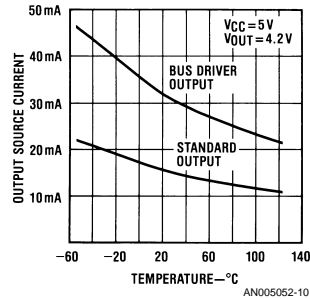


FIGURE 8. Comparison of 74HC, 74LS and CD4000/ 74C Output Drive Currents, I_{OH} and I_{OL}

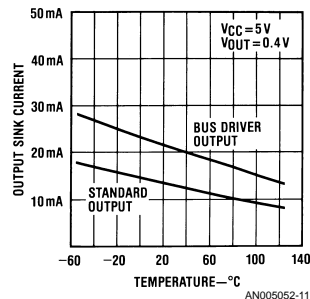
Table 2 summarizes the various output current specifications for MM74HC CMOS along with their equivalent LSTTL fanouts. As Table 2 shows, the output currents of the MM74HC devices are derated from the MM74HC devices. The derating is caused by the decrease in current drive of the output transistors as temperature is increased. To show this, Figures 9, 10 plots typical output source and sink currents against temperature for both standard and bus driver circuits. This variation is similar to that found in metal-gate CMOS, and so the same -0.3% per $^{\circ}\text{C}$ derating that is used to approximate temperature derating of CD4000 and MM74C can be applied to 74HC. As an example, the approximate worst case 25°C current drive one would expect

by using the 4 mA 85°C data sheet number would be about 4 mA at $V_{OUT}=0.26\text{V}$, and this is what is specified in the device data sheets.



(a)

FIGURE 9. Typical Output (a) Source



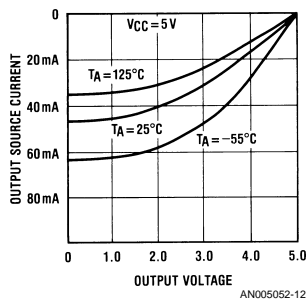
(b)

FIGURE 10. Typical Output (b) Sink Current Temperature for Standard and Bus Outputs

TABLE 2. Data Sheet Output Current Specifications for MM74HC Logic

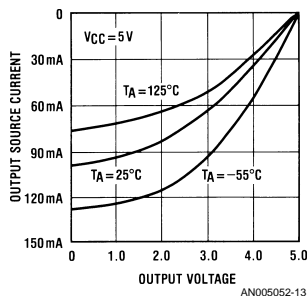
Device $V_{CC}=4.5\text{V}$	Output High Current	Output Low Current	LSTTL Fanout
Standard 74HC	4.0 mA ($V_{OUT}=3.94$)	4.0 mA ($V_{OUT}=0.33\text{V}$)	10
Bus 74HC	6.0 mA ($V_{OUT}=3.94$)	6.0 mA ($V_{OUT}=0.33\text{V}$)	15

The data sheet specifications for output current are measured at only one output voltage for either source or sink current for each of three temperature ranges, room, commercial, and military. The outputs can supply much larger currents if larger output voltages are allowed. This is shown in Figures 11, 12, 13, which plot output current versus output voltage for both N-channel sink current and P-channel source current. Both standard and bus driver outputs are shown. For example, a standard output would typically sink 20 mA with $V_{OL}=1\text{V}$, and typically capable of a short circuit current of 50 mA.



(a)

FIGURE 11. Typical P-Channel Output Source Current vs. Output Voltage for (a) Standard Outputs



(b)

FIGURE 12. Typical P-Channel Output Source Current vs. Output Voltage for (b) Bus Outputs

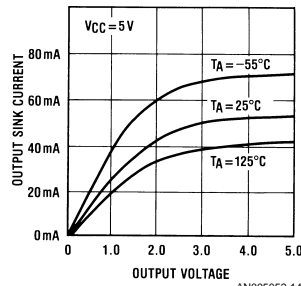
The output current and voltage characteristics of a logic circuit determine how well that circuit will switch its output when driving capacitive loads and transmission lines. The more current available, the faster the load can be switched. In order for HC-CMOS to achieve LSTTL performance, the outputs should have characteristics similar to LSTTL. This similarity is illustrated in Figure 11 by plotted typical LSTTL and HC-CMOS output characteristics together.

As the supply voltage is decreased, the output currents will decrease. Figure 17 plots the output sink current versus power supply voltage with a 0.4V output voltage, and Figure 18 plots output source current against power supply with an output voltage of $V_{CC}-0.8V$. It is interesting to note that MM74HC powered at $V_{CC}=3V$, typically, will still drive 10 LSTTL inputs ($T=25^{\circ}C$).

Absolute Maximum Ratings

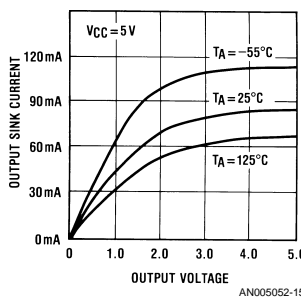
Absolute maximum ratings are a set of guidelines that define the limits of operation for the MM74HC logic devices. To exceed these ratings could cause a device to malfunction and permanently damage itself. These limits are tabulated in Table III, and their reasons for existing are discussed below.

The largest power supply voltage that should be applied to a device is 7V. If larger voltages are applied, the transistors will breakdown, or “punch through”. The smallest voltage that should be applied to a MM74HC circuit is $-0.5V$. If more negative voltages are applied, a substrate diode would become forward biased. In both cases large currents could flow, damaging the device.



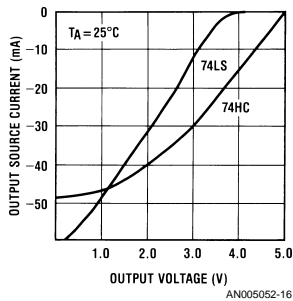
(a)

FIGURE 13. Typical N-Channel Output Sink Current vs. Output Voltage for (a) Standard Outputs



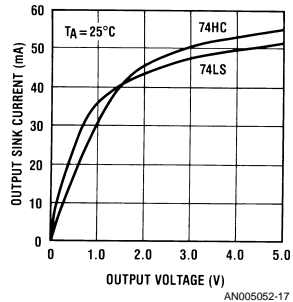
(b)

FIGURE 14. Typical N-Channel Output Sink Current vs. Output Voltage for (b) Bus Outputs



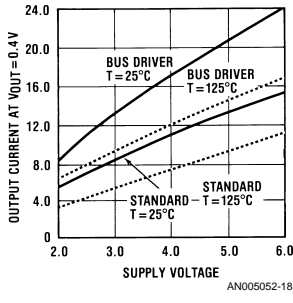
(a)

FIGURE 15. Comparison of Standard LSTTL and HC-CMOS Output (a) Source Currents



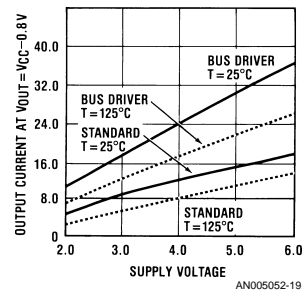
(b)

FIGURE 16. Comparison of Standard LSTTL and HC-CMOS Output Sink Currents



(a)

FIGURE 17. Output (a) Sink Current Variation with Power Supply



(b)

FIGURE 18. Output (b) Source Current Variation with Power Supply

High-speed CMOS inputs should not have DC voltages applied to them that exceed V_{CC} or go below ground by more than 1.5V. To do so would forward bias input protection diodes excessive currents which may damage them. In actuality the diodes are specified to withstand 20 mA current. Thus the input voltage can exceed 1.5V if the designer limits his input current to less than 20 mA. The output voltages should be restricted to no less than $-0.5V$ and no greater than $V_{CC}+0.5V$, or the current must be limited to 20 mA. The same limitations on the input diodes apply to the outputs as well. This includes both standard and 3-STATE outputs. These are DC current restrictions. In normal high speed systems, line ringing and power supply spiking unavoidably cause the inputs or outputs to glitch above these limits. This will not damage these diodes or internal circuitry. The diodes have been specifically designed to withstand momentary transient currents that would normally occur in high speed systems.

Additionally, there is a maximum rating on the DC output or supply currents as shown in Table 3. This is a restriction dictated by the current capability of the integrated circuit metal traces. Again this is a DC specification and it is expected that during switching transients the output and supply currents could exceed these specifications by several times these numbers.

For most CD4000 and MM74C CMOS operating at $V_{CC}=5V$, the designer does not need to worry about excessive output currents, since the output transistors usually cannot source or sink enough current to stress the metal or dissipate excessive amounts of power. The high-speed CMOS devices do have much improved output characteristics, so care should be exercised to ensure that they do not draw excessive currents for long durations, i.e., greater than 0.1 seconds. It is also important to ensure that internal dissipation of a circuit does not exceed the package power dissipation. This will usually only occur when driving large currents into small resistive loads.

TABLE 3. Absolute Maximum Ratings for MM74HC CMOS Logic

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to 7.0	V
V_{IN}	DC Input Voltage	-1.5 to $V_{CC}+1.5$	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC}+0.5$	V
I_{OUT}	DC Current, Per Output Pin	Standard	±25 mA
		Bus Driver	±35 mA

TABLE 3. Absolute Maximum Ratings for MM74HC CMOS Logic (Continued)

Symbol	Parameter	Value	Unit	
I_{CC}	DC V_{CC} or Ground Current	Standard	± 50	mA
		Bus Driver	± 70	mA
I_{IK}, I_{OK}	Input or Output Diode Current	± 20	mA	

MM74HC Input Protection

As with any circuits designed with MOS transistors "HC" logic must be protected against damage due to excessive electrostatic discharges, which can sometimes occur during handling and assembly procedures. If no protection were provided, large static voltages appearing across any two pins of a MOS IC could cause damage. However, the new input protection which takes full advantage of the "HC" silicon-gate process has been carefully designed to reduce the susceptibility of these high-speed CMOS circuits to oxide rupture due to large static voltages. In conjunction with the input protection, the output parasitic diodes also protect the circuit from large static voltages occurring between any input, output, or supply pin.

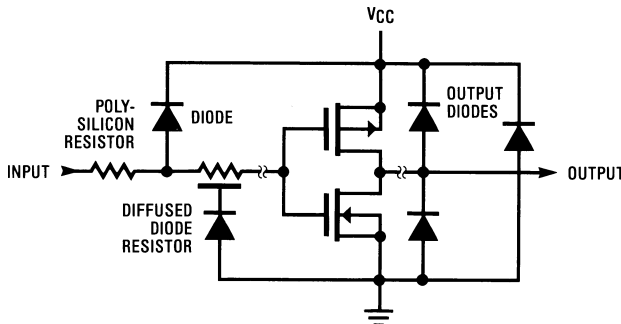
Figure 19 shows a schematic of the input protection network employed. The network consists of three elements: a poly-silicon resistor, a diode connected to V_{CC} , and a distributed diode-resistor connected to ground. This high-speed process utilizes the poly resistor to more effectively isolate the input diodes than the diode-resistor used in metal-gate CMOS. This resistor will slow down incoming transients and dissipate some of their energy. Connected to the resistor are the two diodes which clamp the input spike and

prevent large voltages from appearing across the transistor. These diodes are larger than those used in metal-gate CMOS to enable greater current shunting and make them less susceptible to damage. The input network is ringed by V_{CC} and ground diffusions, which prevent substrate currents caused by these transients from affecting other circuitry.

The parasitic output diodes (Figure 19) that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents, preventing damage to other parts of the circuit.

Summary

The MM74HC, because of many process enhancements, does provide a combination of features from 74LS and metal-gate CMOS logic families. High-speed CMOS gives the designer increased flexibility in power supply range over LSTTL, much larger output drive than CMOS has previously had, wider noise immunity than 74LS, and low CMOS power consumption.



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FIGURE 19. Schematic Diagram of Input and Output Protection Structures

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