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# Embedded IEEE 1149.1 Test Application Example

Fairchild Semiconductor
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This application example discusses the implementation of embedded, system level boundary scan test within an actual design, the Fairchild boundary scan demonstration system. Its intent is to describe the decisions, actions and results when applying boundary scan and Fairchild's SCAN EASE Software within a system. For more information see also AN-1022, "Boundary Scan Silicon and Software Enable System Level Embedded Test."

## HARDWARE DESCRIPTION

The Fairchild boundary scan demonstration system is comprised of a multidrop backplane which interconnects a processor card to several system I/O cards. The backplane contains a 16-bit data bus, a 16-bit address bus and several control signals routed to six connectors. The processor card consists of a processor core which includes a Motorola 68302 µP, boot EPROM and working SRAM, a RS232 port for remote communication, a parallel backplane interface and an auxiliary parallel port. The I/O cards, each sharing an identical architecture, include a 16-bit LCD display, an on board EPROM which stores LCD messages, and a backplane interface. Each I/O card also contains logic which multiplexes data, from either the backplane or EPROM, to the display.

The number of I/O cards can vary within a given system. While five backplane I/O card connectors are available, only 2 of the 5 slots are typically populated with I/O cards. The multidrop (i.e. parallel) backplane architecture enables cards to populate any of the five connectors and allows connectors to remain empty. Board addressing is used to select cards for functional operation.

Functionally, the system is designed to display messages and system status information using the LCD display located on each I/O card. This message and status information is driven from the processor card, via the system backplane, or from EPROMs local to each I/O card. To demonstrate the features and functions of boundary scan, the system also contains LEDs which display the status of boundary scan activity.

## TEST OBJECTIVES

The fundamental test objective for the Fairchild demonstration system was to utilize techniques which could be applied over the life of the product, including development, manufacturing and in-field operation. With effective prototyping to ensure functionality and timing performance, printed circuit board (PCB) structural faults, resulting from manufacturing errors or in-system board stress (e.g., temperature changes or mechanical stresses), were the primary focus. Boundary scan was seen as an effective means of detecting and diagnosing printed circuit board failures at all stages of the product's life cycle.

A specific area of concern during the development of the test strategy was system level test. Typically, limited tester access forces system test to rely on functional patterns to test for even simple interconnect failures. This leads to very complex test patterns, poor fault coverage and very difficult failure diagnostics. More importantly, the functional test routines depend on sound interconnects between components to be effective. Embedded, system-level boundary scan was perceived as a way to replace many of the functional tests with simple and easily diagnosable tests.

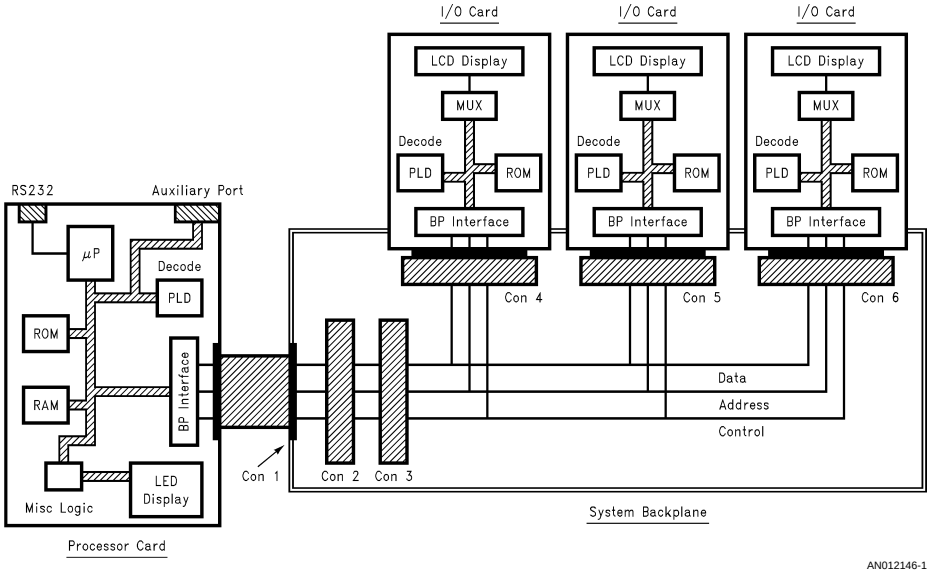


**FIGURE 1. Demonstration System Layout**



 

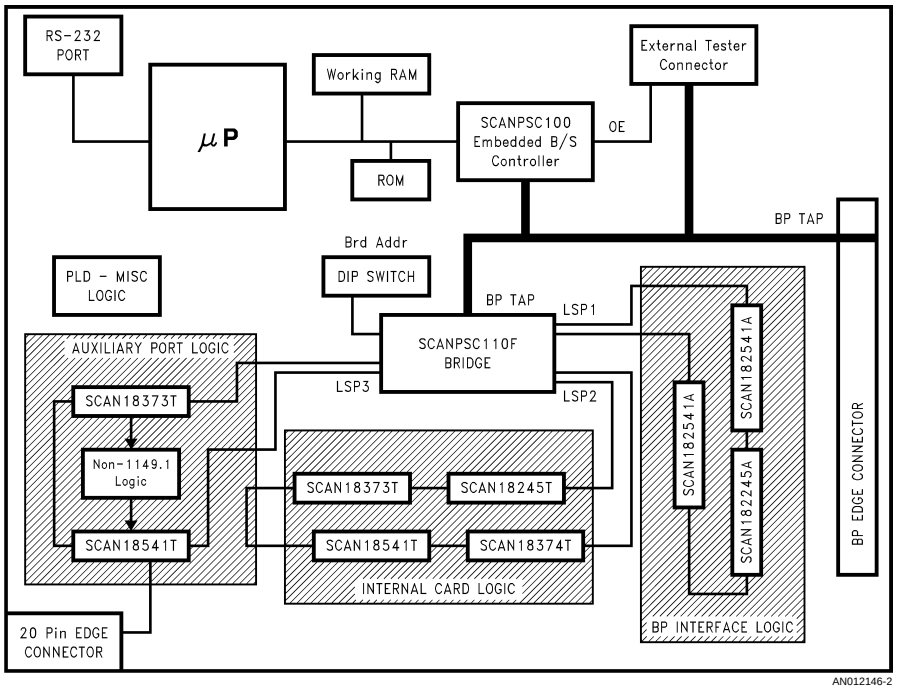


**FIGURE 2. Demonstration Processor Card**

Boundary scan was viewed as only a part of the complete test solution. Functional test routines were still required to test system memory and confirm effective µP-to-system peripheral communication. Using the two techniques together maximized test effectiveness while reducing test development efforts.

### IEEE 1149.1 COMPLIANT SYSTEM ARCHITECTURE

To accomplish the boundary scan test objectives, the 1149.1 test strategy covered three aspects of the system: board and backplane boundary scan test points, system level boundary scan access and embedded boundary scan control.

#### Board and Backplane Test Points

The first step in implementing boundary scan is to integrate 1149.1 compliant components into the functional design. Maximizing the percentage of nets covered by boundary scan reduces the cost of other techniques and equipment like in-circuit testers, while increasing the ability to apply the benefits of boundary scan at later phases of the product's life cycle. In the case of the Fairchild demo system, boundary scan was included on nearly every logic IC which populated the processor card and I/O cards.

To support backplane interconnect testing, Fairchild's 18-bit SCAN ABT Test Access Logic components were implemented at the backplane interface on both the processor card and I/O cards. Using 1149.1 compliant SCAN ABT logic (SCAN182245A) provided the required backplane test points while also creating a hot insertable (Note 1) backplane interface. The hot insertable interface allowed failing processor or I/O cards to be removed or inserted without powering down the system.

To increase the structural fault coverage on nets connected to devices which are not available with boundary scan, a "cluster test" can be implemented. A cluster test relies on at least two boundary scan components and a functional knowledge of the cluster (i.e., cluster of devices) connected between them. Using one 1149.1 compliant component to drive test vectors to the cluster and the other to receive expected data from the cluster, the structural integrity of the cluster can be evaluated.

As the number and complexity of components increases, the development of test vectors becomes more difficult and diagnostic resolution increases. Within the demo system, a cluster test was implemented on the processor card's auxiliary port (see *Figure 2* ).

On future demo design revisions, boundary scan will be expanded beyond the logic components to include an 1149.1 compliant microprocessor and programmable device (i.e., integrating the separate, non-1149.1 programmable devices into a single 1149.1 FPGA or CPLD). These additions will continue to drive the structural fault coverage towards 100% and also provide non-test capabilities, such as µP emulation and in-system FPGA programming via the JTAG port.

**Note 1:** Fairchild's SCAN ABT 18-bit boundary scan like SCAN182245A devices provide level II hot insertion. Level II insertion insures that the components can be inserted into a powered on system without component damage. See the SCAN182245A datasheet for more information on power-up reset and definition of Level 1, 2, 3 live insertion.

#### System Level Boundary Scan Access and Partitioning

With the 1149.1 components placed on the processor and I/O cards, the next objective is to interconnect the 1149.1 component TAP signals—TMS, TCK, TDI, TDO and

TRST—at both the board and system levels. For the Fairchild demo design, this task was accomplished by adding a 5-bit bus to the backplane design and placing a Fairchild Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F bridge, component at the backplane interface of the processor card and each I/O card. The SCANPSC110F bridge provides two key features to efficiently interconnect and partition a 1149.1 compliant system:

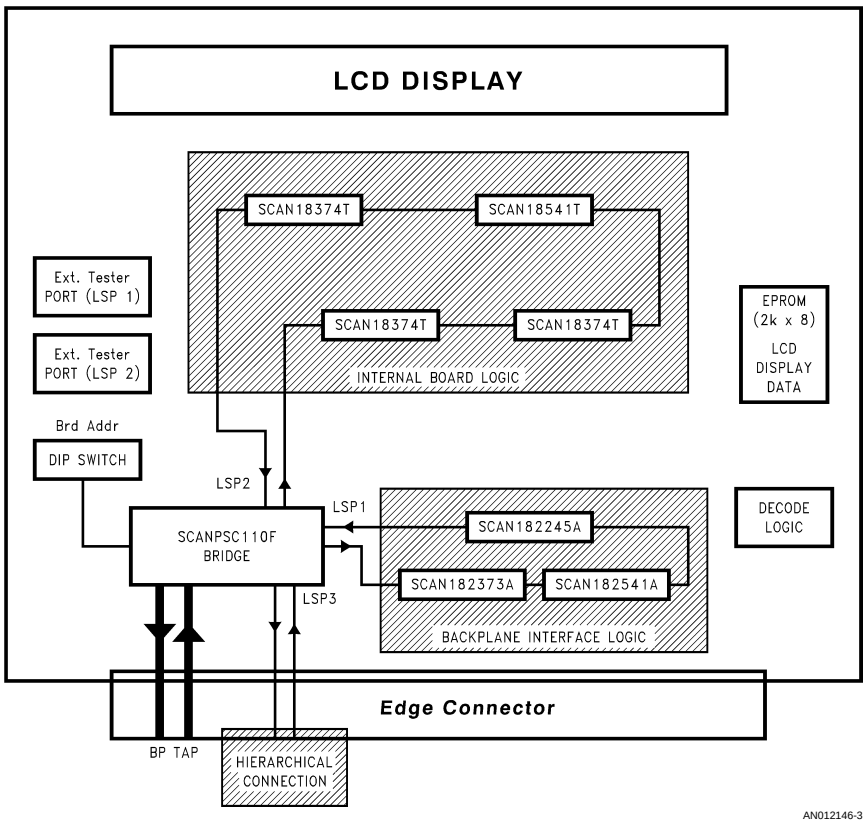


**FIGURE 3. Demonstration I/O Card**

- **System Level Partitioning:** The SCANPSC110F bridge provides an addressable, multidrop interface to a single backplane TAP bus. This multidrop TAP interface is a perfect fit for this application because it preserves the ability for cards to be placed in any of the backplane connectors and for connectors to be left empty without requiring an entirely new set of boundary scan test vectors. Using a 1149.1 protocol, each SCANPSC110F bridge and, in turn, each board, can be addressed to participate in boundary scan test operations.
- **Board Level Partitioning:** Typically, board level boundary scan components are connected to form a single chain. The SCANPSC110F bridge provides three local scan ports (LSPs) which allows board level components to be partitioned into smaller, more manageable chains. Using the SCANPSC110F bridge's internal data registers, the LSPs can be configured to individually connect a single scan chain to the backplane TAP or to simultaneously connect up to three scan chains in series with the backplane TAP.

The ability to partition a board and system using the SCANPSC110F bridge simplifies test development, improves test efficiency and allows failures to be diagnosed to the partition level without using an off-line diagnostics tool. However, these benefits are only realized if the 1149.1 components are intelligently grouped and connected. The objective for testing the demo system was to test each board as a separate entity and to test the interconnects between the boards (i.e., the backplane). Enabling each board to be tested separately was easily accomplished when the SCANPSC110F bridge was placed at each card's backplane interface and connected to a system wide backplane TAP. With this interface, the tester TAP signals could be applied to each board separately.

With exclusive access to each board, the next critical task was to select which board components were grouped and connected to the SCANPSC110F bridge LSPs. Again, the test objectives were considered. To enable the development of an efficient, backplane specific boundary scan test, the 1149.1 compliant backplane interface components on each card were exclusively assigned to a single LSP. To group and assign the remaining 1149.1 compliant, board-level components to the other two SCANPSC110F bridge LSPs, each board type was viewed separately.

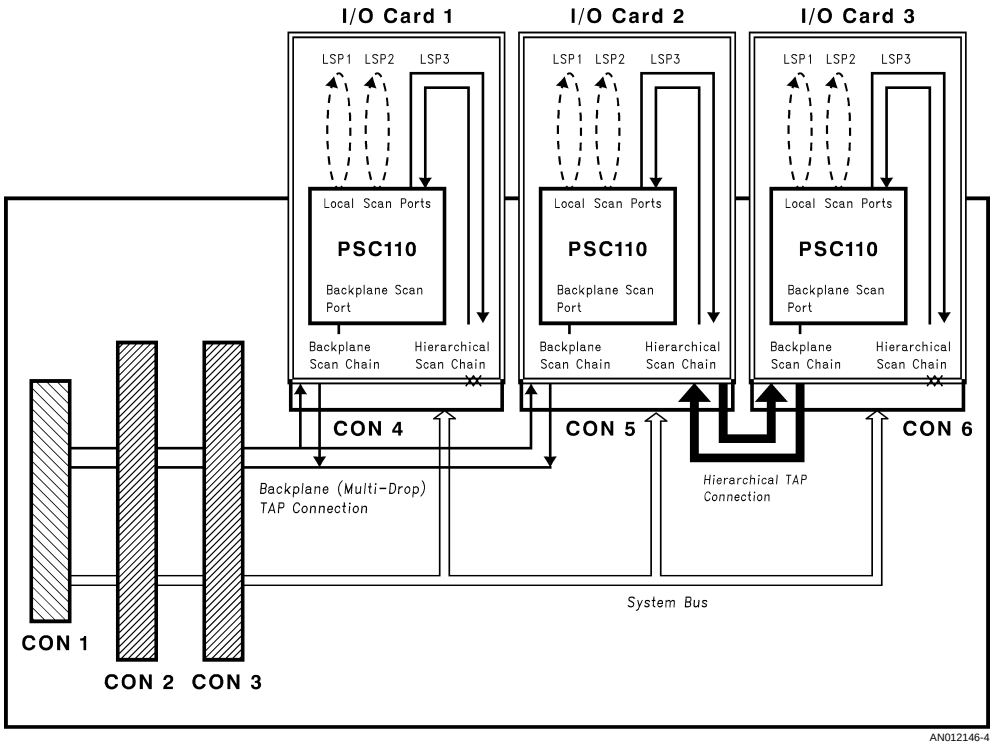


**FIGURE 4. Backplane—Hierarchical Connection**

For the processor cards, the remaining compliant components were grouped an an internal logic chain and an auxiliary port logic chain. As with the backplane partition, these groups were selected to enable the development of group specific tests. The auxiliary port is intended to support a connection to a 1149.1 compliant sub-system. Assigning the port's compliant components to a unique LSP allows tests to be generated specifically for this port (and what is connected to it). The internal logic covers all other board level 1149.1 compliant components.

A similar component group was implemented for each I/O card. The internal card logic was grouped and assigned to one LSP while the other LSP was connected directly back to the backplane connector in order to provide a hierarchical connection. A hierarchical bridge connection is realized by connecting one SCANPSC110F bridge's LSP to a second SCANPSC110F bridge's backplane interface TAP. Hierarchical connections enable board scan chains to be split into more than the three chains supported by a single bridge. Hierarchical connections also enable a system to be partitioned into addressable sub-systems. In the case of the demonstration design, the hierarchical configuration was implemented to show the concept and addressing scheme required to address a bridge and its LSPs hierarchically. Since each I/O card shares an identical architecture, each I/O card's LSP3 connects directly to the backplane edge connector. The hierarchical connection is then realized using backplane routing between Con 5 and Con 6 (see *Figure 4* ).

**Embedded Boundary Scan Test Control**

The final step of a boundary scan hardware design is to provide the means to apply and evaluate the boundary scan test vectors. For boards and systems which are tested using an external tester, the hardware implementation simply involves adding an applicable tester interface; e.g., additional pins on the edge connector, a special purpose connector/header or vias for ICT probes. For boards and systems which don't permit physical access, and/or require self-test or remote test capability, the test control must be embedded within the system.

For designs which require embedded test control, the optimal hardware implementation is one which enables both embedded and external tester access. This allows the design to benefit from the strengths of each method. The external tester offers the best means of developing tests for hardware debug and manufacturing. Using the ATPG and diagnostic tools provided with the external tester, tests can be easily developed and modified. Once the tests have been applied, failures can be diagnosed to the net or pin level automatically. With the tests finalized, and the boards/system tested, the tests and control are embedded to provide self-test and remote test access capability.

The Fairchild demo system hardware was designed to support both embedded and external test application. With the ability to address each demo card separately using the SCANPSC110F bridge, embedded and external access was

only required on the processor card. The processor card then acted as the master to test each card and the backplane.

- **Embedded Test:** The embedded test capability for the demo system was implemented using the processor card's µP and the Fairchild SCANPSC100F Embedded Boundary Scan Controller. The SCANPSC100F provides an efficient, asynchronous interface between the µP's parallel data bus and the serial 1149.1 TAP, and is fully supported by the SCAN EASE software tools. The generic, asynchronous interface allows SCANPSC100F to interface with a wide range of processors and operate independent of the processor's operating frequency. The microprocessor views the SCANPSC100F as a standard I/O device. The processor card provided two options to initiate and evaluate embedded tests. For a power-on or post-reset self test, an LED display block was included with a separate LED for each card in the system. To initiate/evaluate tests remotely, the UART on the microprocessor was configured to provide an RS232 interface and an RS232 connector was added to the processor card. This remote interface also allows new tests to be downloaded and results to be uploaded.
- **External Test:** To provide system level access to an external tester, a connector was added to the processor card. In addition to the required tester signals, this connector included a sense line tied to the output enable pin on the SCANPSC100F. When the external tester was connected, the sense line was pulled high disabling the TAP pins on the SCANPSC100F. This, in turn, disabled the embedded tester and allowed the external tester, alone, to control the system TAP.

*Figure 2* shows the high level connection between the µP, SCANPSC100F and external connector.

## IEEE 1149.1 TEST EQUIPMENT

### Hardware

A wide range of 1149.1 compliant testers are commercially available, ranging from in-circuit testers to PC-AT cards. For the demo system, the requirements for the tester hardware were low cost and portability. Based on these factors, two testers were selected: the JTAG Technologies PM3705 and the Corelis 1149.1/100F PC-AT card.

The PM3705 is a portable controller box which connects to a PC's parallel I/O port. It provides two 1149.1 TAPs and connects to the demo system via a 10-pin connector. Connectors are placed on each board (per PSC110F bridge LSP) to support board level test and on the processor card to support processor card and system level test. The PM3705 was used primarily for low volume board and system level manufacturing test, and for externally driven in-field test using a laptop computer.

The Corelis 1149.1/100F PC-AT card is based on Fairchild's SCANPSC100F which provides the ideal development platform for developing and debugging SCAN EASE functions. The SCAN EASE source code can be conditionally compiled to run directly on a 1149.1/100F PC-AT card. With a connection to the demo processor card's TAP connector, SCAN EASE was developed and debugged using a commerically available ANSI C debugger.

### ATPG (Automatic Test Pattern Generation) Software Tool

Both the PM3705 and 1149.1/100F PC-AT card are supported by the JTAG Technologies ATPG tool, called VIP (Vector Interface Package). This tool automatically generates system level 1149.1 structural tests using four user-provided input files:

- **BSDL Selection File:** Boundary Scan Description Language files, which are provided by the component vendor or ASIC designer, define the specific implementation of 1149.1 features with an IC (see Fairchild SCAN Databook Section 6 Boundary Scan Design Support). With VIP, the user must create a BSDL selection file which provides the directory path to the BSDL file for each 1149.1 component included in a given test.
- **PCB Net List (in BNET Format):** A net list is automatically created by the PCB design and layout tool used to develop the PCB. The user must convert this net list format to a specific format which is read by VIP. This VIP format, called BNET, contains only the boundary scan nets. It also defines the connection of 1149.1 components in each boundary scan chain and associates a tester TAP with each chain.
- **Connection File:** This file defines the connection between each tester TAP (provided in the BNET file) and the SCANPSC110F bridges LSPs. It also defines how the SCANPSC110F bridges are connected to the backplane TAP and to each other (e.g., multidrop or hierarchical).
- **Pin Constraint File:** This file defines I/O pins in the net list which are pulled to fixed logic levels, I/O pins which must remain in the high-impedance state during a test to avoid bus contention, or system inputs which must maintain a specific logic level during a boundary scan test (e.g., a reset input pin).

### SCAN EASE Software Tools

All three of the tools within SCAN EASE were utilized to develop and test the demonstration system:

- **EmbedPrep:** This tool was used to translate test vectors from the JTAG Technologies pattern format (PAT) to Embedded Vector Format (EVF). EVF is a compacted, ATPG-independent format that is used by the other SCAN EASE tools. EmbedPrep has no dependence on system hardware and is discussed further in the Embedding the Test Vectors section.

- **EmbedCom:** The EmbedCom tool is a Windows-based GUI which provides a user-friendly interface to the embedded test system. With this GUI, system self-test is initiated, new tests are downloaded to system RAM, pass fail information is displayed and datalogs can be uploaded. The GUI allows a user to test the system with no knowledge of 1149.1 or the embedded test code.
- **EmbedTest:** This tool, provided as ANSI C source code, contains functions which communicate with the system hardware and manage the application/evaluation of test data. Three aspects of the code must be considered when integrating EmbedTest into a specific design: integrating the EmbedTest functions with the application's operating system and system application code; mapping the SCANPSC100F addresses within the system; and implementing the drivers to support the µP specific UART (if serial communication with the EmbedTest code is required).

EmbedTest was written as multi-level modules. These levels range from the SCANPSC100F device drivers to a module called PG__CTRL which oversees the execution of tests and initialization of the test hardware. Integration with the system's operating system and application code is performed at the program control level. For the demo system, no operating system was implemented. A simple boot up routine was implemented to initialize the processor card hardware and run EmbedTest. A self-test was run immediately after power up (or after a manual system reset button was pressed), then the system polled the RS232 port for further instruction.

EmbedTest includes three device driver options for mapping the SCANPSC100F. Two of the three drivers, the PSC100F in a memory mapped architecture and the PSC100 in an I/O mapped architecture, were included to ensure that the SCANPSC100F could be implemented with any commercially available microprocessor. For the demo, a Motorola 68K µP was used and, therefore, the memory mapped driver was selected. EmbedTest uses a conditionally defined macro to allow the user to easily specify the driver option.

The third SCANPSC100F driver option was written to support the application of EmbedTest using the SCANPSC100F-based Corelis 1149.1/100F PC-AT card. The demo system was used extensively in the development of the SCAN EASE tools. The Corelis 1149.1/100F PC-AT card enabled the majority of code development to occur on a PC using an ANSI-C debugger. Debugging modifications, prior to embedding the code within the system, minimized the time required to program a new EPROM each time a change to the code was made.

The final aspect of EmbedTest is the serial communication code. EmbedTest includes two modules which support serial communication. The highest level module interprets the commands entered using the EmbedCom GUI or generic emulator, and calls the appropriate EmbedTest application functions. The other, lower level, module is a UART specific device driver. For the demo, this device driver was specific to the Motorola 68K RS232 UART. The device driver configures and controls the UART hardware.

## TEST DEVELOPMENT

### Developing Test Vectors

In a previous section, the concept and benefit of system/board test partitioning was discussed. With the partitions defined in hardware, the next step is to develop tests corresponding to each partition. For the Fairchild demo application, separate tests were developed using the JTAG ATPG tool for each card and for the backplane. When applying embedded tests using SCAN EASE, each test is applied and evaluated separately. This enables SCAN EASE to provide pass/fail results for each test. For the demo, this level of resolution was enough to allow boards to be replaced and then fully diagnosed later using an external tester.

- **I/O Card:** Since all I/O cards share identical boundary scan configurations, generating tests to cover every I/O card required only one BNET file, one BSDL selection file and one constraint file. A unique Connection File was then created for each I/O card to provide the SCANPSC110F bridge address and LSP configuration. Samples of these files are shown in *Figure 5* through *Figure 8*.

  **Internal Logic:** The internal logic boundary scan test verifies the structural integrity of boundary scan nets within each I/O card. Some nets are shared between the internal logic chain (LSP2) and the backplane interface logic chain (LSP1). To access these shared nets, SCANPSC110F bridge is configured in the connection file to serially connect LSP1 and LSP2. The ATPG then views the LSP1 and LSP2 chains as a single chain and generates tests accordingly.

```
DESIGN S4A2_ABT

CHAIN               TAP1
  TCK               TCKL1
  TDI               TDIL1
  TDO               TDOL1
  TMS               TMSL1
  TRST              -
    IC_LIST
      U27           SCAN182245A
      U31           SCAN182541A
      U29           SCAN182373A
    END_IC_LIST
END_CHAIN

CHAIN               TAP2
  TCK               TCKL2
  TDI               TDIL2
  TDO               TDOL2
  TMS               TMSL2
  TRST              -
    IC_LIST
      U10           SCAN18541T
      U16           SCAN18374T
      U23           SCAN18374T
      U22           SCAN18374T
    END_IC_LIST
END_CHAIN
```

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```
!PARRALLEL_CONNECTOR_LIST
!END_PARRALLEL_CONNECTOR_LIST

NETLIST
!NETname      ICname     PINnumber;
ADDIS0        U16        42
              U23         2
              U23        15;
ADDIS1        U16        41
              U23         4
              U23        16;
ADDIS2        U16        39
              U23         5
              U23        18;
ADDIS3        U16        38
              U23         7
              U23        19;
ADDIS4        U16        36
              U23         8
              U23        21;
ADDIS5        U16        35
              U23        10
              U23        22;
```

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**FIGURE 5. Sample BNET File**

```
SYNTAX_VERSION 1.2
DESIGN IO_INT_2
REVISION UNKNOWN

TESTER_CHANNEL TAP1

! Board address is
! decimal 2 (00000010)
! The address is the only
! item that changes
! when creating internal
! net test for each I/O card
! TAP1 and TAP2 chains
! defined in BNET
! FROM TESTR (PART, ADDRESS, NAME OF LSPs
1-3) CASCADE1 (PSC110F, 2, TAP1, TAP2,
NONE)
END_CHANNEL
```

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**FIGURE 6. Sample Connection File**

```
PRIMARY_IO  N;
! input tied to GND - set to sense low
OE1         S 0;
! input tied to VCC - set to sense high
DS1         S 1;
!Reset Pin - must remain high
! during test
RSTL        D 1;
```

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**FIGURE 7. Sample Constraint File**

```
! path to BSDL files for
! devices involved in test
C:\bst\bstlib\nsl82245.dsh
C:\bst\bstlib\nsl82373.dsh
C:\bst\bstlib\nsl8374.dsh
C:\bst\bstlib\nsl8541.dsh
C:\bst\bstlib\nsl82541.dsh
```

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**FIGURE 8. Sample BSDL Selection File**

**Hierarchical Board Test:** (only applies to board populating Con 6): This test verifies the same nets covered in the internal test, but includes an extra SCANPSC110F bridge device in the path between the I/O card and the backplane TAP. The extra SCANPSC110F bridge is handled in the connection file and all other input files are unchanged. The connection file is shown in *Figure 9*.

```
SYNTAX_VERSION 1.2
DESIGN hierarc
REVISION UNKNOWN

TESTER_CHANNEL TAP 1

!FROM TESTR (PART, ADDRESS, NAME OF TAPS
1-3 FOR THIS BRIDGE)
  CASCADE1 (PSC110F, 3, NONE, NONE,
  CASCADE2)
  CASCADE2 (PSC110F, 4, TAP1, TAP2, NONE)
END_CHANNEL
```

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**FIGURE 9. Hierarchical Board Connection File**

- **Processor Card:** The processor card includes boundary scan nets, but also serves as the test master for the remainder of the system. This dual role dictates that separate internal processor card tests must be created for applications with an external tester versus application with the embedded tester. When applying embedded tests, the 1149.1 components which access and evaluate the processor's local bus cannot be included in the boundary scan test. Controlling the local bus with boundary scan would prevent the processor from communicating with board resources required to apply the tests. When applying tests with an external tester, the processor communication is not required except with dynamic memory which must be refreshed. Therefore, the local bus boundary scan nets can be tested.

**Internal Logic (External Tester):** The same process used to generate the internal logic tests for the I/O card was repeated to generate tests for the I/O card's internal logic nets. A BNET was created to include the boundary scan nets including the local bus nets; the selection file was created to point to the BSDL files; a constraint file was created to force or sense specific values; and a connection file was created, in this case, including all three LSPs in the chain.

The processor card's auxiliary port logic (LSP3) contains a logic component connected between two boundary scan components. Therefore, testing the nets between these devices requires that signals pass through this component. A special list, called a cluster test, was generated to support this connection. To implement a cluster test, the user must provide a set of functional vectors for the cluster logic, in this case a single component. These functional vectors can range from a full functional vector set to only those vectors required to detect interconnect faults. For the JTAG Technologies ATPG tool, VIP, the functional patterns are passed into a post-process file called the APL file. The APL file is later compiled by the VIP tool to generate the test vectors.

**Internal Logic (Internal Tester):** This test is a sub-set of the external tester version. For the embedded test version, boundary scan device outputs which interface the processor local bus were disabled throughout the test. Forcing the boundary

scan outputs to a high impedance state was handled in the constraint file. A portion of the constraint file is shown in *Figure 10*.

```
PRIMARY_IO  N;
! input tied to GND - set to sense low
OEl         S 0;
! input tied to VCC - set to sense high
DSl         S l;
! Reset Pin - must remain high during test
RSTL        D l;
! Local bus pin - forced to high impedance
CPUD0               Z;
CPUD1               Z;
CPUD2               Z;
CPUD3               Z;
CPUD4               Z;
CPUD5               Z;
CPUD6               Z;
.
.  continues....
.
```

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**FIGURE 10. Processor Card Internal Logic Constraint File**

- **Backplane:** With tests generated for each board, the only remaining step is to develop tests to evaluate the interconnects between boards. For the JTAG Technologies VIP tool, a backplane test is viewed as just another board test. A BNET file for the boundary scan backplane nets and a connection file are created to indicate the SCANPSC110F bridges and LSPs containing components which interface these nets. In the case of the Fairchild demo, each card's backplane interface logic was connected to the SCANPSC110F bridges' LSP1. The backplane test connection file and BNET file are shown in *Figure 11* and *Figure 12*.

```
END_IC_LIST
END_CHAIN

! I/O Card 2
CHAIN                TAP3
  TCK                TCKL3
  TDI                TDIL3
  TDO                TDOL3
  TMS                TMSL3
  TRST               -
    IC_LIST
      U324           SCAN182245A
      U328           SCAN182541A
      U326           SCAN182373A
    END_IC_LIST
END_CHAIN
!PARRALLEL_CONNECTOR_LIST
!END_PARRALLEL_CONNECTOR_LIST
```

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```
NETLIST
!NETname       ICname     PINnumber;
BP_A0          U11        25
               U126       55
               U326       55;
BP_A1          U11        24
               U126       53
               U326       53;
BP_A2          U11        22
               U126       52
               U326       52;
BP_A3          U11        21
               U126       50
```

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**FIGURE 11. Backplane BNET File**

```
! Configuration file for backplane test.
!

SYNTAX_VERSION 1.2
DESIGN BCKPLN
REVISION UNKNOWN

TESTER_CHANNEL TAP1

!FROM TESTR (PART, ADDRESS, NAME OF TAPS 1-3
!FOR THIS BRIDGE)
 MULTIDROP1 (PSC110F, 1, TAP1, NONE, NONE)
!processor card
 MULTIDROP2 (PSC110F, 2, TAP2, NONE, NONE)
!I/O card 1
 MULTIDROP3 (PSC110F, 3, TAP3, NONE, NONE)
!I/O card 2

END_CHANNEL
```

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**FIGURE 12. Backplane Connection File**

### Embedding the Test Vectors

At this point, the hardware design is complete, the tests have been generated and the SCAN EASE code has been integrated into the system. The last step is to embed the test vectors into the system memory. This action requires two phases.

First, the vectors must be converted from the ATPG tool's output file format to EVF. The JTAG Technologies VIP tool generates test patterns in a unique file format, called the pattern format (PAT). To translate the PAT files into EVF files, the SCAN EASE EmbedPrep tool provides a PAT to EVF compiler. The compiler, called PAT2EVF, is an executable file which runs on a PC or workstation.

Each PAT file, representing a single test, is entered as an input to the compiler. PAT2EVF also prompts the user for infor-

mation regarding the test name, test type and date. The test name, test type and date are included in the EVF's file header, which is later used by SCAN EASE to associate pass/fail status with the specific test.

With each PAT file converted to a corresponding EVF file, the next action required is to actually embed the vectors into memory. For the demo application, an EPROM programmer was used to embed each EVF file into the processor card's EPROM (the same PROM which contained the SCAN EASE EmbedTest code). EmbedTest uses a single locate statement to point to the embedded EVF vectors. Therefore, the separate EVF files must be appended together before programming the EPROM. EmbedTest uses the file header to determine where each separate EVF file starts and ends within this single, appended EVF file.

## TEST APPLICATION AND FAILURE DIAGNOSTICS

At all stages of the demonstration system's life cycle, a combination of external and internal tests were performed. For PCB prototyping and board/system manufacturing test, an external test was applied, followed by an embedded test. For field level test, the opposite order was followed. The system was tested using the embedded tester and then, if necessary, tested using the external tester. The order of testing was dependent on the number of failures expected and the ability to diagnose failures with the embedded versus external test methods.

During prototyping and manufacturing, each PCB (cards and backplane) is tested for the first time. Therefore, these stages have the highest occurrence of PCB interconnect failures. For the demo application, external testing provided a quick test application and access to the JTAG Technologies diagnostic tool. With this tool, boundary scan failures were diagnosed automatically to the pin and/or net level. This extremely tight resolution facilitated board repairs. Once the failures were resolved, the embedded tests were applied to confirm correct operation of the embedded test routines and to enable execution of the non-boundary scan, functional test routines.

During field level test of the demo system, the objective was to quickly confirm that the interconnects were sound and that the system was functioning. Since the system was already thoroughly tested in manufacturing, the likelihood of a failure was very low. For this reason, the embedded self-test was an ideal method of testing the system.

For most field applications, the level of field test resolution is at the board or sub-system level. The goal in the field is to minimize system down time. If a failure is found, the board or sub-system is removed, replaced and retested. Depending on the cost, the board or sub-system is discarded or sent back to a repair depot. A similar goal was used for the demo system. With a separate test for each demo card and for the backplane, SCAN EASE was able to provide pass/fail diagnostics to the card/backplane level. If a failure was found, three options were available:

- **Card Removal:** The most simple option was to replace the card with a spare and diagnose the failure at the factory using an external tester.
- **Embedded Diagnostics:** SCAN EASE supports serial communication with the Fairchild demo system. With this link, new tests are downloaded to system RAM. These tests offer tighter diagnostic resolution than the card-level tests which are embedded in system ROM and applied during power on self-test. For example, the power on test simply shows that the card is failing. The downloaded tests may view a specific connection between devices on the card to determine which internal card connections are failing.
- **Off-line, Pin Level Diagnostics:** To provide pin level diagnostics for failing demo cards, an external tester and off-line diagnostics tool was utilized. The connection was made on the processor card to disable the embedded tester and provide access to the entire system. Since the embedded and external testers were connected at the same hardware location and since the embedded/external tests were identical, the embedded failures were repeatable on the external tester. For a system which does not provide external tester access, an alternative method of running off-line, pin level diagnostics is to use the datalogging option and serial communication capability provided with SCAN EASE to upload failing vectors to a file. This file is the converted to a format that is readable with an off-line tool.

## BOUNDARY SCAN BENEFITS REALIZED WITH THE FAIRCHILD DEMO APPLICATION

### Prototyping Boards and System

For the initial hardware debug, boundary scan proved to be a tremendous time saver. It eliminated the structural faults which are often very difficult and time consuming to debug using functional techniques. Once we were sure that the components were effectively placed on each PCB, we were able to focus our efforts on the primary objective of debugging functional and timing related problems.

### Manufacturing Process Verification

Boundary scan provided a means of testing the interconnects for the entire system. With the use of the SCANPSC110F bridge on each card, tests were applied using a single, system wide tester connector, but partitioned for each card and the backplane. Boundary scan enabled efficient failure detection, diagnosis to the pin/net level and PCB repair.

### Field Level System Test and Diagnostics

The Fairchild demonstration system is transported and presented all over the world. Therefore, the ability to test and resolve failures in the field was a key requirement of the test capability. With the ability to embed boundary scan test control within the system, the system interconnects were easily verified prior to each functional presentation. Additionally, remote access to the boundary scan vectors and test application code enabled test downloading and result evaluation to occur using a laptop computer.

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