Application Review and Comparative Evaluation of Low-Side MOSFET Drivers

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Abstract — Power MOSFETs require a gate drive circuit to translate the on/off signals from an analog or digital controller into the power signals necessary to control the MOSFET. This paper provides details of MOSFET switching action in applications with clamped inductive load, when used as a secondary synchronous rectifier, and driving pulse/gate drive transformers. Potential driver solutions including discrete and integrated driver designs are discussed. MOSFET driver datasheet current ratings are examined and circuits are presented to assist users in evaluating the performance of drivers on the lab bench.

I. INTRODUCTION

In many low to medium power applications a low-side (ground referenced) MOSFET is driven by the output pin of a PWM control IC to switch an inductive load. This solution is acceptable if the PWM output circuitry can drive the MOSFET with acceptable switching times without dissipating excessive power. As the system power requirements grow the number of switches and associated drive circuitry increases. Also, as control circuit complexity increases, it is becoming more common to omit onboard drivers because of grounding and noise problems. When the onboard driver does not offer acceptable performance (or is not included) external driver circuits are needed.

Synchronous rectifiers (SRs) are increasingly used to replace standard rectifiers when high efficiency and increased power density are important. It is common for isolated power stages delivering tens of amps to parallel two or more low resistance MOSFETs in each rectifying leg, and these devices require current pulses reaching several amps to switch the devices in the sub-100ns time frame desired. External drivers can provide these high current pulses and also provide a means to implement timing to eliminate shoot through and optimize efficiency to control the SR operation. In addition, drivers can translate logic control voltages to the most effective MOSFET drive level.

Low-side drivers are also used to drive transformers which provide isolated MOSFET gate drive circuits or to provide communication across the power supply isolation boundary. In these applications a driver is required to handle concerns specific to transformer drive as discussed later.

Low-side drivers may seem to be a mundane topic, and several papers have been written on the subject. Though often presented as an ideal voltage source that can source or sink current determined by the circuit's series impedance, the current available from a driver is in fact limited by the discrete or integrated circuit design. This topic will review the basic requirements of drivers from an application viewpoint, and then investigate methods for testing and evaluating the current capability of drivers on the lab bench.

II. CLAMPED INDUCTIVE SWITCHING

The simplified boost converter in Fig. 1 provides the schematic for a typical power circuit with a clamped inductive load. When the MOSFET Q is turned on the input voltage V_{IN} is applied across inductor L and the current ramps up in a linear fashion to store energy in the inductor. When the MOSFET turns off the inductor current flows through diode D1 and delivers energy to C_{OUT} and R_{LOAD} at voltage V_{DC}. The inductor is assumed to be large enough to maintain the current at a constant level during the switching interval.

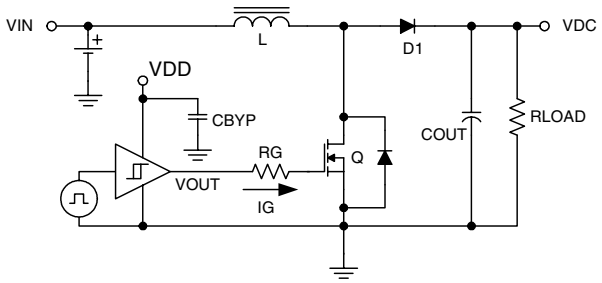

Fig. 1. Simplified boost converter

The circuit waveforms for a MOSFET that is turning on into a clamped inductive load are illustrated in Fig. 2.

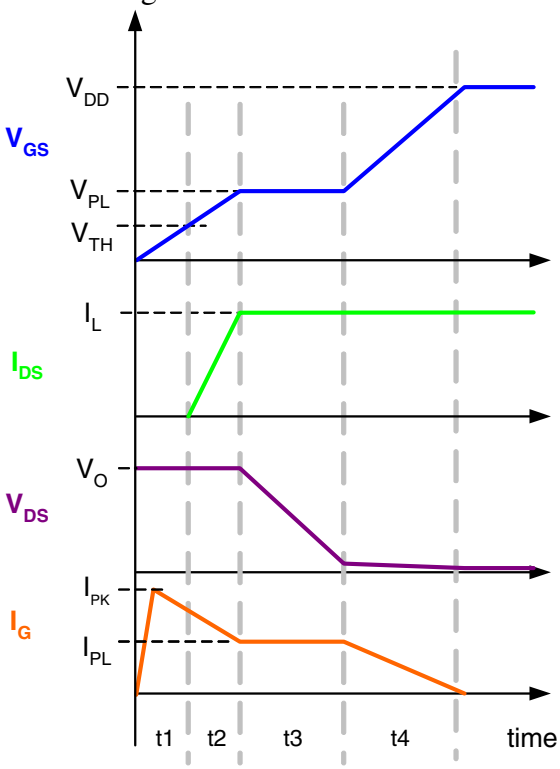

Fig. 2. MOSFET turn on with inductive load

Fig. 3 (a)-(d) indicates the gate current paths which are active during the individual intervals of the MOSFET turn on process.

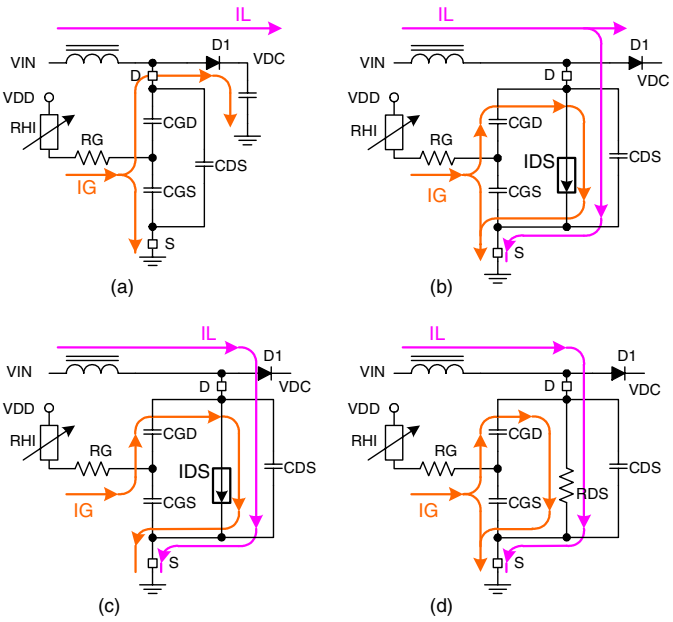

Fig. 3. Current paths during MOSFET turn on

R_G represents the series combination of the MOSFET internal gate resistance along with any series gate resistor. R_{HI} represents the driver's internal resistance whose effective value changes throughout the switching interval. As shown below, the driver current I_G can be determined by combining information presented in [1] and [2].

During interval t1 I_G increases quickly and charges the combination of C_{GS} and C_{GD} to the gate threshold voltage V_{TH} through the path shown in Fig. 3(a). In this interval the MOSFET carries no inductor current.

As interval t2 begins the MOSFET starts to conduct current in the linear mode

$$I_D = g_m (V_{GS} - V_{TH}) \quad (1)$$

through the current paths shown in Fig. 3(b). The parallel combination of C_{GD} and C_{GS} are charged from the threshold voltage to a plateau level given by

$$V_{PL} = \frac{I_D}{g_m} + V_{TH} \quad (2)$$

as the drain current rises from zero to I_L. Q_{GS2} is the charge needed during this transition and can be determined from the MOSFET datasheet characteristic curves as illustrated in the application example presented later in this section. Q_{GS2} allows us to calculate the time required for this transition as

$$t2 = T_{IDS,rise} = \frac{Q_{GS2}}{I_G}. \quad (3)$$

Throughout t2 V_{DS} remains at V_{OUT}, clamped by diode D. At the end of t2 the MOSFET conducts the full I_L current and the diode commutates.

As interval t3 commences the gate current flows through C_{GD} and the MOSFET channel as shown in Fig. 3(c). All of I_G is used to discharge C_{GD} as V_{GS} remains at V_{PL}, and V_{DS} begins to fall with a time period given by

$$t3 = T_{VDS,fall} = \frac{Q_{GD}}{I_G}. \quad (4)$$

In interval t4 I_G flows through a combination of C_{GS}, C_{GD}, and the decreasing channel resistance R_{DS} as shown in Fig. 3(d). During t4 the gate-source voltage rises from the plateau level to V_{DD}. This allows one to determine the total gate charge $Q_{G,T}$ required to turn on the MOSFET.

As the drain current rises during t2 and V_{DS} falls during t3 the MOSFET has simultaneous high voltage across it and high current flowing through it, so the instantaneous power can be very high. An equation relating I_G to the switching loss during the turn on interval is

$$P_{SW,ON} = \left(\frac{V_{IN} \times I_{LOAD}}{2}\right)(F_{SW})\left(\frac{Q_{GS2}}{I_{G,t2}} + \frac{Q_{GD}}{I_{G,t3}}\right). \quad (5)$$

This equation clearly shows the importance of the magnitude of I_G in relation to the switching losses. Unfortunately, there are no formal equations to calculate the current available from a given driver as the output voltage swings throughout its range. Empirical methods that allow users to determine the value of I_G at different driver output voltage levels will be presented in section VII.

For a practical example, the Gate-Source Voltage versus Total Gate Charge is reproduced from the Fairchild FCP20N60 power MOSFET datasheet in Fig. 4. The curve was produced using a test circuit that drives the gate of the DUT (Device Under Test) with a small current source of 3 mA. In this example, the gate charge needed to reach the threshold voltage of 3V is approximately 7 nC. The charge required during interval t2, Q_{GS2}, is found to be 14 nC – 7 nC = 7 nC. In interval t3 the value of Q_{GD} is found to be Qgd = 46 nC – 14 nC = 32 nC. In this typical case the effect of Q_{GD} on the switching loss is seen to be more significant than the contribution resulting from Q_{GS2}.

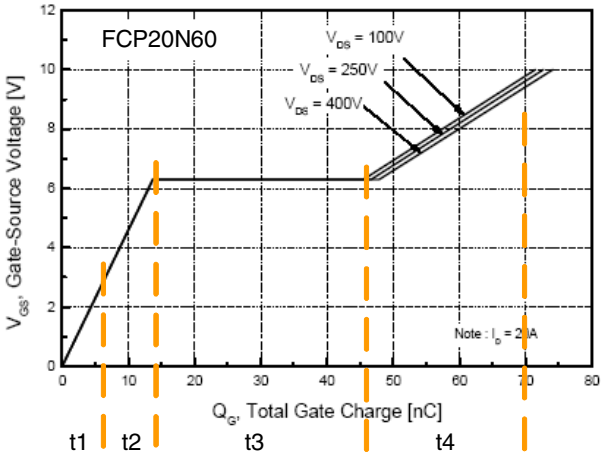

Fig. 4. Vgs versus Qg for FCP20N60

With V_{GS} at the final drive level the value for $Q_{G,total}$ is known. This allows one to find the average current required from the bias supply

$$I_{DD} = Q_G \cdot f_{SW}. \quad (6)$$

where f_{sw} is the switching frequency of the power stage. With the average current requirement known, the input power drawn from the V_{DD} bias supply can be found as

$$P_{dr} = V_{DD} \cdot I_{DD} = V_{DD} \cdot Q_G \cdot f_{SW}. \quad (7)$$

The circuit waveforms and current paths during inductive load turn off are similar to those for turn on, but taken in a reverse order. For brevity, the circuit waveforms are indicated in Fig. 5 but the current paths are not shown.

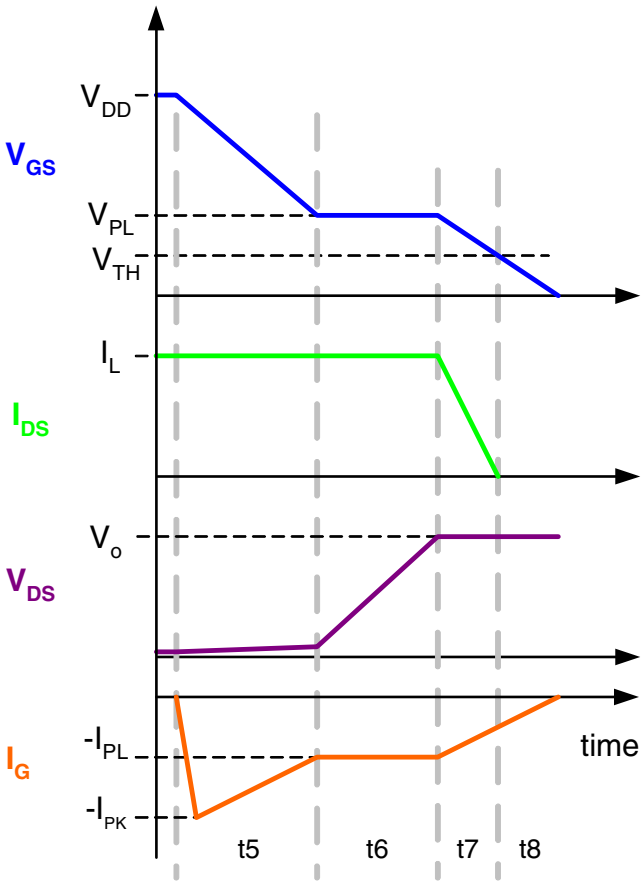

Fig. 5. MOSFET turn off with Inductive load

In the t5 interval I_G rises to discharge V_{GS} from V_{DD} to the plateau level defined by (2). In the t6 interval V_{GS} remains at the plateau voltage while V_{DS} rises to the off state voltage. The t6 interval lasts for a time approximated by

$$t6 = T_{VDS,rise} = \frac{Q_{GD}}{I_G}. \quad (8)$$

In interval t7 the drain current I_{DS} falls from the value of I_L to 0 while V_{GS} falls from V_{PL} to V_{TH}. This time interval is given by

$$t7 = T_{IDS,fall} = \frac{Q_{GS,2}}{I_G}. \quad (9)$$

In the t8 interval V_{GS} is discharged from the threshold voltage to zero.

An equation relating I_G to the switching loss during the turn off interval is given as

$$P_{SW.OFF} = \left(\frac{V_{IN} \times I_{LOAD}}{2}\right) \cdot (F_{SW}) \cdot \left(\frac{Q_{GD}}{I_{G,t6}} + \frac{Q_{GS2}}{I_{G,t7}}\right). \quad (10)$$

III. Synchronous Rectifier Operation

A MOSFET operated as a synchronous rectifier (SR) experiences a switching interval that is significantly different from the case of a clamped inductive load. Fig. 6 shows a simplified forward converter power stage with a synchronous rectifier Q_{SR} in place of the freewheel diode.

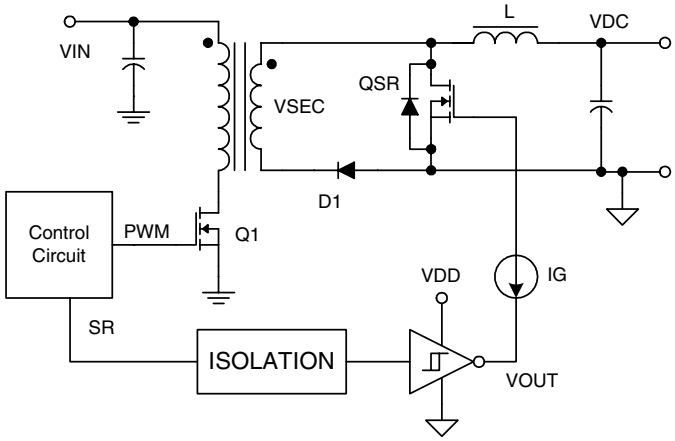

Fig. 6. Simplified forward converter

In this example an SR signal generated by the control circuit crosses the isolation boundary to keep the synchronous rectifier Q_{SR} on while Q1 is off. However, the SR signal should command Q_{SR} to turn off before Q1 turns on to apply positive voltage to the transformer. Figure 7 shows four intervals that are used to illustrate the turn off sequence of the synchronous rectifier.

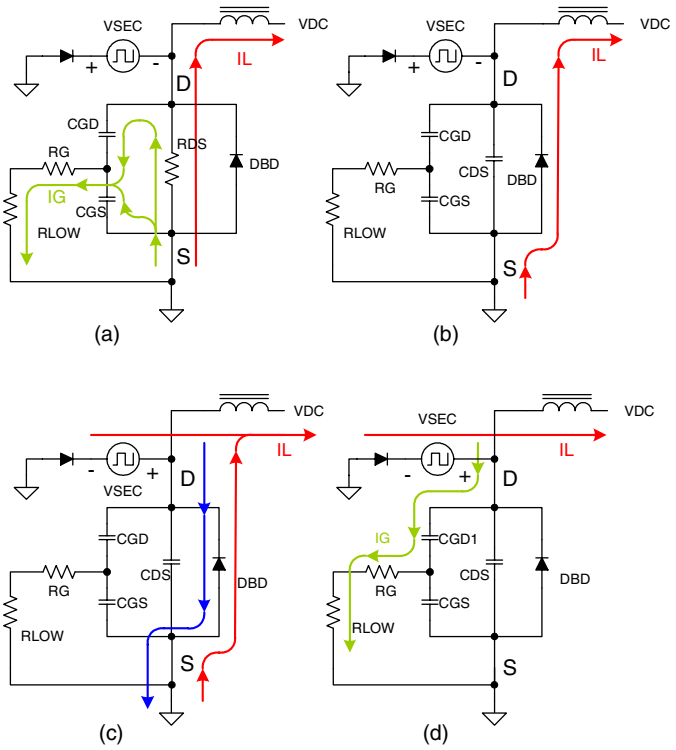

Fig. 7. SR MOSFET turn off

Prior to turn off the MOSFET conducts load current I_L through the resistive channel R_{DS} and the drain to source voltage is negative. In Fig. 7(a) the output of the driver is low and the combination of C_{GD} and C_{GS} are discharged in parallel in a time interval given by

$$t_{off} = \frac{Q_{Q,SR}}{I_G}, \tag{11}$$

where Q_{QSR} is defined in [3] to be

$$Q_{Q,SR} = (C_{GS} + C_{GD,SR}) \cdot V_{DD}. \tag{12}$$

Also in [3] $C_{GS,SR}$ is estimated as

$$C_{GD,SR} = 2 \cdot C_{RSS,SPEC} \cdot \sqrt{\frac{V_{DS,SPEC}}{0.5 \cdot V_{DD}}}. \tag{13}$$

From standard MOSFET nomenclature

$$C_{GS} = C_{ISS} - C_{RSS}. \tag{14}$$

In Fig. 7(b) the MOSFET is fully off and I_L flows through the body diode and the V_{SEC} polarity has not changed. When V_{SEC} changes polarity as shown in Fig. 7(c) current flows from V_{SEC} to recover the body diode stored charge and the diode commutates. In Fig. 7(d) the body diode has been fully recovered and V_{DS} rises quickly. The high dV/dT on the MOSFET's drain can cause a capacitive current to flow through the C_{DS}/C_{GS} voltage divider, so a driver with strong current sink capability is essential to hold the gate voltage below the threshold voltage.

In the synchronous rectifier application I_G does not affect switching losses as it did in the clamped inductive load application. However, the paralleled MOSFETS used in SR applications require high current pulses to switch them effectively, and high current drivers are often located in close proximity.

IV. Transformer Drive Applications

In power converters such as a half-bridge, full-bridge, two-switch forward converters, and active clamp forward converters there are high side switches or a combination of high/low switches that must be controlled. If galvanic isolation is not needed between the control and the power switches the MOSFETs may be driven with a semiconductor half-bridge gate driver, but the inherent propagation delay must be considered in the design. For circuits that do need isolation or can benefit from short propagation delays the venerable gate drive transformer should be considered as a potential solution.

In a related application, it is often necessary to provide high speed communication between the primary and secondary sides of an isolated converter. This can be accomplished by using technologies such as opto-isolators with digital outputs or magnetic pulse transformers. These pulse transformers are similar to the gate drive transformer but they are only required to transmit logic signals instead of delivering the high current pulses to turn a power MOSFET on and off.

The simplified circuit of Fig. 8 will be used to illustrate the basic operation of a low side driver and pulse transformer used in a communication circuit. The transformer is shown as ideal transformer with turns ratio NP:NS = 1:1 in parallel with magnetizing inductance L_{MAG}. In both cases, the dc blocking capacitor C_C is large enough so that its voltage is approximately constant.

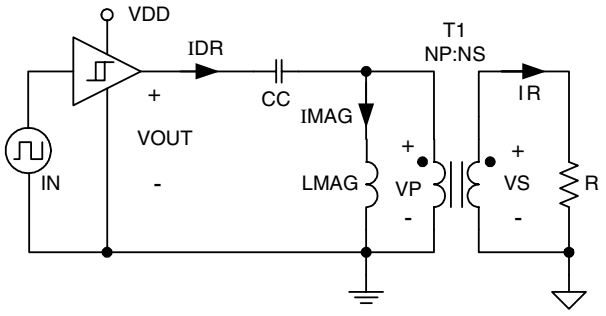

Fig. 8. Simplified pulse transformer circuit

In Fig. 9 the circuit is modified so that the resistor is replaced by the gate to source terminal of a MOSFET located on the high side of a bridge circuit.

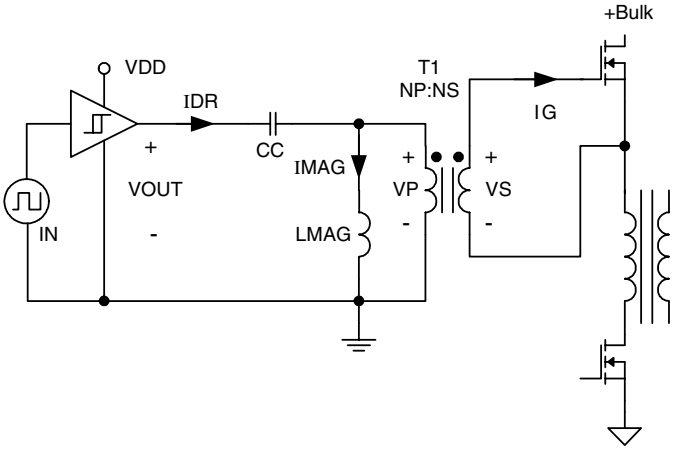

Fig. 9. Simplified gate drive transformer circuit

Fig. 10(a) shows the operational waveforms for the pulse transformer circuit while Fig. 10(b) shows operation in a gate drive application.

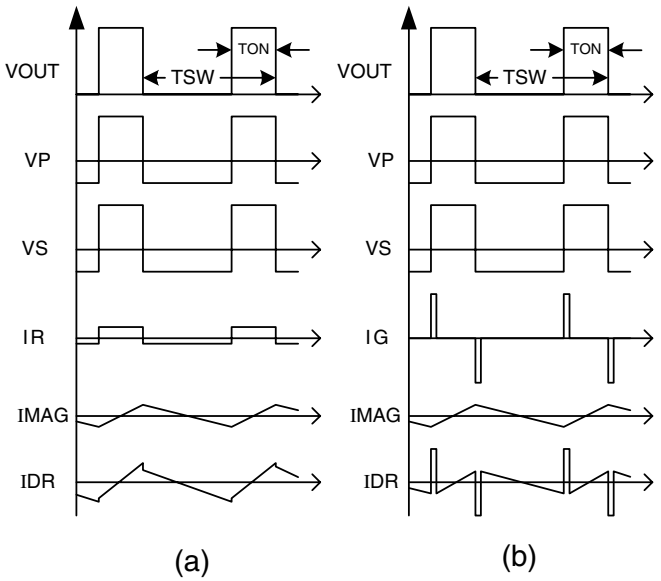

Fig. 10(a) Pulse transformer waveforms and (b) Gate drive transformer waveforms

The output of the driver swings from 0 V to V_{DD} producing a DC component equal to V_{DD} x duty cycle. If this voltage was applied directly to the primary winding of T1, the transformer would saturate and not be able to transmit useful information. To prevent this from occurring coupling capacitor C_C is inserted in series with the primary winding to block the DC voltage while passing the AC portion of the V_{OUT} signal. Transformers designed for pulse and gate drive applications usually specify a voltage-time product that the device can withstand without saturating the transformer.

In many cases the same transformer could be used as either a pulse transformer operation or a gate drive transformer. In Fig. 10 the major difference between the two applications is found in the current waveforms. With a constant drive voltage and magnetizing inductance L_{MAG} the magnetizing current I_{MAG} is the same in both circuits. In the pulse transformer waveforms shown in 10(a) the resistor current I_R follows the secondary voltage V_S, and the driver supplies a current that is the sum of these two components. In the MOSFET gate drive waveforms shown in Fig. 10(b) the gate current I_G is seen to be positive pulses at turn on and negative pulses at turn off. As in the first example

the driver supplies a current that is the sum of these two components, but the waveform has a larger RMS value due to the high current pulses.

It is important to examine the direction of current flow between driver and transformer for the examples of Fig. 10. When V_{OUT} swings high as shown Fig. 11(a), one might expect the driver to immediately source current. However, the magnetizing current is negative, and if the load current is not larger than the magnetizing current the driver must sink current until I_{DR} goes positive. The opposite situation exists in Fig. 11(b) when V_{OUT} goes from high to low and the driver must source current when expected to operate as a current sink. Figure 11(c) shows additional diodes that provide a current path if the driver cannot sink current when V_{OUT} is high or source current when V_{OUT} is low, as found in drivers with a bipolar output stage.

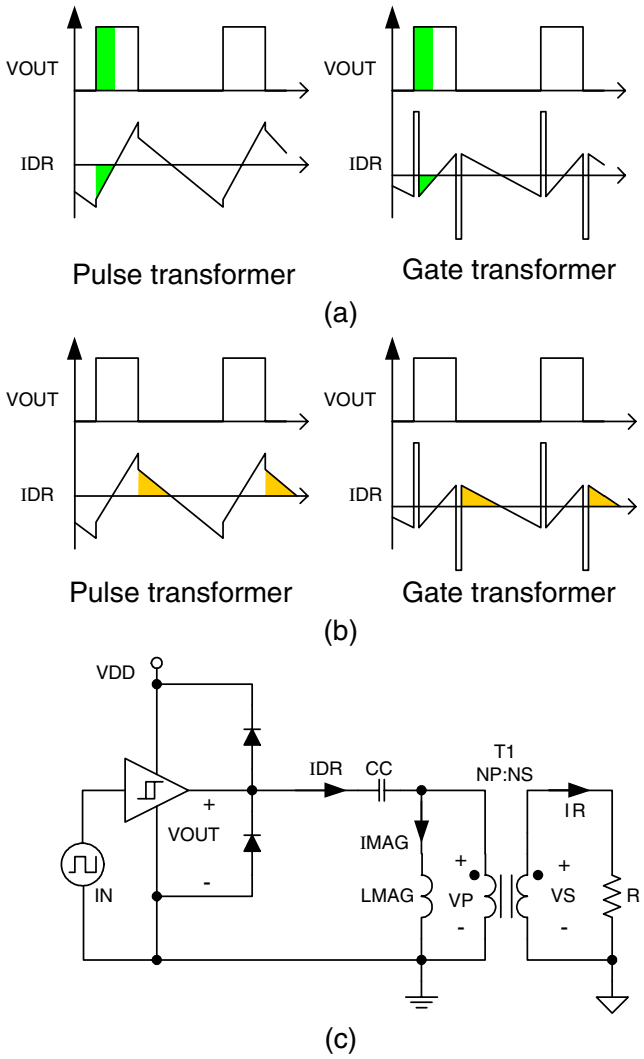

Fig. 11. Current Flow and diode clamp circuit for transformer driver

If the transformer is designed with low leakage inductance the propagation delays through the transformer can be less than 50 ns. The GT03 series of transformers from ICE Components [4] is an example of devices that have leakage inductance of a few hundred nanoHenries. This low value is obtained by using tightly coupled windings on a small ferrite core.

In the previous transformer examples the positive and negative peaks vary with duty cycle while the secondary voltage V_S swings around zero volts. In a pulse transformer application, the pulses might feed circuits that cannot accept the negative going pulses. The circuit in Fig. 12 incorporates a clamp circuit consisting of a second coupling capacitor C_{CS} and a diode which restores the DC level of the secondary

voltage.

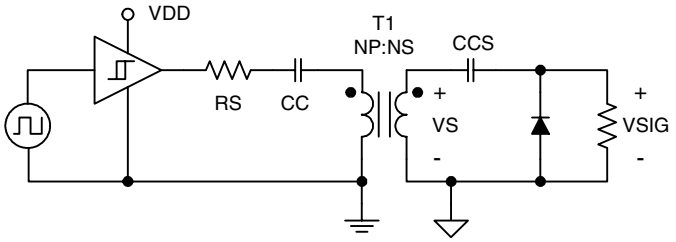

Fig. 12. Pulse transformer with DC restore circuit

Series resistor R_S serves to damp the initial transient at startup when C_{CS} is initially uncharged, and is often a discrete resistor in addition to the internal driver impedance. From classical RLC circuit theory a value of R_S for critical damping is approximately

$$R_S = 2 \cdot \sqrt{\frac{L_{MAG}}{C_{CC}}}, \qquad (15)$$

where L_{MAG} is the magnetizing inductance of the transformer.

Fig. 13 shows a gate drive application circuit that utilizes the DC restore circuit of the previous example along with some additional modifications.

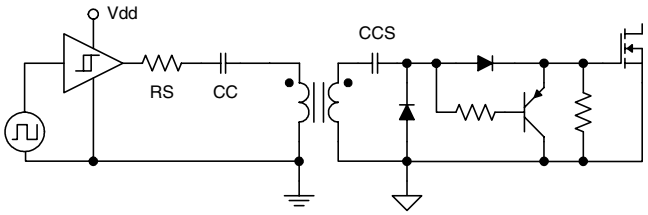

Fig. 13. Improved gate drive transformer circuit

The PNP transistor added at the gate of the MOSFET is turned on when the secondary voltage goes negative to speed up the turn off time of the MOSFET.

Reference [3] offers further information on transformer coupled gate drives, and should be consulted for detailed design methodology beyond the scope of the present topic.

V. DISCRETE OR INTEGRATED DRIVERS

External drivers can be designed using discrete transistors or by using integrated circuit solutions which come as predesigned blocks. In order to select a solution the designer must evaluate the competing size, features, cost and the overall range of applications to be covered. Regardless of the driver selection there are some common requirements. Integrated or discrete-design drivers need a local bypass capacitor to supply the high current pulses delivered during the switching intervals, and might include a resistor between the driver and the PWM supply V_{DD}. In general, drivers have the greatest impact when located close to the MOSFET gate-source connections to minimize parasitic inductance and resistance effects.

Discrete solutions can be designed using bipolar transistors as shown in Fig. 14. The NPN/PNP totem pole features a non-inverting configuration that is driven by the PWM output. This circuit prevents shoot-thru in the bipolar stage because only one of the totem pole devices can be forward biased at a time. In the bipolar common emitter configuration the driving signal must have fast edges to provide fast switching, and it should be noted that the MOSFET gate is not ohmically connected to the rail when high or low.

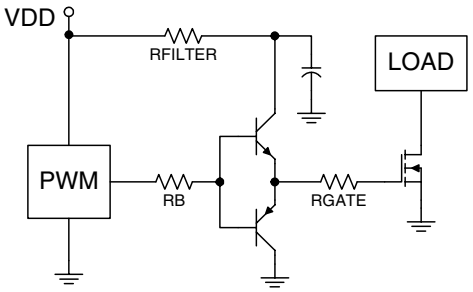

Fig. 14. Discrete bipolar transistor drive circuit

The PMOS/NMOS version shown in Fig. 15 has a natural inversion and would require an inverter to follow the PWM signal polarity. This circuit offers rail to rail operation, but shoot-thru is a problem that must be considered in design because both devices can conduct when the common gate node voltage is in the middle part of the V_{DD} range.

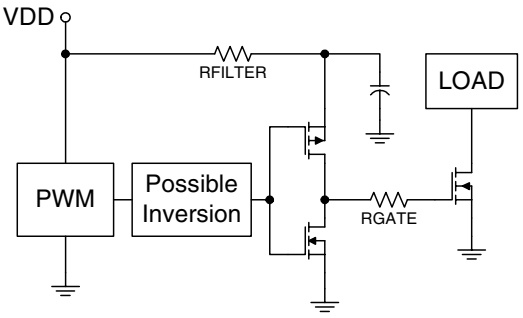

Fig. 15. Discrete PMOS/NMOS drive circuit

Using the discrete driver approach leads to a higher component count that requires more pcb board space along with more assembly and test time. The higher component count can lead to more procurement costs along with more reliability concerns. If the input signal comes from a logic circuit or a low voltage PWM the discrete driver requires additional circuitry to translate from the logic levels to power drive levels.

Integrated circuit drivers offer significant benefits in addition to large pulse current capability. New integrated dual drivers in 3x3 mm packages and single drivers in 2x2 mm packages include a thermal pad for heat removal. These devices require less board space than discrete solutions while offering enhanced thermal performance, so they are well-suited for the most dense power designs. Features integrated into the device such as an enable function and UVLO create ease of use, and less component-level design is required by users. It has been common practice to offer drivers with TTL compatible input thresholds that can accept inputs ranging from logic-level signals up to the V_{DD} range of the device. Drivers utilizing CMOS input thresholds (2/3 Vdd = high, 1/3Vdd = low) can be used to alleviate noise issues or to set more accurate timing delays at the input of the driver.

VI. Driver Datasheet Current Ratings

Driver datasheet current ratings and test conditions can lead to confusion. Many users consider the gate driver to be a near ideal voltage source that can instantly deliver current as determined by the circuit series resistance, and this is not necessarily true. Usually, the current available from a driver is limited by the internal circuit design regardless of the semiconductor technology used. This self-limiting nature should not be confused with self-protecting, however, because if a driver output is shorted high or low the device is likely to fail.

Here are some common methods used for driver datasheet current ratings:

1. Peak current available from device, usually at initial turn on at max V_{DD}
2. Current available with the output clamped at a specific voltage, often around $V_{DD}/2$
3. Current available with low value resistance to rails (perhaps 0.5 ohm, even short circuit)
4. Current measured with a current probe

Integrated MOSFET drivers are commonly available in one of three technologies, either primarily MOSFET, bipolar, or a combination of the two technologies often referred to as compound devices. The MOSFET and bipolar versions are similar to the discrete solutions previously mentioned, while the compound design combines features from both technologies.

For low-side drivers built with a MOS output state (PMOS high side and NMOS low side, similar to the discrete circuit illustrated in Fig. 15) the datasheet current rating is generally specified as the peak current available from the part, often specified with V_{DD} near the maximum rating of the part. Fig. 16 shows the output current and voltage for a 4 Amp driver using test methods detailed in section VII. This testing shows that the internal circuitry limits the peak output current to a value near the rated 4 Amps with no external resistor.

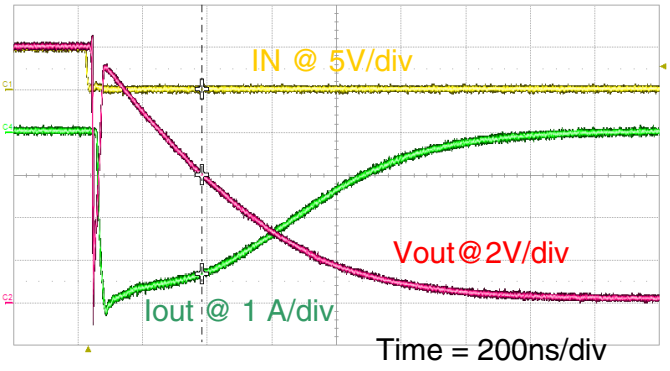

Fig. 16. PMOS/NMOS driver Vout and Iout

The PMOS/NMOS drivers usually specify the driver output resistance when it is sinking or sourcing a specified current such as 100 mA. It is interesting to note that the MOS-type driver does not attain the $R_{O,high}$ or $R_{O,low}$ resistance values immediately when the device begins switching. For example, 4 Amp drivers commonly specify a value for $R_{O,high}$ or $R_{O,low}$ from 1 ohm to 2 ohms. If the devices reached this low resistance value instantaneously the peak currents would be more than seven amps with V_{DD} = 15 V.

In compound devices, bipolar and MOSFET devices are combined in a parallel configuration such as the one shown in Fig. 17, where the power output devices are shaded. The bipolar transistors are able to deliver high sink and source current while the output voltage swings through the middle part of the output range. The PMOS and NMOS operate in parallel with the bipolar devices to pull the output voltage to the positive or negative rail as required.

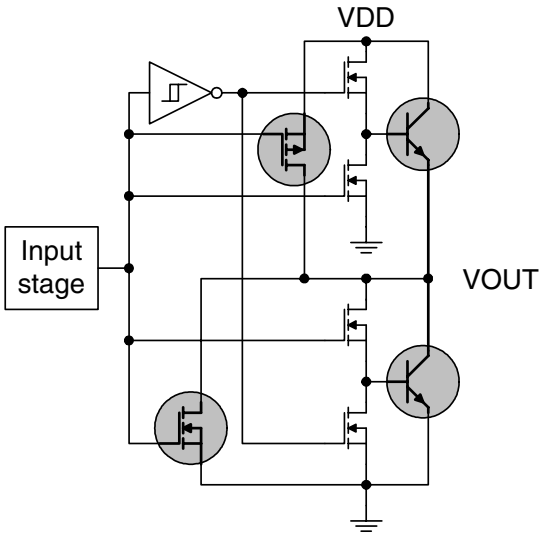

Fig. 17. Compound driver output stage

For compound drivers the output current is often specified with the output voltage at a specified voltage such as $V_{DD}/2$ to highlight the current that is available during the Miller plateau region of the V_{GS} waveform. In tests performed using the methods described in sec VII the peak output current is generally seen to be higher than the current specified at $V_{DD}/2$. Fig. 18 shows the sink current capability of a 4 Amp compound driver (FAN3224C) to be 4.76 Amps while the output is at 6.1 V, after reaching a peak just under 6 Amps. Thus, a compound driver rated at 4 Amps might deliver a higher peak current than a comparably rated PMOS/NMOS driver. This type of information is practically impossible to obtain from the driver datasheets, so specific test methods are required.

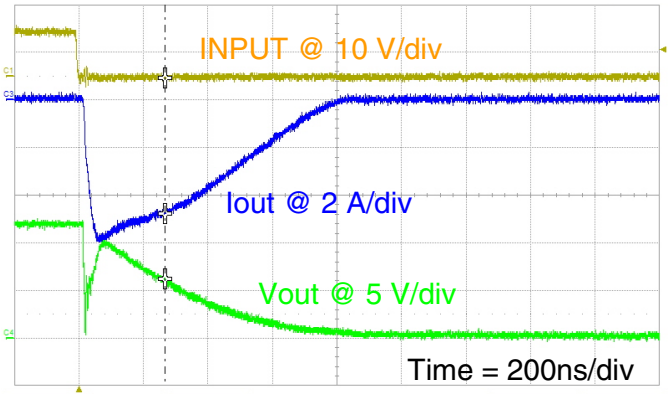

Fig. 18. Compound driver current sink waveform

VII. Evaluating Drivers on the Bench

Real-world driver comparisons are difficult to perform in the lab because the fast signal ramp rates cause complex interactions between the inductive and capacitive circuit components. These fast edge rates can introduce overshoots and undershoots of several volts, and some examples to help quantify this effect in power circuits can be found in [5]. Although the parasitic inductance varies according to specific circuit layout and ground structure, [6] gives an approximate value of 10 nH/inch (4nH/cm) for microstrip on FR-4 with the trace exposed to air on one side. This provides an estimate that can be used with the circuit capacitance to calculate a damping resistor when needed.

It is difficult to compare competing devices using only datasheets which offer information produced using different test conditions. Competing technologies used in integrated circuit solutions further complicate device comparison. In the following paragraphs several circuits that can be used to test and compare drivers on the bench are presented.

Fig 19 shows a circuit that can be used to test the

pulsed current source capability of a driver by clamping V_{OUT} to a level equal to V_{DSCH} + V_{DZEN} when the output is high. To minimize power dissipation the input is driven with a 200 ns positive-going pulse (for non-inverting driver) with a 2% duty cycle. In this circuit the positive-going voltage across R_{CS} is used to monitor the current sourced out of the driver. In order to change the value of the output clamping voltage, the voltage rating of D_{ZEN} must be changed.

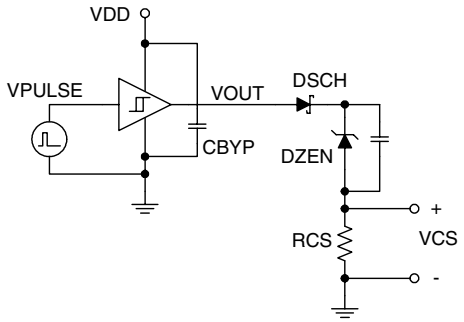

Fig. 19. Current source test circuit with clamped Vout

Fig. 20 shows a circuit used to test the pulsed current sink capability of a driver with the output voltage clamped at a level V_{ADJ}-VD_{SCH}. Here, the input is driven with a 200 ns negative-going pulse (for a non-inverting driver) with a 2% duty cycle. In this circuit the negative-going voltage across R_{CS} is used to monitor the current that the driver is sinking.

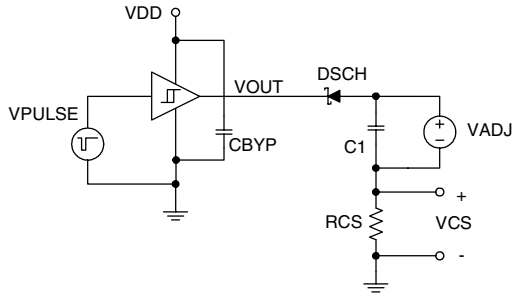

Fig. 20. Current sink test circuit with clamped Vout

In both of these circuits there is a voltage transient that may last for 50-100ns as the current increases to the limits of the driver. A compact layout using surface mount components will help to keep the loop area small to minimize the parasitic inductance.

The two previous circuits require a unique surface mount layout. It is possible to evaluate driver current capability by connecting a relatively large capacitive load on the output of a driver with the simple circuit shown in Fig 21.

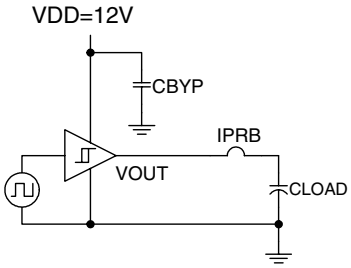

Fig. 21. "Large" load test circuit

For a starting point, C_{LOAD} is chosen to be 100 times larger than the load used for rise and fall time measurements, and the input is driven with a 1 kHz square wave. On typical datasheets, 2 Amp drivers are specified with 1 nF load for the rise and fall time specs, so C_{LOAD} would be selected to be 0.1uF. This relatively large load prevents the output from changing rapidly, allowing the driver output current to reach its internal limiting value. A current probe I_{PRB} can be used to monitor the output current along with the output voltage V_{OUT} on an oscilloscope. This allows one to plot the output current available at the corresponding output voltage. Bench comparisons have shown that the current measurement obtained using this method agrees closely with that obtained using the clamp circuits in Figs 19 and 20. In addition, the slower current rise and fall times allow the current measurements to be made comfortably within the bandwidth limits of a current probe.

Fig. 22 shows the waveforms obtained using the test circuit shown in Fig. 21 to evaluate a 2 Amp sink / 1.5 Amp source driver (FAN3227C) with a compound output stage. When the driver input Vin goes high, there is a transient glitch on the Vout trace as the output current quickly increases to 3 Amps through the inductance of the current probe loop. After approximately 70 ns the current has reached its peak value and the voltage spike across the parasitic inductances vanishes. With Vout = 6 V the output current is measured as 1.5 Amps (source current).

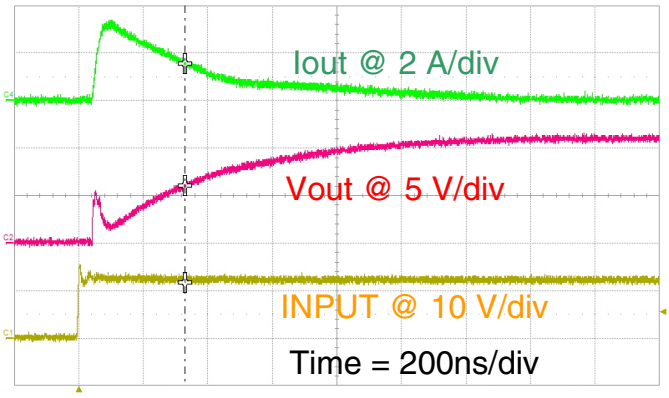

Fig. 22. Compound driver current source waveforms

Fig. 22 shows the leading spike across the inductance introduced by the wire loop inserted in the circuit to enable use of a current probe. If the wire loop is removed and the 0.1uF surface mount capacitor is installed in a layout with minimal parasitic inductance, the waveforms shown in Fig. 23 are obtained. In short intervals where the voltage waveform is approximately linear the basic relation

$$I = C_{LOAD} \cdot \left(\frac{dV_{OUT}}{dT} \right) \tag{16}$$

can be applied to provide an estimate of the current.

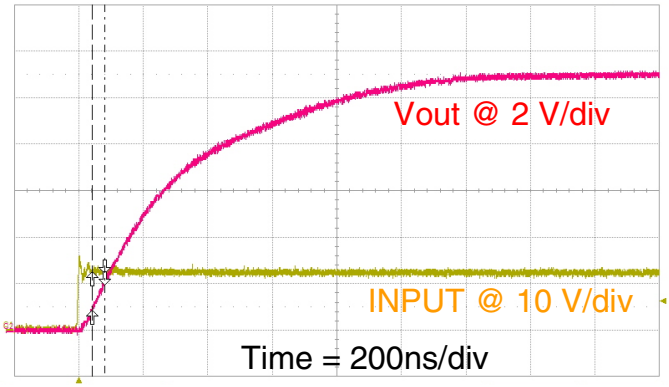

Fig. 23. Compound driver current estimation

The oscillogram in Fig. 23 allows one to calculate current during the cursor interval as

$$I = 0.1uF \cdot \left(\frac{1.131V}{40.6ns} \right) = 2.8A, \tag{17}$$

providing close agreement with the peak value seen in the I_{OUT} trace in Fig. 22. A similar calculation around VOUT = 6 V provides a current estimation of 1.5 Amps, nearly identical to the result obtained with direct current measurement using a current probe. The close agreement between the current measurement techniques using the large load helps to develop confidence in the results obtained.

VIII. Summary

Low-side drivers are used to drive power MOSFETs in applications including clamped inductive load switching, synchronous rectifier circuits, and pulse/gate transformer drive circuits. The relationship of gate drive current to the MOSFET switching and transition intervals has been detailed during the prominent MOSFET switching intervals. Potential driver solutions including discrete components, integrated PMOS/NMOS, and compound drivers were examined. Some of the non-ideal characteristics of the various driver circuits were highlighted.

There has not been a simple unified method to characterize the output current sink and source capability of the many types of drivers available in the market. The test circuits presented in this topic can be used to investigate the V_{OUT} versus I_{OUT} capability of discrete and integrated circuit drivers, enabling users to evaluate and compare drivers for a range of applications.

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