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Symmetric Dual N-Channel Shielded Gate PowerTrench® MOSFETs for Half-Bridge DC-DC Converter in Telecommunication Brick Module Application

Abstract

This application note presents symmetric dual N-channel shielded gate PowerTrench® MOSFETs optimized for the primary switches of a half-bridge DC-DC converter. A well-balanced $R_{DS(ON)}$ and Q_g of a shielded gate PowerTrench® MOSFET technology improves the Figure of Merit (FOM) ($R_{DS(ON)}$ x Q_g) factor is selected to achieve the highest efficiency with a well-balanced ratio between conduction loss and switching losses. A symmetric dual N-channel Power56 package containing two identical dies for primary high-side and low-side switches is able to increase the power density. The validity of symmetric dual N-channel shielded gate PowerTrench® MOSFETs is tested on a 100 W half-bridge DC-DC converter in a telecommunication quarter-brick size module.

Introduction

A brick DC-DC converter with a 48 V DC voltage bus in a telecommunication and network application needs higher power within the limited standard area, so higher efficiency and power are required. Internet facilities and telecommunication systems require sophisticated infrastructure and functionality. To design a highly efficient brick DC-DC converter, it is important to select the proper MOSFET because it generates most of power losses. MOSFET power losses consist of conduction and switching losses. Conduction loss is dominated by on-state resistance ($R_{DS(ON)}$). Switching losses are dominated by the gate charge (Q_g). To reduce power losses of a MOSFET, a well-balanced $R_{DS(ON)}$ and Q_g combination should be selected due to their trade-off relationship. Excellent thermal performance and compact size package is also essential to increase power density because the brick size of DC-DC converters is standardized regardless of power requirements.

This application note is organized as follows. In Section I, a basic operation of the half-bridge DC-DC converter and MOSFET power loss analysis in primary switch are performed. In Section II, shielded gate PowerTrench® MOSFET technology is shown and the power loss of different $R_{DS(ON)}$ - Q_g combinations of the given technology are examined. Experimental results of Power56 symmetric dual N-channel shielded gate PowerTrench® MOSFETs in 100 W half-bridge DC-DC converter (V_{IN}=36 V~48 V, V_{OUT}=3.3 V, I_{OUT}=30 A) are provided in Section III.

Section I

Telecommunication Brick DC-DC Converter

As telecommunication and network systems require a higher power due to the complex infrastructure support, their power architecture has been changed from Distributed Power Architectures (DPAs) to Intermediate Bus Architectures (IBAs) to increase the total system efficiency. Front-end isolated converters in Figure 1 were utilized in traditional DPAs to supply all required voltage levels from higher input, such as 48 V, to lower voltages required by each load. In some cases, these architectures cause high current circulating on the boards, along with fairly large voltage drop; therefore increasing power consumption. In IBA, the front-end converter would be similar to DPA, but the intermediate bus converter produces a bus line voltage and then Point of Load (POL) converters change it into the required voltages. Sharing this bus line means POLs can be synchronous buck or boost converters that can achieve the greatest efficiency and minimize the system size. An intermediate brick DC-DC module needs a higher efficiency and more power density as it increases its power coverage.

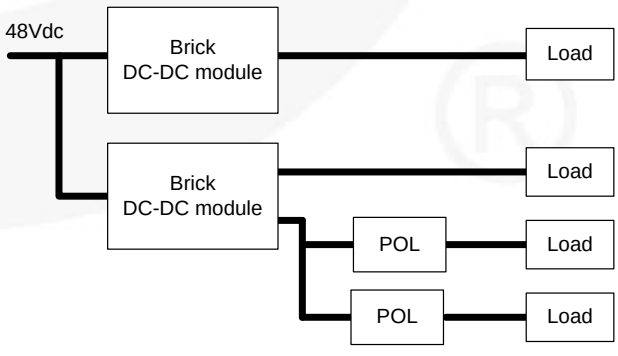


Figure 1. Distributed Power System Architecture

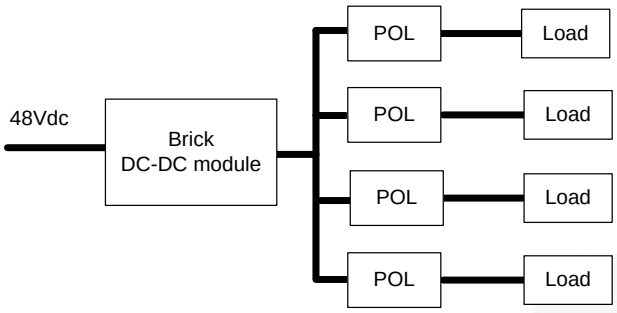


Figure 2. Power System Intermediate Bus Architecture

Basics of Half-Bridge DC-DC Converter

Along with reducing the brick DC-DC module size and increasing power density, the half-bridge topology offers high efficiency and good power handling capability up to 200 W. It is a good choice in isolated step-down DC-DC topologies. Figure 3 shows waveforms of the primary QH and QL for each time interval and Figure 4 - Figure 7 show the equivalent circuit of the half bridge DC-DC converter with a transformer center-tapped rectifier for each time interval. Each time interval is determined by switching of both primary high-side and low-side MOSFETs.

[$T_0 – T_1$]: Primary high-side MOSFET (QH) and secondary synchronous MOSFET (QS1) are ON and primary low-side MOSFET (QL) and other secondary synchronous MOSFETs (QS2) are OFF. The voltage across the primary transformer (V_p) is a half of input voltage (V_{IN}) and the secondary transformer voltage (V_S) is V_p / N. N is turn ratio of the transformer. The voltage across the output inductor is $V_S – V_O$ and the inductor charges the current.

[$T_1 – T_2$]: Primary QH and QL are OFF and QS1 and QS2 are ON. V_p and V_S are zero voltage. The voltage across the output inductor is $–V_O$ and the output inductor is discharged through QS1 and QS2.

[$T_2 – T_3$]: Primary QL and QS2 are ON and primary QH and QS1 are OFF. The voltage across the primary transformer (V_p) is a negative half of V_IN and the secondary transformer voltage (V_S) is V_p / N. The voltage across the output inductor is $V_S – V_O$ and the inductor charges the current.

[$T_3 – T_4$]: Primary QH and QL are OFF and QS1 and QS2 are ON. V_p and V_S are zero voltage. The voltage across the output inductor is $–V_O$ and the output inductor is discharged through QS1 and QS2.

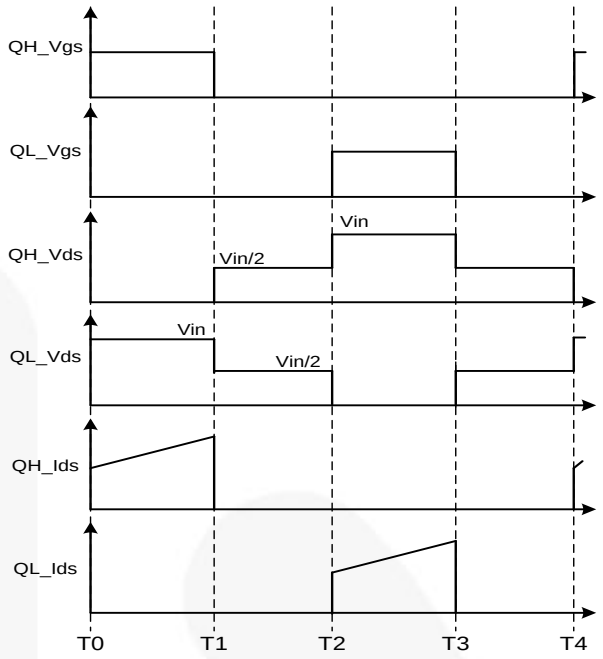


Figure 3. Primary MOSFETs Waveforms in Half-Bridge

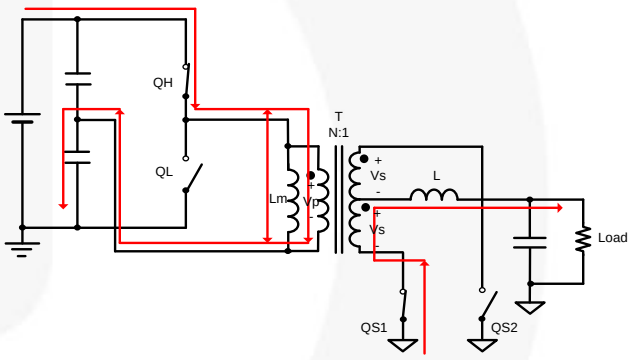


Figure 4. Half-Bridge Equivalent Circuit for Operation Time Interval; [T0 – T1] QH:ON, QL:OFF, QS1:ON, QS2:OFF

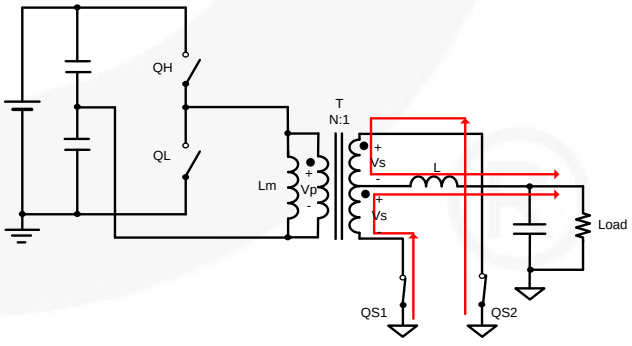


Figure 5. Half-Bridge Equivalent Circuit for Operation Time Interval [T1 – T2] QH:OFF, QL:OFF, QS1:ON, QS2:ON

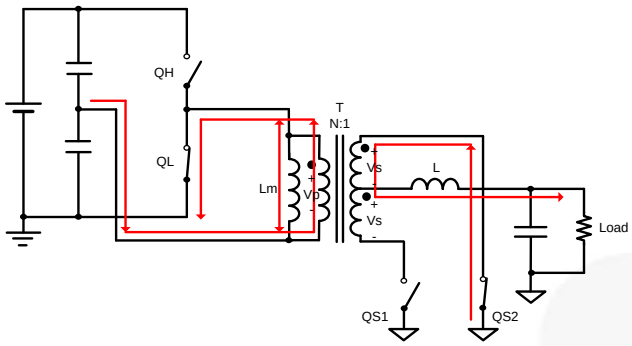


Figure 6. Half-Bridge Equivalent Circuit for Operation Time Interval [T_2 – T_3] QH:OFF, QL:ON, QS1:OFF, QS2:ON

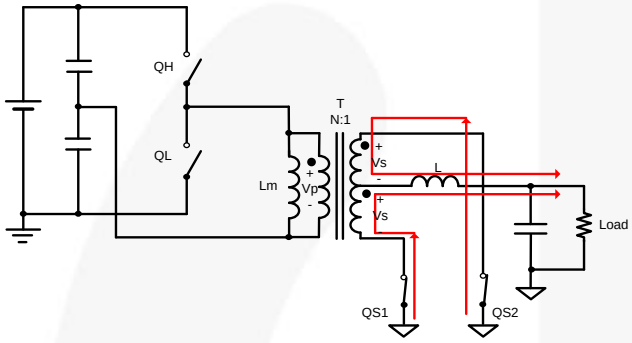


Figure 7. Half-Bridge Equivalent Circuit for Operation Time Interval [T_3 – T_4] QH:OFF, QL:OFF, QS1:ON, QS2:ON

Power Losses in Primary MOSFETs of Half-Bridge DC-DC Converter

Power losses in primary QH and QL MOSFETs of the half-bridge topology consist of the conduction loss and switching losses. The conduction loss is dominated by the $R_{DS(ON)}$ of the MOSFET, increased by a drain-to-source current.

$$\text{Conduction loss} = I_{RMS}^2 \times R_{DS(ON)} \quad (1)$$

Switching losses are dominated by gate charge (Q_g) and it increases by drain–to-source voltage. Switching losses can be broken into turn-on and off crossover losses, an output capacitance loss, and a gate-driving loss. Figure 8 shows gate-to-source voltage (V_{gs}) and a turn-on crossover loss when a MOSFET turns on in an inductive load.

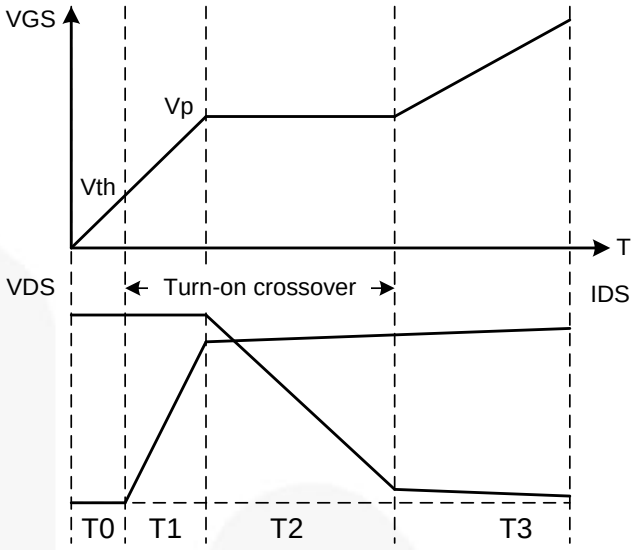


Figure 8. Gate to Source Voltage and Turn-on Crossover Loss

MOSFET switching starts by charging the MOSFET's input capacitance (C_{iss}). During T_0, there is no change in drain-to-source voltage (V_{DS}) and drain-to-source current (I_{ds}). Once V_{gs} reaches V_{th}, a MOSFET starts conducting and I_{ds} rises during T_1. V_{DS} is still clamped. During T_2, V_{DS} begins fall. Drain-to-gate voltage takes on negative values, so the reverse transfer capacitance (C_{rss}) increases hugely. Due to the dramatic rise in C_{rss}, V_{gs} is held at the plateau voltage (V_p). In T_3, the MOSFET is fully enhancing the channel to obtain its rated $R_{DS(ON)}$ at V_{gs}. Turn-on crossover loss occurs in T_1 and T_2 of turn-on crossover time ($\text{Turn-on}_{crossover}$). The turn-off crossover loss occurs in the same manner as the turn-on crossover.

$$\text{Crossover loss} = 0.5 \times (V_{DS} \times I_{ds}) \times (\text{Turn-on}_{crossover} + \text{Turn-off}_{crossover}) \times f_{sw} \quad (2)$$

where f_{sw} is a switching frequency.

The stored charge in the output capacitance (C_{oss}) is dissipated as shown in the below equation:

$$\text{Output capacitance loss} = 0.5 \times (C_{oss} \times V_{ds}^2 \times f_{sw}) \quad (3)$$

Gate driving loss at driver is related to the gate charge as:

$$\text{Gate driving loss} = Q_g \times V_{gs} \times f_{sw} \quad (4)$$

To reduce power losses of a MOSFET, $R_{DS(ON)}$ and Q_g must improve, but $R_{DS(ON)}$ and Q_g have a trade-off relationship.

Section II

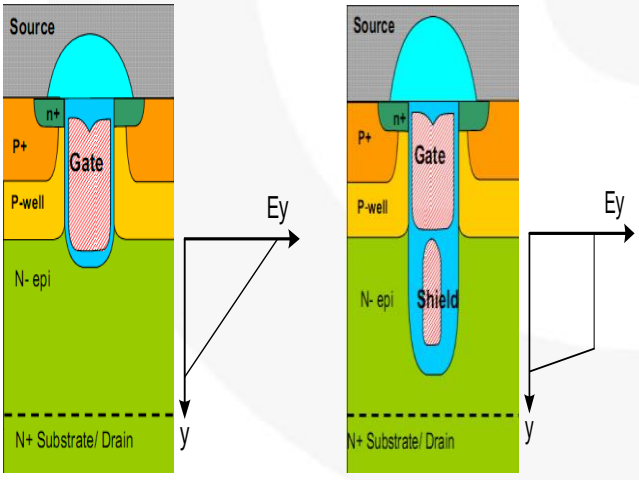
Shielded Gate PowerTrench® MOSFET Technology

Figure 9(a) shows the vertical structure of the conventional PowerTrench. To reduce $R_{DS(ON)}$ of the conventional PowerTrench, the pitch between gate trenches is reduced to make more cells in the limited die size, but it causes increased reverse transfer capacitance (C_{rss}), resulting in increased switching losses.

Table 1. Components of $R_{DS(ON)}$ for Conventional Trench, $R_{DS(ON)}$ V_g = 10 V, 200 A/cm^2

	V_{DS} = 30 V	V_{DS} = 100 V
$R_{Channel}$	47%	16%
$R_{Epitaxial}$	29%	78%
$R_{Substrate}$	24%	6%

Table 1 shows the $R_{DS(ON)}$ components, comparing a 30 V-rated with a 100 V-rated conventional trench MOSFET. The $R_{DS(ON)}$ contribution from the epitaxial drift region is a much larger percentage for the 100 V MOSFET because a high blocking voltage requires a relatively thick and low-doped epitaxial drift region. Fairchild's shielded gate PowerTrench® MOSFET employs the shield electrode connected to source for the charge balance in epitaxial drift region, as shown in Figure 9(b).[1] The electric field in epitaxial is plated by the charge balance, so the doping concentration in epitaxial can be increased, resulting in a reduced epitaxial resistance. It leads reduced conduction loss of a MOSFET.



(a) Conventional PowerTrench (b) Shielded Gate PowerTrench

Figure 9. (a) Conventional vs. (b) Shielded-Gate Vertical Structure PowerTrench® MOSFET

The shield electrode resides below the gate electrode, converting most of the gate-to-drain capacitance (C_{gd} or C_{rss}) at the bottom of the conventional trench MOSFET to gate-to-source capacitance (C_{gs}). The shield electrode wraps the gate electrode from the drain potential.

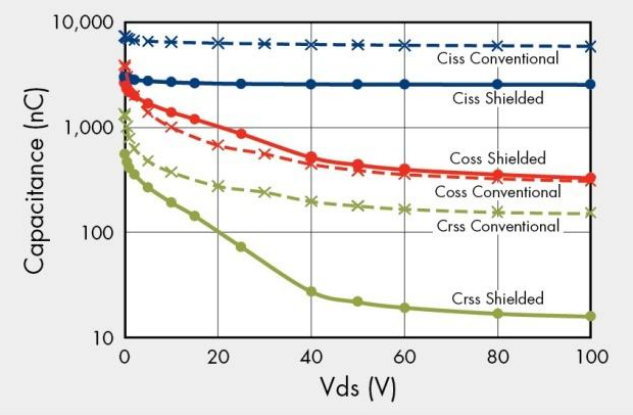


Figure 10. Comparison of Capacitive Components for Conventional and Shielded-Gate Trench with Equivalent 20 A $R_{DS(ON)}$ 5.7 mΩ

Figure 10 compares the capacitive components of a conventional and a shielded-gate trench MOSFET with equivalent $R_{DS(ON)}$. By reducing C_{rss}, turn-on and turn-off crossover losses are minimized by shortening the T_2 period in Figure 8.

Optimized $R_{DS(ON)}$ and Q_g for High-Efficiency Half-Bridge DC-DC Converter

Telecommunication brick DC-DC converters request the wide input voltage range from 36 V to 75 V. At the minimum input voltage of 36 V, the conduction loss has the larger portion of the maximum input voltage of 75 V due to higher current in Equation (1). The switching losses are reduced at the minimum input voltage since drain-to-source voltage (V_{DS}) is reduced in equation (2) and (3). Table 2 shows the electrical specification of the quarter brick DC-DC converter in this application note.

Table 2. Electrical Specification of Quarter Brick DC-DC Module

Brick DC-DC Module Size	Quarter Brick
Topology	Half-Bridge
Input Voltage	36 V ~ 75 V
Output Voltage	3.3 V
Maximum Output Current	30 A
Switching Frequency	200 kHz

Table 3 shows different $R_{DS(ON)}$ and Q_g combinations of shielded gate PowerTrench® MOSFET.

Table 3. Measured Electrical Parameters

MOSFETs	$R_{DS(ON)}$ [mΩ] at 10 V_{gs}	Q_g [nC] at10 V_{gs}
A	6.3	39.0
B	11	19
C	20.0	11.7
D	27.0	7.5

Figure 11 shows the evaluated efficiency graph at 100 W of output power with the various $R_{DS(ON)}$ and Q_g combinations.

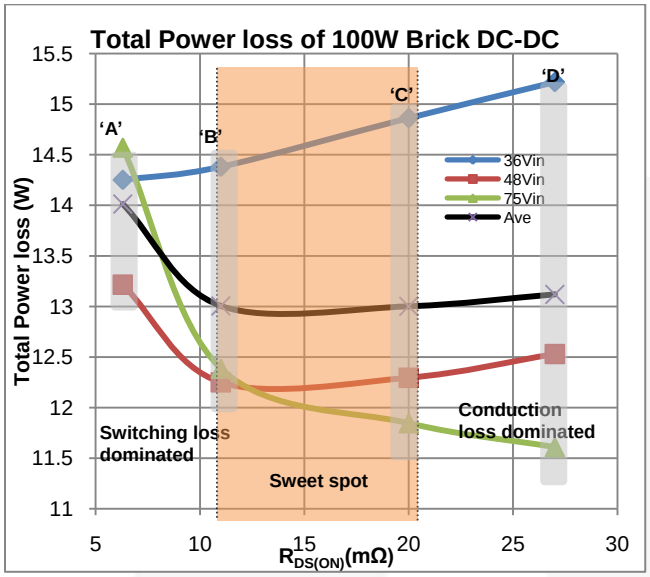
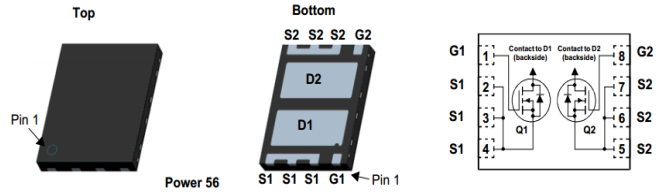


Figure 11. Efficiency & Power Loss, Varied $R_{DS(ON)}$ at V_{IN}=48 V, V_{OUT}=3.3 V, I_{OUT}=30 A, T_A=25°C, Natural Convention

Because MOSFET Q_g and $R_{DS(ON)}$ have an inverse relationship, the switching losses of a MOSFET with a lower $R_{DS(ON)}$ tend to increase even if the conduction loss is decreased. On the other hand, the conduction loss of a higher $R_{DS(ON)}$ MOSFET is increased, but the switching losses are reduced. Figure 11 shows that the power loss tendency at the maximum 75 V input voltage is reduced by decreasing Q_g rather than $R_{DS(ON)}$, even though, in the minimum voltage of 36 V, the lowest $R_{DS(ON)}$ MOSFET has the lowest power loss. Each switching loss and condition loss ratios depends on the input voltage. In the case of 'B' in Figure 11, the total power loss at 36 V, 48 V, and 75 V of input voltage is 14.38 W, 12.24 W, and 12.38 W, respectively. The average power loss according to the input voltage from 36 V to 75 V is calculated to 13 W. By using the average power loss graph, an optimized $R_{DS(ON)}$ and Q_g combination can be found. To achieve the highest efficiency in all the input voltage coverage, a well-balanced $R_{DS(ON)}$ and Q_g MOSFET should be selected. The well-balanced ratio between switching losses and conduction loss can be found in the "sweet spot" of Figure 11.

Symmetric Dual Power56 Package

Because the telecommunication brick DC-DC module size is standardized and limited, the MOSFET package plays a critical role in power density. The symmetric dual N-channel Power56 package contains two identical dies for high-side and low-side MOSFETs for the half-bridge's primary side switch, replacing two separate Power56 MOSFETs. The Power56 symmetric dual package occupies only half the footprint compared with two separate single packages. Therefore, it increases power density for half-bridge DC-DC converters.



$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Figure 12. Symmetric Dual Power 5x6 Package

Section III

FDMS8090 Performance in Quarter Brick DC-DC Converter

The FDMS8090 offers a well-balanced $R_{DS(ON)}$ and Q_g combination for the primary switch of the half-bridge DC-DC converter. and the thermally enhanced symmetric dual Power56 package saves PCB space. Table 4 shows the electrical characteristics of FDMS8090.

Table 4. FDMS8090 Electrical Characteristics

Package	MOSFET	BV_{DSS} (V)	$R_{DS(ON)}$ [mΩ]@ 10V_{gs}	Q_g [nC]@ 10V_{gs}	Q_{gd} [nC]
			Typ.	Typ.	Typ.
Power 5x6 Symmetric Dual N-ch	Q1	100	11	19	4.1
	Q2	100	11	19	4.1

The performance of FDMS8090 is tested on the 100 W quarter brick DC-DC converter specified in the Table 2. Figure 13 and Figure 14 show the total efficiency and thermal performance, respectively.

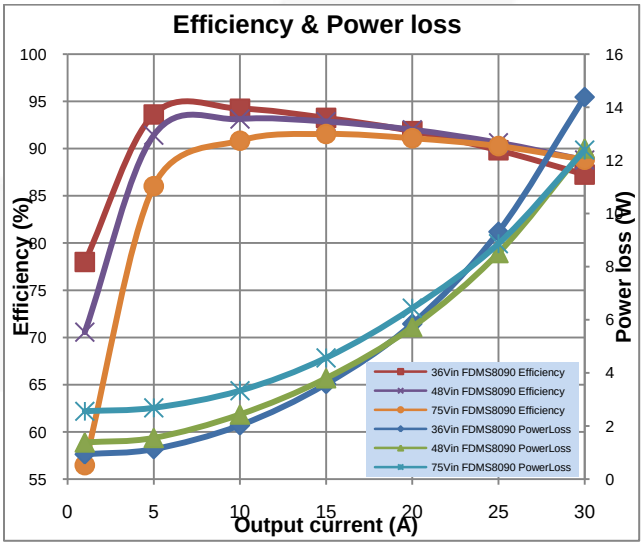


Figure 13. Efficiency and Power Loss at V_{IN}=36 ~ 75 V, V_{OUT}=3.3 V, f_{SW}=200 KHz, T_A=25°C, Natural Convention

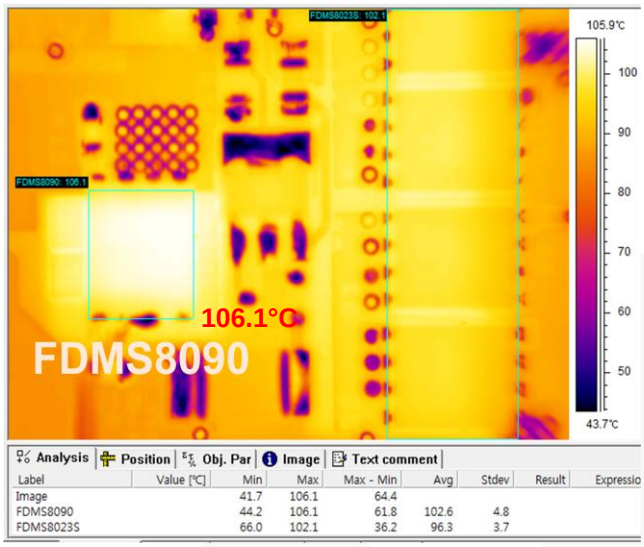


Figure 14. Thermal Performance at V_{IN}=48 V, V_{OUT}=3.3 V, I_{OUT}=30 A, f_{SW}=200 KHz, T_A=25°C and Natural Convention

Telecommunication brick DC-DC converters require the wide input voltage from 36 V to 75 V, so selecting a well-balanced $R_{DS(ON)}$ and Q_g MOSFET is the critical design step. The maximum load efficiencies of the FDMS8090, with input voltages 36 V, 48 V, and 75 V are 87.25%, 88.78%, and 88.82%, respectively.

Conclusion

It is essential that telecommunication brick DC-DC converters have higher efficiency and more power density. Shielded-gate PowerTrench® MOSFETs, such as the FDMS8090 with its well-balanced $R_{DS(ON)}$ and Q_g in the symmetric dual N-channel Power56 package, are able to improve the efficiency and power density of half-bridge DC-DC converter in the limited size.

Authors

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Dongsup Eom - Applications Engineer (Dongsup.Eom@fairchildsemi.com)

References

[1] SungJin Kuen, Dongsup Eom, Joe Yedinak; "Mid-Voltage Shielded PowerTrench® MOSFET in High Step-Up DC-DC for Edge-Lit LED TV Backlighting" Fairchild Application Note AN-9763.

Related Resources

FDMS8090 — PowerTrench® Power Stage 100 V Symmetric Dual N-Channel MOSFET: 100 V, 10 A, 13 mΩ N-Channel

AN-9763 — Mid-Voltage Shielded PowerTrench® MOSFET in High Step-Up DC-DC for Edge-Lit LED TV Backlighting

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