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AN-5077
Design Considerations for High Power Module (HPM)

Abstract

Fairchild's High Power Module (HPM) solution offers higher reliability, efficiency, and power density to improve performance and reduces size and weight compared to a discrete solution. It also provides simpler repair and maintenance and design. The market trend in industrial power systems; such as photo-voltaic inverters, welding machines, and uninterruptible power supplies; is rapidly moving toward the module approach. Fairchild's leading power semiconductor products in the market include 600 V / 650 V field-stop IGBTs, 650 V / 1200 V field-stop trench IGBTs, 600 V / 650 V super-junction MOSFETs and fast / soft recovery diodes. Fairchild has now launched the High Power Module (HPM) solution with leading power devices. This application note introduces HPM products and shows the differences between module vs. discrete solutions, describes considerations and guidance for PCB layout design, and explains how to design and use HPMs properly and efficiently.

Introduction of HPM

The HPM "F-series" offers custom modules as well as standard modules, covering a full scope in the power, ranging up to hundreds of amperes with 600 V / 650 V / 1200 V devices. F-1 and F-2 cover under tens of kilowatts and will be extended to the larger package size for the higher power. Figure 1 shows the package dimensions.

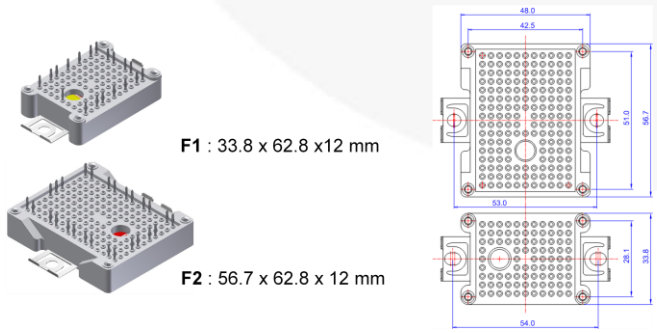


Figure 1. Package Dimension of F1 & F2

F-Series Key Features

- High Integration and Compact Design
- Low Switching Loss
- Low Stray Inductances
- Optimized Thermal Performance
- Long Isolation Distances and Creepage
- Press-Fit Contact Technology

The HPM features provides superb reliability and high efficiency to systems and benefits system design through design-friendly layout, mounting with PressFIT terminal, fast solderless assembly, and the optimized system cost for the diverse topologies such as converters, inverters, and customized circuitry.

Design Considerations

- Parasitic Inductances
- Voltage / Current Spikes / Oscillations through Parasitic Inductance
- Route of PCB Patterns
- Kelvin Source / Emitter Gate Drive
- Location of Components

PCB Layout Guidance

This section demonstrates the general guideline for Printed Circuit Board (PCB) layout by discussing considerations that affect the performance of HPM. The following sections detail how to optimize the design of PCB with HPM.

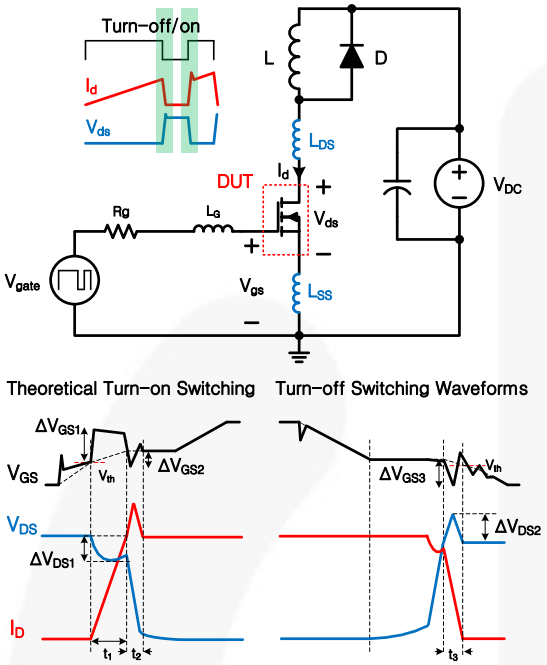


Figure 2. Double-Pulse Inductive Switching Circuit with Parasitic Inductance and Switching Behavior

Influence of Parasitic Inductance

Parasitic inductance in fast-switching applications is a major problem, causing over-voltage spikes and increasing switching turn-off losses. Figure 2 shows the double-pulse inductive switching circuit with parasitic inductances: L_{DS}, L_{SS}, and L_G and the switching behavior. The switching characteristics can be measured using the circuit under any voltage and current stresses without self-heating as long as the double-pulse gate signals are given. The influence of each inductance through the circuit is visible, which also represents almost inductive switching circuits. The influence is well documented from prior research[1]-[2] and reaffirmed through simulated results from PSpice models.[3] The di_D/dt drain-current slope is generated during switching transients and limited by L_{SS} as a negative voltage source. There are voltage spikes and drops in parasitic inductances by the di/dt, such as: $\Delta V_{DS1} = (L_{DS}+L_{SS}) * di_D/dt_1$, $\Delta V_{GS1} = L_{SS} * di_D/dt_1$, $\Delta V_{GS2} = L_{SS} * di_D/dt_2$, $\Delta V_{GS3} = L_{SS} * di_D/dt_3$, and $\Delta V_{DS3} = (L_{DS}+LSS) * di_D/dt_3$.

The simulation result in Figure 3 shows the effect of the drain inductance, L_{DS}, also called loop inductance. The inductance intrinsically resonates with the output capacitance of MOSFET / IGBT and diode junction capacitance when turning on and off. That oscillation inevitably affects the gate loop through Miller capacitance. Therefore, as L_{DS} increases, ringing in all V_{GS}, V_{DS}, and I_D waveforms is introduced during the switching transients. The overshoot in V_{DS} at turn-off is much more significant than in the gate drive loop, which can cause worse oscillation and stresses on the device over breakdown voltage. Though the DC-link voltage is only 400 V, the peak voltage at turn-off can reach up to 480 V with 60 nH loop inductance in the simulated conditions, while only 420 V with 1 nH even with the same di_D/dt. The drain inductance comes from the long and narrow PCB route from DC-link capacitor's positive pin-to-pin of MOSFET / IGBT's drain / collector and even from the internal parasitic of package, such as long lead or substrate.

The simulated turn-on and turn-off switching waveforms in Figure 4 clearly show the influence of the common source inductance, L_{SS}. L_{SS} serves as a negative feedback from the switching loop into the gate loop. During the rise and fall periods of I_D, the voltage across the inductance, $V_{LSS}=L_{SS}*di_D/dt1$, reduces the gate voltage. This decreases the charging current for gate charge, slowing down the drain current. The increase of L_{SS} decreases the di_D/dt due to the lower negative V_{LSS}. Although that increase can suppress the current ringing into the device and reduce the voltage across the parasitic inductances due to the lower di_D/dt, it significantly increases the switching energy loss at turn-on and turn-off. The inductance results from the parasitic on the route from the source / emitter pin of MOSFET / IGBT to the DC-link capacitor's negative pin and its package lead and internal bonding wires to connect the chip's active source / emitter area to the package lead pin.

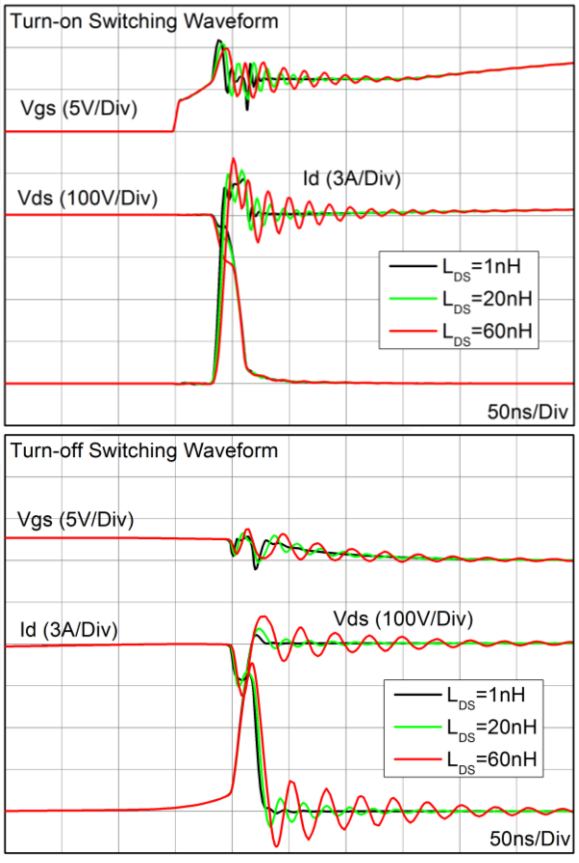


Figure 3. Influence of Drain Inductance, L_{DS}

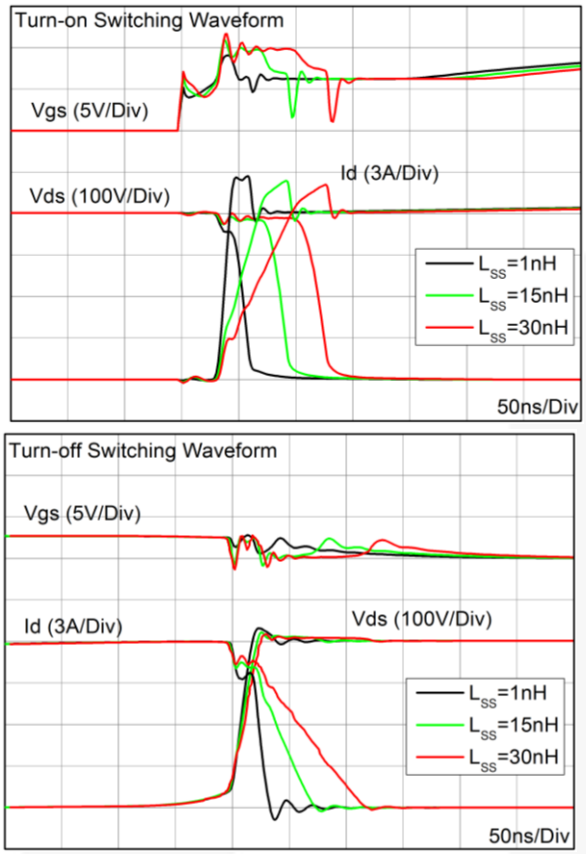


Figure 4. Influence of Common Source Inductance, L_{SS}

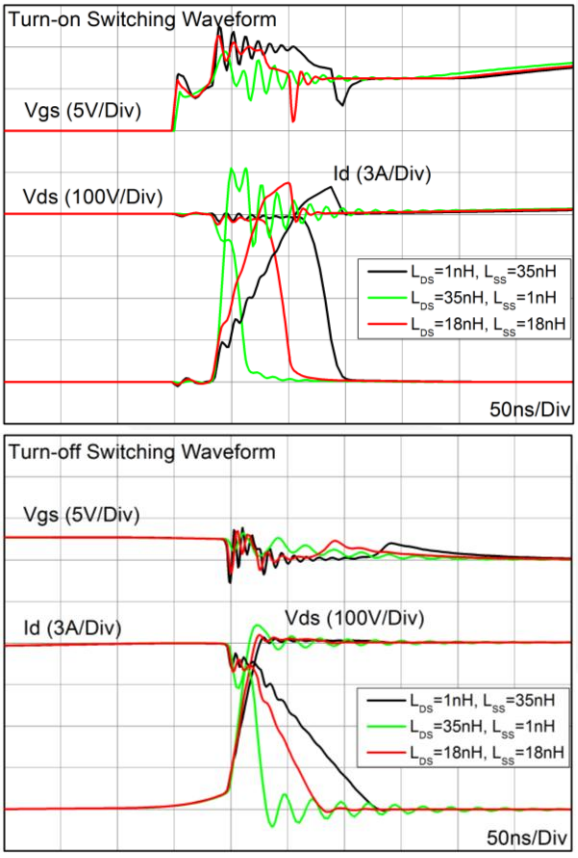


Figure 5. Influence L_{DS} and L_{SS}

The ringing is caused by L_{DS}, which can be suppressed by L_{SS} because of its negative feedback effect to limit di_D/dt slope. The simulation result in Figure 5 demonstrates that voltage overshoot is determined by both the total parasitic inductance and the magnitude of common-source inductance. For example, the voltage overshoot at turn-off is reduced with an increase of common-source inductance by decreasing di_D/dt slope while keeping a constant total inductance. However, the price is much higher switching loss. Electromagnetic Interference (EMI) problems caused by overshoot and oscillation in parasitic inductances can be removed by increasing the turn-off gate resistor that limits the charging and discharging gate current, having the same effect as an increase in L_{SS}.

Since the common-source inductance works as dependent source on di_D/dt during the switching transient state; in this period of di_D/dt, the equivalent circuit in the gate drive path can be expressed as R-L-C series resonance circuit with the dependent source of V_{LSS}.[4] Two different values of gate inductance are compared in clamped inductive load switching circuit in Figure 6. A circuit with low value for L_G (white lines) has lower peak gate negative voltage than the circuit with higher L_G (color lines). To achieve optimized gate waveform, it is necessary to reduce gate inductance, L_G, as well as common-source inductance, L_{SS}. The gate inductance can come from long and narrow PCB route from driver to gate pin, parasitic components of drive IC, gate resistor, internal bonding wires, and long lead length. The PCB designer should place the gate driver as close electrically as possible to minimize the potential resonance from the gate loop inductance and avoid parallel PCB pattern that create parasitic capacitance between the positive and negative rails.

The influence of inductances L_{DS}, L_{SS}, and L_G can come from components' parasitic and PCB routes. Before design and layout with HPM, the difference between discrete and module must be understood. The components' parasitic inductance; such as bonding wire, copper substrate, lead pin, resistors, and capacitor stray inductance must be managed by considering the difference and stray, then reducing the parasitic inductance of the PCB pattern caused by the long and narrow paths and the types of route (discussed in the next section).

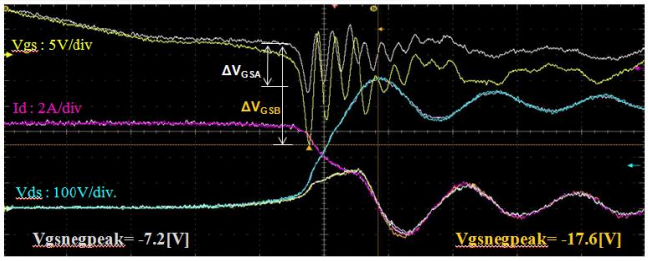


Figure 6. Influence of Gate Stray Inductance

HPM vs. Discrete — Reducing Inductance

Figure 7 and Figure 8 show parasitic inductances in full-bridge configuration with discrete devices and HPM. L_{WB} is parasitic inductance by wire bonding, L_{EC} is by external connection like PCB pattern, L_{LEAD} is by leads / pins / terminals, and L_{SUB} is substrate's parasitic inductance. Other components, like contact resistors and stray capacitances, are eliminated to focus on the inductance. The discrete solution has more parasitic inductances than HPM because the inevitable external connection from pin to pin through the PCB pattern and additional terminals to connect each device. Therefore, with the same gate resistance and devices, HPM solution can provide the higher di/dt, dv/dt by lower common source / emitter inductance and less oscillation due to lower drain / collector inductance than discrete solution. HPM offers optimized switching performance over discrete solutions regarding the components' parasitic inductance. The next effort should be to reduce PCB pattern strays of route to HPM.

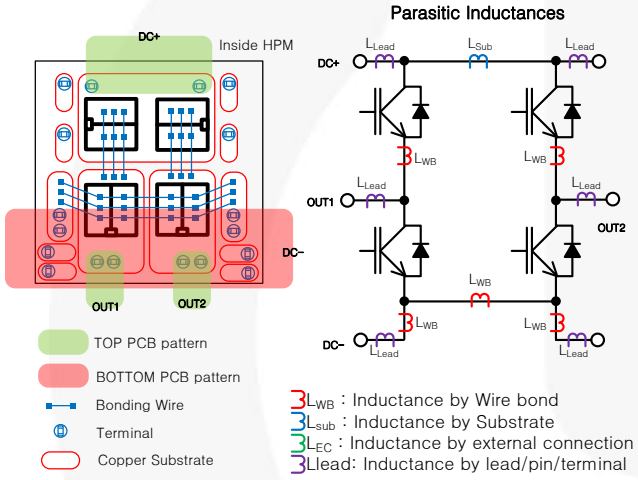


Figure 7. HPM Full-Bridge, Parasitic Inductance

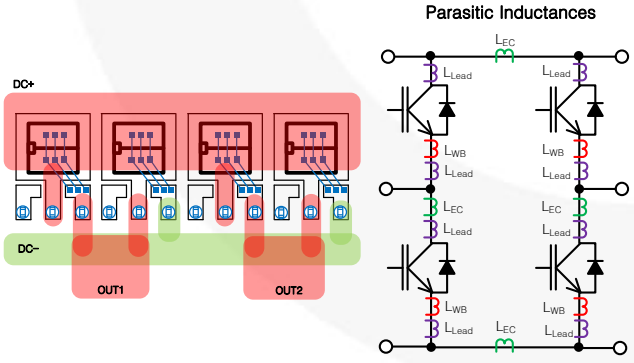
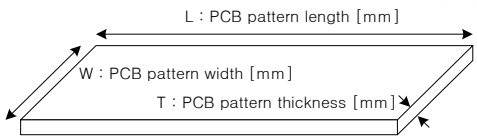
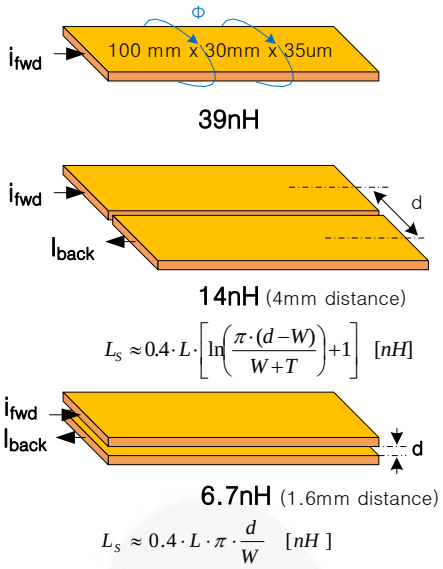


Figure 8. Discrete Full-Bridge, Parasitic Inductance



$$L_S = 0.2 \cdot \left[\ln\left(\frac{2 \cdot L}{W+T}\right) + 0.2235\frac{(W+T)}{L} \right] \quad [nH]$$

Figure 9. Self Inductance of PCB Pattern



$$L_S \approx 0.4 \cdot L \cdot \left[\ln\left(\frac{\pi \cdot (d-W)}{W+T}\right) + 1 \right] \quad [nH]$$

$$L_S \approx 0.4 \cdot L \cdot \pi \cdot \frac{d}{W} \quad [nH]$$

Figure 10. Example to Reduce Inductance

The PCB pattern's parasitic self inductance can be defined as Figure 9[5], which increases with the longer path, narrower width, and thinner thickness. It also depends on the type of the route, as shown in Figure 10[6]. From the equation, a flat conductor of the first example has a self inductance of 39 nH by PCB pattern of 100 mm length, 30 mm width, in case of 1 ounce (0.0035 mm). The two flat side-by-side patterns with 4 mm distance of the second example, considering isolation distance over 400 V on a single layer, show a return inductance of 14 nH to cancel the magnetic field; partly by bringing the return current close to the forward current. The third example of two flat patterns in parallel on a double-layer layout, can be reduced to 6.7 nH with 1.6 mm distance.

To reduce loop inductance from DC-link capacitors to HPM's power pins, the third example would be the best layout with multilayer and second example is also suitable for single-layer because the parasitic capacitance is not a large problem in a drain-source loop path. Regarding the gate inductance, these examples might increase the capacitances, causing more oscillations. It is therefore important that gate driver be placed as close electrically as possible to remove inductance, then avoid the route like these examples for the lower capacitance. The vertical route of gate line against drain / collector and source / emitter also can reduce the capacitances.[7]

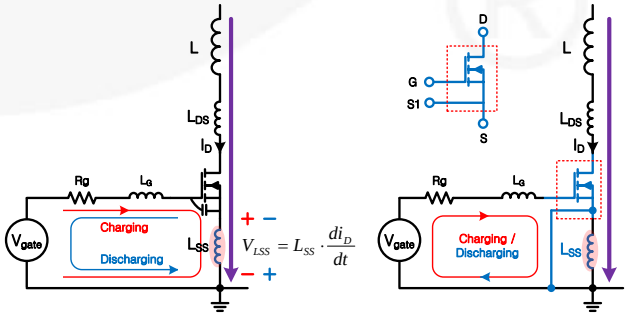


Figure 11. Kelvin Source / Emitter Gate Drive

Effectiveness of Kelvin Source/Emitter

HPM provides an additional pin for a Kelvin source / emitter to drive the gate. In this section, the effectiveness of the Kelvin, improving switching performance by removing oscillation by high di/dt, is discussed.

Figure 11 indicates the effectiveness of Kelvin source / emitter drive on the gate-source drive path compared with a conventional three-pin gate drive. When turning on and off, the stray inductance counteracts as a dependent source by di_D/dt and the voltage across L_{SS}, $V_{LSS}=L_{SS}*di_D/dt$, becomes negative feedback to disturb charging and discharging current into gate-source, decreasing di_D/dt. The Kelvin source drive can remove this disturbance by separating the gate-drive current from the high-drain current. It can increase the di/dt slope with the same resistor and with less gate oscillation compared to the three-pin drive.

Figure 12 shows the switching loss improvement of 77 mΩ SuperFET® 2 FRFET® inside HPM at V_{CE}=400 V, T_C=25°C, and R_g=10 Ω with Kelvin source drive compared with non-Kelvin. The solid line is non-Kelvin and the dotted line is Kelvin drive. With the advantage, it can reduce the switching performance by up to 44% E_{ON} as well as 40% E_{OFF} at the rated current. In the measured switching waveforms of Figure 13, it is clear that it increases di_D/dt with Kelvin drive, so can reduce switching energy losses. Compared with non-Kelvin, 3 A-to-30 A di/dt slope is increased from 627 A/µs to 1430 A/µs for E_{ON}, 25 A-to-5 A slope from 804 A/µs to 1170 A/µs, while slightly increasing 100 V-to-300 V dv/dt slope from 54.4 V/ns to 57.9 V/ns at turn-off. It shows that the faster di/dt is the more effective.

The most important benefit of Kelvin drive is the ability to increase di/dt with less gate oscillation compared with three-pin. Increasing switching speed can normally be achieved by reducing the gate resistor, but that can result in higher gate oscillation due to increased gate current. This means that Kelvin drive should be mandatory for the faster switching devices, especially for a module with lower parasitic inductance than discrete devices. In low-frequency switching with low di/dt line-frequency, it is optional.

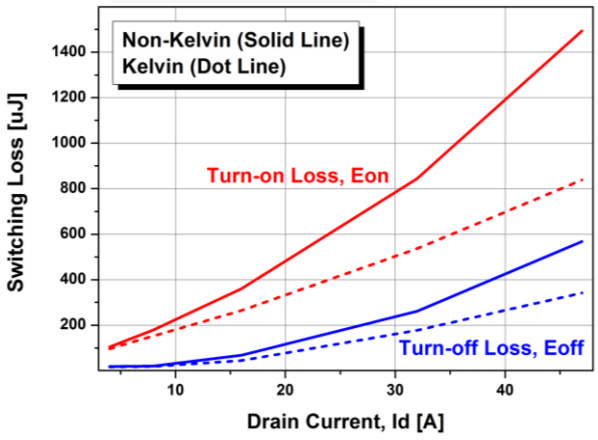


Figure 12. Switching Loss Improvement by Kelvin

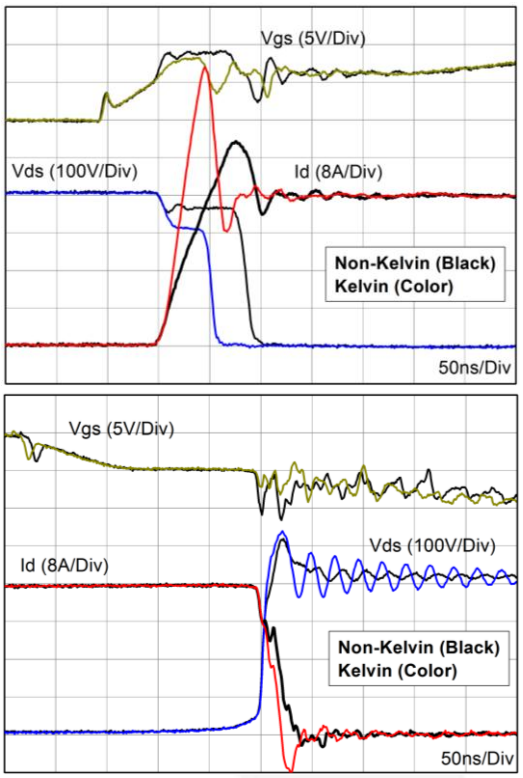


Figure 13. Switching Waveform Comparison for Kevin

In this section, the advantage of Kelvin drive is discussed. The additional pin provides better switching performance with the less gate oscillation than three-pin driving. As shown in switching waveforms, di/dt and dv/dt are increased, which means the PCB designer must consider EMI and reduce parasitic elements, such as loop / drain inductance and capacitance of gate-to-drain / source.

Location of Bypass Capacitor

The location of the DC-link capacitors is important because a long path from DC-link capacitors to the DC+ and DC- terminals of the HPM results in the high parasitic inductance, as shown in Figure 14, even with the well-designed PCB layout. The bypass capacitor is required to reduce the disadvantage of the long path, which can't be avoided. Figure 15 shows the influence by the location of bypass capacitors. The color waveforms with the bypass capacitor closest to module's DC input pin has less oscillation in turn-on/off currents, turn-off voltage, and gate waveforms. Voltage drop during turned-on is also reduced compared to the black lines with the long path.

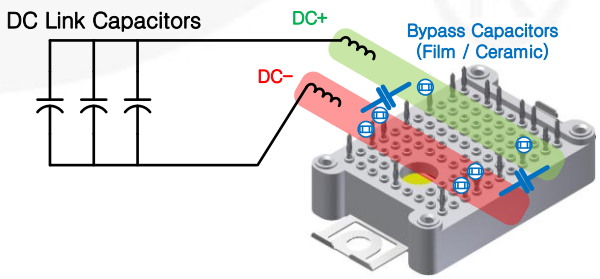


Figure 14. Inductance by Path from DC Link Capacitors to Terminals

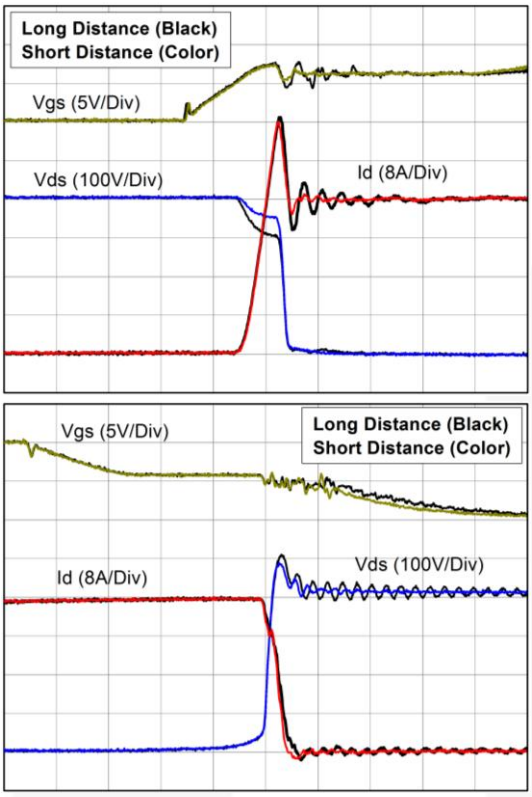


Figure 15. Effectiveness of Bypass Capacitor

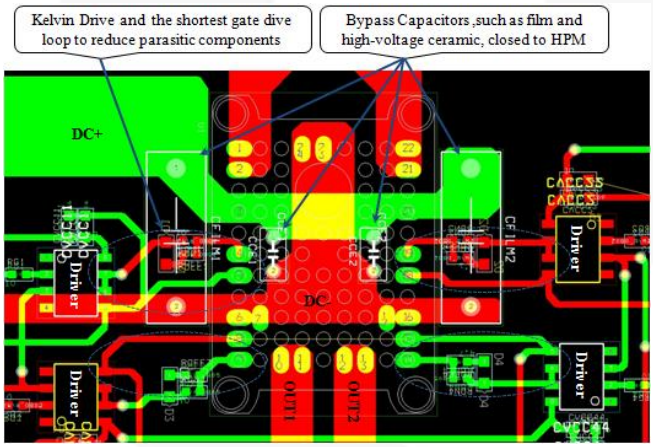


Figure 16. Example of PCB Design

Figure 16 shows an example of PCB design with HPM. Bypass capacitors of film and high-voltage ceramic capacitors are placed close to the module to remove the drawback of the long path from the DC-link capacitor. The gate drive loop is separated from the main drain current path using Kelvin source pins for improved switching. It is also considered the shortest path for lower inductance to place the driver IC as close as possible and routed into a both-side pattern to reduce capacitances.

Summary and Conclusion

Considerations for PCB design, investigation of the influences of parasitic inductances and methods to reduce it, and the benefits of Kelvin drive have been discussed.

Summary of HPM Design Considerations

- Drain (loop) inductance: larger L_{DS} causes oscillations in switching voltage and current, which can be minimized with the proposed examples.
- Common source inductance, which is related to di_D/dt: smaller inductance increases speed, but can cause oscillation. HPM provides an optimized pattern compared to discrete configuration.
- Gate loop inductance, which resonates with gate junction capacitance and stray capacitance, resulting in gate oscillation: the placement of the drive IC close to HPM, the shortest path, and the route to avoid parasitic capacitance are recommended.
- Kelvin drive: can improve switching performance, providing higher di_D/dt even with the less gate oscillation, which removes the drawback of common-source inductance.
- Bypass capacitor: close to the module can remove the drawback of long path from DC-link capacitors to power terminals of module.

References

[1] *Zheng Chen, Dushan Boroyevich and Rolando Burgos, "Experimental Parametric Study of the Parasitic Inductance Influence on MOSFET Switching Characteristics," The 2010 International Power Electronics Conference.*

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[3] *PSpice Models of Super Junction MOSFETs on Fairchild semiconductor website, http://www.fairchildsemi.com/models/modelDetails?modelType=PSPICE#resultDiv*

[4] *Dongkook Son, Wonsuk Choi, "New generation Super-Junction MOSFET in PQFN88 for High Efficiency and Low Profile Power Systems," The 2012 PCIM-Aisa.*

[5] *"PCB Design Guidance for SPM," AN-9760, Fairchild Semiconductor.*

[6] *"Parasitic effects in Power Electronics", PEMC – Power Electronics and EMC*

[7] *"New Generation Super-Junction MOSFETs, SuperFET II and SuperFET II Easy Driver MOSFETs for high Efficiency and Lower Switching Noise," AN-5232, Fairchild Semiconductor.*

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