Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

AN-1065

Fairchild Semiconductor
Application Note
November 1996
Revised February 2001

GTLP: An Interface Technology for Bus and Backplane Applications

Abstract

The development of the Gunning Transceiver Logic (GTL) technology has yielded a high performance interface family ideal for bus and backplane interface applications. Gunning Transceiver Logic Plus (GTLP), Fairchild Semiconductor's derivative of GTL, is ideal in many of today's high speed computing, networking, and telecom backplanes because of its low power, moderate drive, and output edge control. The characteristics and features of GTLP make it an excellent choice in many high speed bus and backplane driving applications. This application note presents information about the advantages and features of GTLP.

Introduction

The need for increased system throughput is pushing today's bus and backplane designs toward higher and higher data rates. Backplane designs which operate at 1 MHz–20 MHz can normally use TTL technologies such as FAST® or ABT because they can afford the settling time required before sampling the bus. As designs require increased throughput the need increases for a low noise, reduced swing family such as GTLP. Fairchild's GTLP technology increases the operating frequency of a bus or backplane application by ensuring incident wave switching into 50Ω with minimal output generated noise. Figure 1 is an example of a GTLP backplane. It has a characteristic trace impedance of 50Ω and is terminated at both ends with pull-up resistors of 50Ω to +1.5V.

Background

The GTL standard was developed by William Gunning of XEROX®. The intention was to make GTL a relatively low cost and high speed technology for driving terminated transmission lines and busses. GTL is a "Reduced Output Swing Technology", meaning the output switching levels are less than both 5V CMOS (Rail-to-Rail) and TTL (~3.5V). The output structure is an open drain NMOS transistor which requires the bus or backplane to be actively terminated for proper signaling. The bus termination for GTL is made up of a pull-up resistor to a termination voltage. The value of the pull-up resistor should be equivalent to the line impedance to reduce reflections. The input, or receiver section, is a differential amplifier which compares the input signal level with an externally supplied reference voltage (designated as V_{REF}). Tight threshold regions, a characteristic of differential amplifiers, ensure a sufficient noise margin with respect to output swing.

Fairchild Semiconductor's GTLP technology is an extension to the GTL standard. Electrical specification differences between GTLP and the GTL standard are: output signal level, reference voltage (V_{REF}), and output termination voltage.

The magnitude of the GTLP output swing is 0.95V (V_{OL} = 0.55V and V_{OH} = 1.5V) whereas the GTL output swing is 0.80V (V_{OL} = 0.4V and V_{OH} = 1.2V). The input threshold region of GTLP is between 1.05V and 0.95V with an externally supplied reference voltage (V_{REF}) of 1.0V. GTL has a specified threshold of 0.75V to 0.85V with a reference voltage requirement of 0.8V. Termination voltage levels are 1.2V for GTL and 1.5V for GTLP. A signal level comparison between GTL and GTLP is shown in Figure 2.

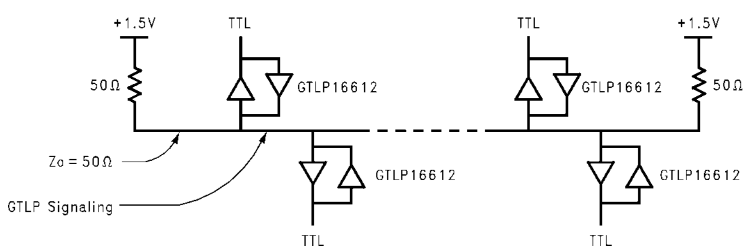

FIGURE 1.

FAST® is a registered trademark of Fairchild Semiconductor Corporation.

Background (Continued)

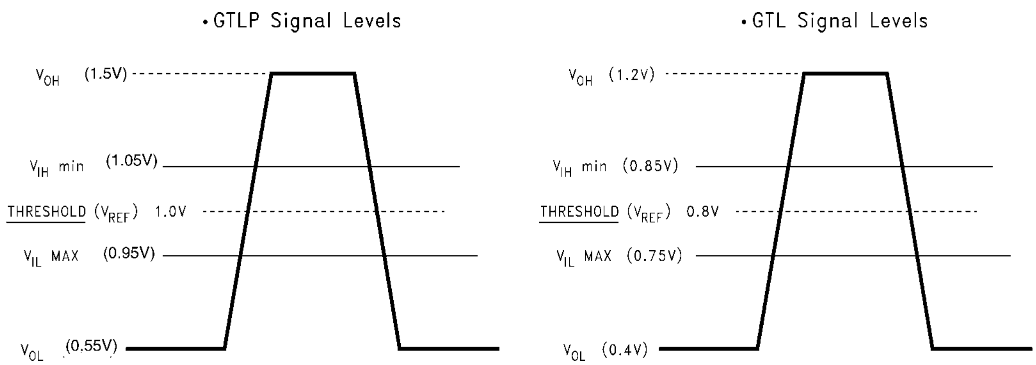

FIGURE 2.

The GTLP Advantage

Many backplane driving technologies are available, and Figure 3 provides a general comparison of today's backplane interface technologies on a speed versus load scale. This plot is an approximation of relative performance of devices in synchronous applications. In the light to moderately loaded backplane environment, GTLP is the logical successor to the high-performance TTL technologies (ABT, LVT, and FCT). The characteristics that make GTLP a high performance technology are: a reduced output swing level, low output capacitance, moderate drive, low output generated noise, and a tight input threshold region for high noise immunity. GTLP provides cost and power advantages in system backplanes that don't need all of the drive of BTL and ECL.

GTLP Features

The input/output (I/O) capacitance of a transceiver is typically the largest contributor to the distributed loading of a backplane. The effects of capacitive bus loading are: increased propagation time and greater drive requirements for the transceiver to switch the level of the bus. Thus, the heavier the load, the lower the throughput of the bus. Minimizing this distributed loading anywhere possible is imperative in high performance backplanes. Connectors for the daughter cards, stubs between the connector and the transceiver on the daughter card, and the transceiver outputs themselves all contribute to the distributed capacitive loading of the backplane trace. Unloaded backplane trace impedance is generally between 60Ω and 80Ω. The effects of distributed capacitive loads on the backplane can reduce the characteristic impedance by 30%–40%. Typical values of I/O capacitance for TTL and 5V output swing technologies can range from 8 pF–15 pF. GTLP I/O capacitance is only 6 pF in comparison. This difference results in a faster bus requiring less drive.

Advanced wave-shaping techniques have been implemented in GTLP to create gradual turn-on and off output characteristics with a controlled slew rate. This circuitry reduces the high frequency components inherent with fast signal transitions thereby improving both output switching noise (V_{OLP}/V_{OLV}, Crosstalk) and device radiated (EMI) noise performance. These controlled signal transitions coupled with properly matched line impedance can greatly reduce the bus settling time requirements on a GTLP bus.

GTLP is ideal for applications where power is a major concern. It is a low power alternative to GTL, ECL, BTL, and most TTL devices. The datasheet specification for I_{CC} is 40 mA maximum. This results in just over 2 mA per bit (18-bit function, i.e., GTLP16612 transceiver). GTLP dynamic power is typically 0.19 mA per MHz (per bit) or less. The small output swing and moderate drive of the GTLP devices results in low bus termination power. Termination power consumption of GTLP is lower than all other backplane transceiver families that use an active bus termination (i.e. BTL and ECL).

Backplane designs usually require the transceiver to provide some level of isolation between the daughter card and motherboard into which it is plugged. This isolation allows for the insertion or removal of a daughter card while the system is powered up and possibly during active backplane signaling. Transceivers that are selected for these applications must isolate the active bus from any power supply excursions on the daughter card and also maintain an output high impedance state during power cycling. GTLP outputs offer this type of isolation through control of either $\overline{OEAB}$ or $\overline{OEBA}$ pins. The output leakage over the power-up region, on the B Port, is typically less than I_{OZL} and I_{OZH} specifications of –10 µA and 5 µA respectively.

GTLP devices, such as the GTLP16612, are targeted primarily at backplane applications. The GTLP16612 is an 18-bit, bi-directional, TTL to GTLP universal bus transceiver. The universal designation infers multiple functionality. It can be used as a line driver/receiver, latch, or a flip-flop. An added advantage of the GTLP open drain output structure, apparent in multi-drop environments, is the ability to wire-OR outputs which provides increased functionality.

GTLP Features (Continued)

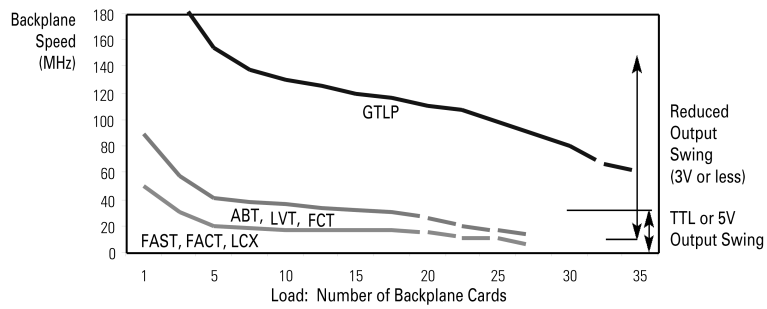

FIGURE 3.

Conclusion

Present and future voice, video, and data needs are putting ever-increasing demands on existing communications and computer systems. As these systems are replaced or upgraded, the need for a versatile, high-speed backplane becomes clear. The characteristics and features of GTLP make it an excellent choice in many high speed bus and backplane driving applications. GTLP has the speed and noise performance to be the upgrade path from existing TTL technologies, as well as the low power, low cost, and high bit-width functions to be an alternative to BTL and ECL in smaller backplanes.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative