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AC Characteristics of MM74HC High-Speed CMOS

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When deciding what circuits to use for a design, speed is most often a very important criteria. MM74HC is intended to offer the same basic speed performance as low power Schottky TTL while giving the designer the low power and high noise immunity characteristics of CMOS. In other words, HC-CMOS is about ten times faster than CD4000 and MM54C/MM74C metal-gate CMOS logic. Even though HC-CMOS logic does have speeds similar to LSTTL, there are some differences in how this family's speeds are specified, and how various parameters affect circuit performance.

To give the designer an idea of the expected performance, this discussion will include how the AC characteristics of high-speed CMOS are specified. This logic family has been specified so that in the majority of applications, the specifications can be directly applied to the design. Since it is impossible to specify a device under all possible situations, performance variations with power supply, loading and temperature are discussed, and several easy methods for determining propagation delays in nearly any situation are also described. Finally, it is useful to compare the performance of HC-CMOS to 74LS and to CD4000.

Data Sheet Specifications

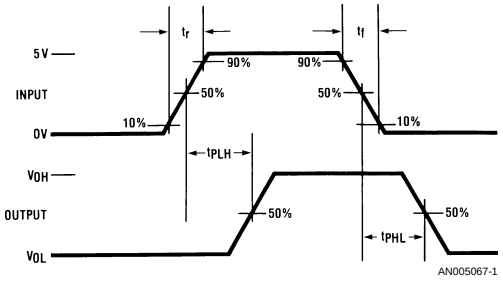
Even though the speeds achieved by this high-speed CMOS family are similar to LSTTL, the input, output and power supply characteristics are very similar to metal-gate CMOS. Because of this, the actual measurements for various timing parameters are not done the same way as TTL. The MM74HCT TTL input compatible circuits are an exception.

Standard HC-CMOS AC specifications are measured at V_{CC}=2.0V, 4.5V, 6.0V for room, military and commercial temperature ranges. Also HC is specified with LS equivalent supply (5.0V) and load conditions to enable proper comparison to low power Schottkey TTL. Input signal levels are ground to V_{CC} with rise and fall times of 6 ns (10% to 90%). Since standard CMOS logic has a logic trip point at about mid-supply, and the outputs will transition from ground to V_{CC}, timing measurements are made from the 50% points on input and output waveforms. This is shown in *Figure 1*. Using the mid-supply point gives a more accurate representation of how high-speed CMOS will perform in a CMOS system. This is different from the 1.3V measurement point and ground to 3V input waveforms that are used to measure TTL timing.

This output loading used for data sheet specifications fall into two categories, depending on the output drive capability of the specific device. The output drive categories are standard outputs (I_{OL}=4 mA) and bus driver outputs (I_{OL}=6 mA). Timing measurements for standard outputs are made using a 50 pF load. Bus driver circuits are measured using both a 50 pF and 150 pF load. In all AC tests, the test load capacitance includes all stray and test jig capacitances.

3-STATE measurements where the outputs go from an active output level to a high impedance state, are made using the same input waveforms described above, but the timing is measured to the 10% or 90% points on the output waveforms. The test circuit load is composed of a 50 pF capacitor and a 1 kΩ resistor. To test t_{PHZ}, the resistor is swiched to ground, and for t_{PLZ} it is switched to V_{CC}. The 3-STATE test circuit and typical timing waveforms are shown in *Figure 2*.

Measurements, where the output goes from the high impedance state to active output, are the same except that measurements are made to the 50% points and for bus driver devices both 50 pF and 150 pF capacitors are used.



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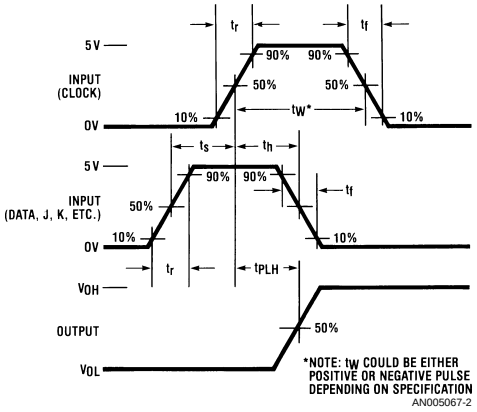

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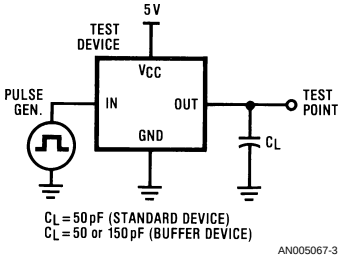
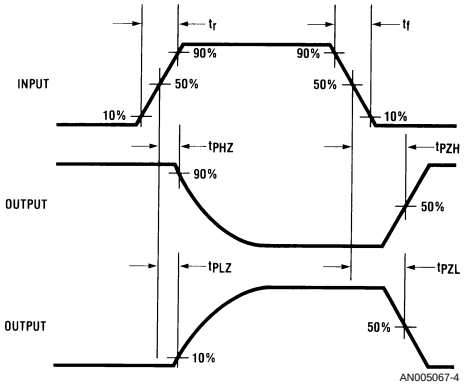
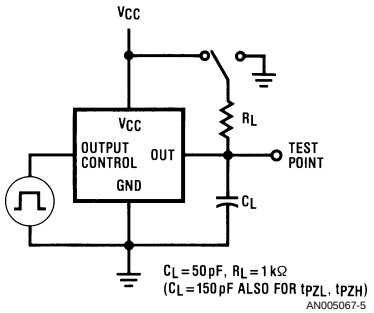


(c)

FIGURE 1. Typical Timing Waveform for (a) Propagation Delays, and (b) Clocked Delays. Also Test Circuit (c) for These Waveforms (t_r=t_f=6 ns)



(a)



(b)

FIGURE 2. Typical 3-STATE (a) Timing Waveforms and (b) Test Circuit for 74HC Devices

Note: Some early data sheets used a different test circuit. This has been changed or will be changed.

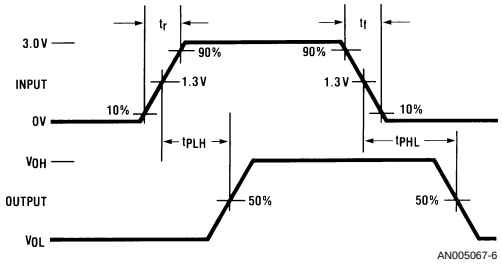
The /MM74HCT TTL input compatible devices are intended to operate with TTL devices, and so it makes sense to specify them the same way as TTL. Thus, as shown in *Figure 3*, typical timing input waveforms use 0–3V levels and timing measurements are made from the 1.3V levels on these signals. The test circuits used are the same as standard HC input circuits. This is shown in *Figure 3*. These measurements are compatible with TTL type specified devices.

Specifying standard MM74HC speeds using 2.5V input measurement levels does represent a specification incompatibility between TTL and most RAM/ROM and microprocessor speed specifications. It should not, however, present a de-

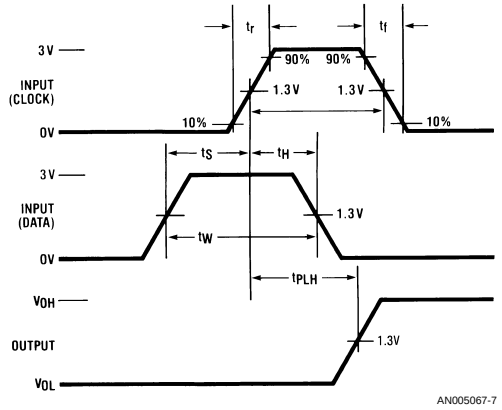
sign problem. The timing difference that results from using different measurement points is the time it takes for an output to make the extra excursion from 1.3V to 2.5V. Thus, for a standard high-speed CMOS output, the extra transition time should result, worst case, in less than a 2 ns increase in the circuit delay measurement for a 50 pF load. Thus in speed critical designs adding 1–2 ns safely enables proper design of HC into the TTL level systems.

Power Supply Affect on AC Performance

The overall power supply range of MM74HC logic is not as wide as CD4000 series CMOS due to performance optimization for 5V operation; however, this family can operate over a 2–6V range which does enable some versatility, especially when battery operated. Like metal-gate CMOS, lowering the power supply voltage will result in increased circuit delays. Some typical delays are shown in *Figure 4*. As the supply voltage is decreased from 5V to 2V, propagation delays increase by about two to three times, and when the voltage is increased to 6V, the delays decrease by 10–15%.



(a)



(b)

FIGURE 3. Typical Timing Waveforms for (a) 74HCT Devices (t_r=t_f=6 ns)Propagation Delays, and (b) Clocked Delays for 74HCT

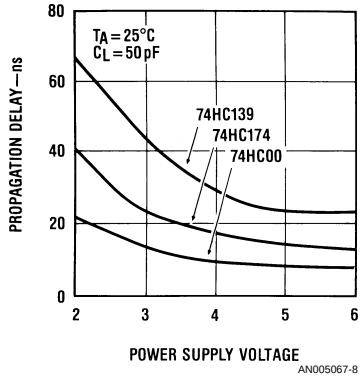


FIGURE 4. Typical Propagation Delay Variations of 74HC00, 74HC139, 74HC174 with Power Supply

In some designs it may be important to calculate the expected propagation delays for a specific situation not covered in the data sheet. This can easily be accomplished by using the normalized curve of *Figure 5* which plots propagation delay variation constant, t(V), versus power supply voltage normalized to 4.5V and 5V operation. This constant, when used with the following equation and the data sheet 5.0V specifications, yields the required delay at any power supply.

$t_{PD}(V) = [t(V)]\ [t_{PD}(5V)]$ 1.0

Where $t_{PD}(5V)$ is the data sheet delay and $t_{PD}(V)$ is the resultant delay at the desired supply voltage. This curve can also be used for the V_{CC}=4.5V specifications.

For example, to calculate the typical delay of the 74HC00 at V_{CC}=6V, the data sheet typical of 9 ns (15 pF load) is used. From *Figure 5* t(V) is 0.9, so the 6V delay would be 8 ns.

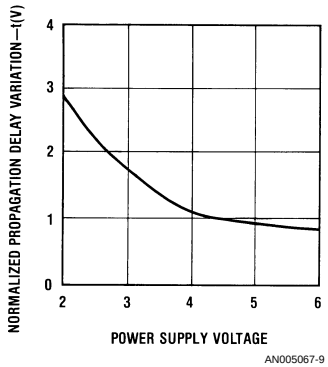


FIGURE 5. MM74HC Propagation Delay Variation Vs. Power Supply Normalized to V_{CC}=4.5V, and V_{CC}=5.0V

Speed Variation with Capacitive Loading

When high-speed CMOS is designed into a CMOS system, the load on a given output is essentially capacitive, and is the sum of the individual input capacitances, 3-STATE output capacitances, and parasitic wiring capacitances. As the load is increased, the propagation delay increases. The rate of increase in delay for a particular device is due to the increased charge/discharge time of the output and the load. The rate at which the delay changes is dependent on the output impedance of the MM74HC circuit. As mentioned, for high-speed CMOS, there are two output structures: bus driver and standard.

Figure 6 plots some typical propagation delay variations against load capacitance. To calculate under a particular load condition what the propagation delay of a circuit is, one need only know what the rate of change of the propagation delay with the load capacitance and use this number to extrapolate the delay from the data sheet vaue to the desired value. *Figure 7* plots this constant, t(C), against power supply voltage variation. Thus, by expanding on equation 1.0, the propagation delay at any load and power supply can be calculated using:

$t_{PD}(C,V) = [t(C)\ (C_L - 15\ pF)] + [t_{PD}(5V)\ t(V)]$ 1.1

Where t(V) is the propagation delay variation with power supply constant, $t_{PD}(5V)$ is the data sheet 4.5V (use (C_L–=50 pF) in equation) or 5V delay, C_L is the load capacitance and $t_{PD}(C,V)$ is the resultant propagation delay at the desired load and supply. This equation's first term is the difference in propagation delay from the desired load and the data sheet specification load. The second term is essentially equation 1.0. If the delay is to be calculated at V_{CC}=5V, then t(V)=1 and t(C)= 0.042 ns/pF (standard output), 0.028 ns/pF (bus output).

Using the previous 74HC00 example, the delay at V_{CC}=6V and a 100 pF load is:

t_{PD}(100 pF,6V)=(0.042)(100 — 15)+(0.9 X 9)=11 ns

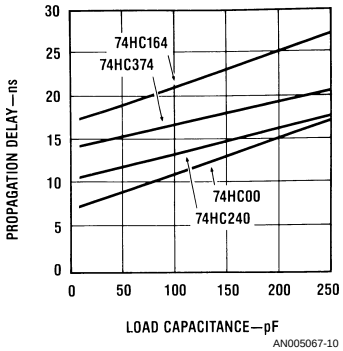


FIGURE 6. Typical Propagation Delay Variation With Load Capacitance for 74HC04, 74HC164, 74HC240, 74HC374

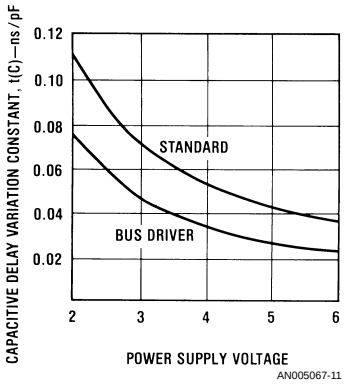


FIGURE 7. Propagation Delay Capacitance Variation Constant Vs. Power Supply

Speed Variations with Change in Temperature

Changes in temperature will cause some change in speed. As with CD4000 and other metal-gate CMOS logic parts, MM74HC operates slightly slower at elevated temperatures, and somewhat faster at lower temperatures. The mechanism which causes this variation is the same as that which causes variations in metal-gate CMOS. This factor is carrier mobility, which decreases with increase in temperature, and this causes a decrease in overall transistor gain which has a corresponding affect on speed.

Figure 8 shows some typical temperature-delay variations for some high-speed CMOS circuits. As can be seen, speeds derate fairly linearly from 25˚C at about −0.3%/C. Thus, 125˚C propagation delays will be increased about 30% from 25˚C.74HC speeds are specified at room temperature, −40 to 85˚C (commercial temperature range), and −55 to 125˚C (military range). In virtually all cases the numbers given are for the highest temperature.

To calculate the expected device speeds at any temperature, not specified in the device data sheet, the following equation can be used:

$t_{PD}(T)=[1 + ((T–25)(0.003))][t_{PD}(25)]$ 1.2

Where $t_{PD}(T)$ is the delay at the desired temperature, and $t_{PD}(25)$ is the room temperature delay. Using the 74HC00 example from the previous section, the expected increase in propagation delay when operated at V_{CC}=5V and 85˚C is [1+(85–25)(0.003)](10 ns)]=12 ns. The expected delay at some other supply can also be calculated by calculating the room temperature delay then calculating the delay at the desired temperature.

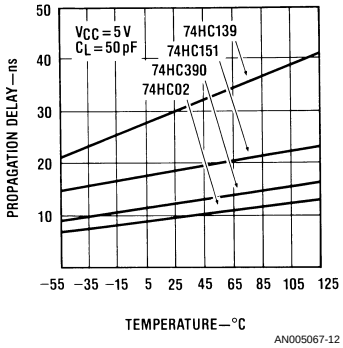


FIGURE 8. Typical Propagation Delay Variation With Temperature for 54HC02, 54HC390, 54HC139, 54HC151

Output Rise and Fall, Setup and Hold Times and Pulse Width Performance Variations

So far, the previous discussion has been restricted to propagation delay variations, and in most instances, this is the most important parameter to know. Output rise and fall times may also be important. Unlike TTL type logic families HC specifies these in the data sheet. High-speed CMOS outputs were designed to have typically symmetrical rise and fall times. Output rise and fall time variations track very closely the propagation delay variations over temperature and supply. *Figure 9* plots rise and fall time against output load at V_{CC}=5V and at room temperature. Load variation of the transition time is twice the delay variation because delays are measured at halfway points on the waveform transition.

Setup times and pulse width performance under different conditions may be necessary when using clocked logic circuits. These parameters are indirect measurements of internal propagation delays. Thus they exhibit the similar temperature and supply dependence as propagation delays. They are, however, independent of output load conditions.

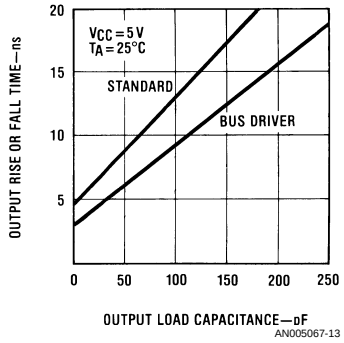


FIGURE 9. Typical Output Rise or Fall Time Vs. Load For Standard and Bus Driver Outputs

Input Rise and Fall Times

Another speed consideration, though not directly related to propagation delays, is input rise and fall time. As with other high-speed logic families and also CD4000B and 74C CMOS, slow input rise and fall times on input signals can cause logic problems.

Typically, small signal gains for a MM74HC gate is greater than 1000 and, if input signals spend appreciable time between logic states, noise on the input or power supply will cause the output to oscillate during this transition. This oscillation could cause logic errors in the user's circuit as well as dissipate extra power unnecessarily. For this reason MM74HC data sheets recommend that input rise and fall times be shorter than 500 ns at V_{CC}=4.5V.

Flip-flops and other clocked circuits also should have their input rise and fall times faster than 500 ns at V_{CC}=4.5V. If clock input rise and fall times become too long, system noise can generate internal oscillations, causing the internal flip-flops to toggle on the wrong external clock edge. Even if no noise were present, internal clock skew caused by slow rise times could cause the logic to malfunction.

If long rise and fall times are unavoidable, Schmitt triggers ('HC14/'HC132) or other special devices that employ Schmitt trigger circuits should be used to speed up these input signals.

Logic Family Performance Comparison

To obtain a better feeling of how high-speed CMOS compares to bipolar and other CMOS logic families, *Figure 10* plots MM74HC, 74LS and CD4000B logic device speeds versus output loading. HC-CMOS propagation delay and delay variation with load is nearly the same as LSTTL and about ten times faster than metal-gate CMOS. Utilizing a silicon-gate process enables achievement of LSTTL speeds, and the large output drive of this family enables the variation with loading to be nearly the same as LSTTL as well.

When comparing to CD4000 operating at 5V, HC-CMOS is typically ten times faster, and about three times faster than CD4000 logic operating at 15V. This is shown in *Figure 11*.

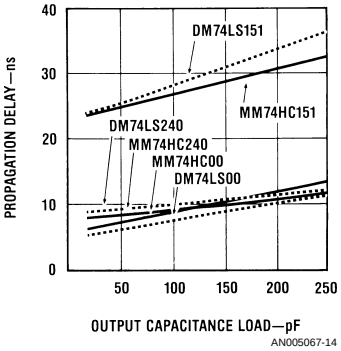


FIGURE 10. Comparison of LSTTL and High-Speed CMOS Delays

At 5V CD4000 has about a tenth the output drive of MM74HC and as seen in *Figure 10*, the capacitive delay variation is much larger.

As shown in *Figure 12*, the temperature variation of HC-CMOS is similar to CD4000. This is due to the same physical phenomenon in both families. The 74LS logic family has a very different temperature variation, which is due to different circuit parameter variations. One advantage to CMOS is that its temperature variation is predictable, but with LSTTL, sometimes the speed increases and other times speed decreases with temperature.

The inherent symmetry of MM74HC's logic levels and rise and fall times tends to make high to low and low to high propagation delay very similar, thus making these parts easy to use.

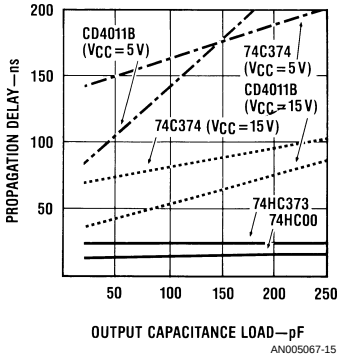


FIGURE 11. Comparison of Metal-Gate CMOS and High-Speed CMOS Delays

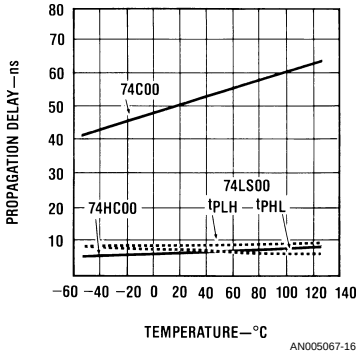


FIGURE 12. Comparison of HC-CMOS, Metal-Gate CMOS, and LSTTL Propagation Delay Vs. Temperature

Conclusion

High-speed CMOS circuits are speed compatible with 74LS circuits, not only on the data sheets, but even driving different loads. In general, HC-CMOS provides a large improvement in performance over older metal-gate CMOS.

By using some of the equations and curves detailed here, along with data sheet specifications, the designer can very closely estimate the performance of any MM74HC device. Even though the above examples illustrate typical performance calculations, a more conservative design can be implemented by more conservatively estimating various constants and using worst case data sheet limits. It is also possible to estimate the fastest propagation delays by using speeds about 0.4–0.7 times the data sheet typicals and aggressively estimating the various constants.

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