



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

Abstract

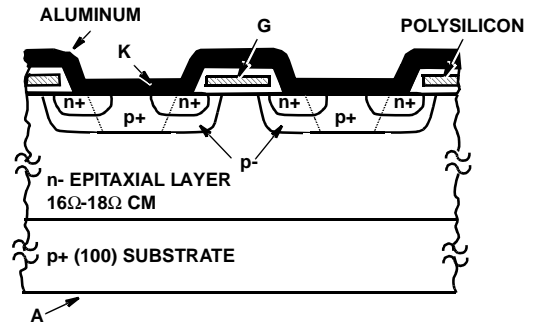
A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n⁻-epitaxial layer grown on a p⁺ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

Introduction

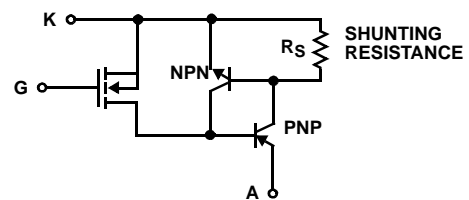
Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,^[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym IGBTs (Insulated Gate Bipolar Transistor).

This device, while similar in structure to the MOS-gated thyristor,^[4,5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.^[6] The structure and the equivalent circuit for the IGBTs are shown in Figure 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n⁻-epitaxial Si layer is grown on a p⁺ substrate instead of an n⁺ substrate. The heavily doped p⁺ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n⁺ and p⁺ regions, provides the shunting resistance shown in Figure 1(b). This has the effect of lowering the current gain of the n-p-n transistor (α_{n-p-n}) so that α_{n-p-n} + α_{p-n-p} < 1. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.^[6]

REGION	THICKNESS (μm)
EPI	60 - 62
n ⁺	1.0 - 1.5
p ⁻	3.5 - 4.0
p ⁺	5.0 - 5.5



(A) STRUCTURE



(B) EQUIVALENT CIRCUIT

In the remainder of this note we describe the operation and characteristics of this device.

Device Operation

The IGBT is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage V_A below the breakdown level V_{BF}. When V_A < V_{BF} and the gate voltage is larger than the threshold value V_{GT}, electrons pass into the n⁻-region (base of the p-n-p transistor). These electrons lower the potential of the n⁻-region, forward biasing the p⁺-n⁻ (substrate-epi-layer) junction, thereby causing holes to be injected from the p⁺ substrate into the n⁻ epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n-region, which dramatically reduces the on-resistance of the device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps α_{n-p-n} very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing α_{n-p-n} to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

Device Characterization

Two different lots of IGBT structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5mm and 3mm square devices were fabricated using a standard HEXFET geometry^[7] with a polysilicon gate electrode over an SiO₂ gate dielectric.

Several hundred IGBT were mounted in standard TO-3 and TO-66 packages and characterized under DC and pulsed conditions, as described below.

With zero gate bias, the forward characteristic of a IGBTs shows very low current (<1nA) up to about 390V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p⁺ substrate and the n⁻ epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100V because edge passivation was not used.

Figure 2(a) shows the MOSFET-like transfer characteristics of an IGBT in the low gate-voltage region. A noteworthy feature of the IGBT characteristic is the ~0.7V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the p⁺ - n⁻ (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Figure 2(b) shows the i(v) characteristic of an IGBT with V_G = 20V, and demonstrates the low on-resistance of the device (~0.084Ω at 20A). The on-resistance values of nearly all of the many IGBT fabricated to date have been less than 0.1Ω (at 20A) for the 3mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Figure 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (Fairchild, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",^[3] supplemented with some of the "best" of Fairchild' commercial and developmental MOSFETs. Note that the on-resistance of the IGBT is approximately 10 times less than that of a 400V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from IGBT designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)^[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present IGBT structures were designed for 600V, but V_{BF} was limited to 400V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the IGBTs on-resistance of less than 0.1 Ω even more attractive for high-voltage applications.

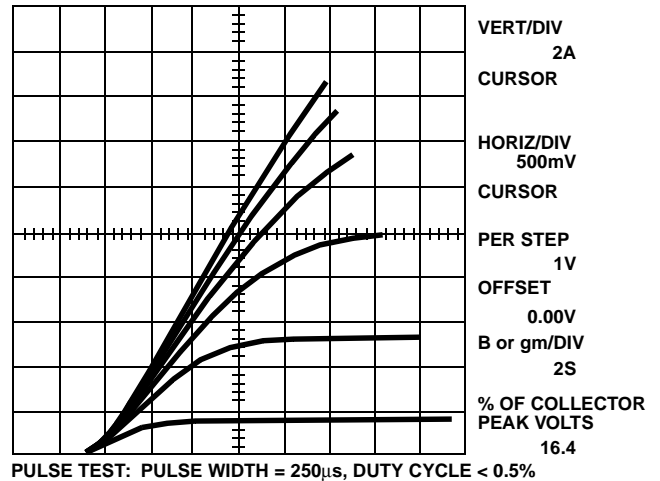


FIGURE 2A MOSFET - LIKE CHARACTERISTIC

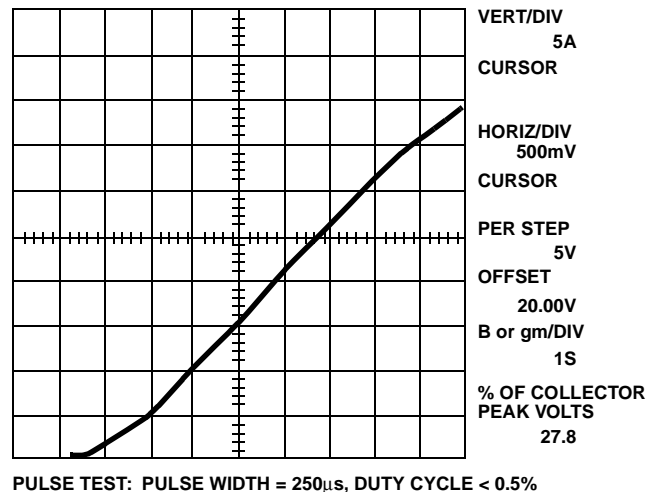


FIGURE 2B. IGBT i(v) with V_G = 20V

Transient Response Measurement

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1µs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Figure 4.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5µs to 20µs were observed, with the precise value depending on circuit conditions and the turn-off time of the gate pulse.

The n-p-n-p structure of the IGBTs is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10A - 30A in 3mm square chips. The magnitude of the latch-

ing current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off ($\sim 10\mu\text{s}$) permits anode currents up to 30A without latching. However, rapid gate turn-off ($\leq 1\mu\text{s}$) leads to latching at a much lower anode current level ($\sim 10\text{A}$) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing α_{n-p-n} to increase, and leading to the condition for latching, $\alpha_{n-p-n} + \alpha_{p-n-p} = 1$. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps α_{n-p-n} sufficiently low to avoid latching.

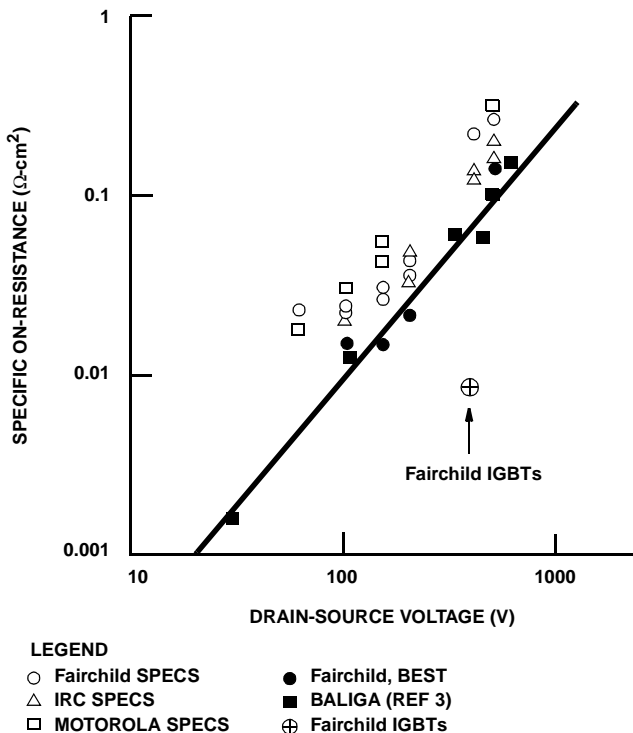


FIGURE 3. SPECIFIC ON-RESISTANCE vs DRAIN-SOURCE VOLTAGE CAPABILITY FOR STATE-OF-THE-ART POWER MOSFETS AND THE IGBTs

Summary

A new MOS-gate-controlled power device, the IGBTs, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on-resistance is due to conductivity modulation of the n epi layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

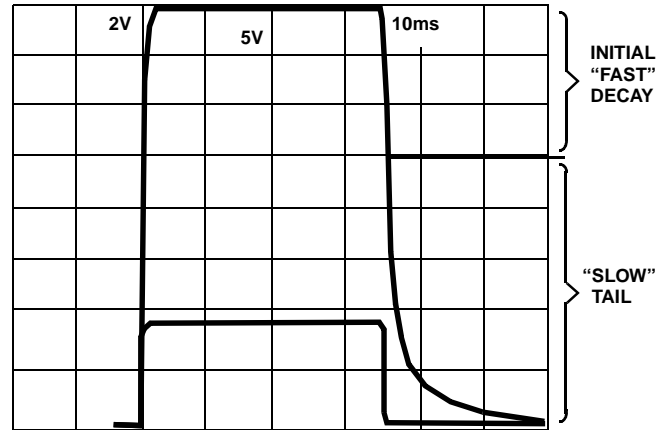


FIGURE 4. GATE VOLTAGE (LOWER TRACE) AND ANODE CURRENT (UPPER TRACE) WAVEFORMS FOR $i_A(\text{MAX}) = 8\text{A}$

Acknowledgment

The authors gratefully acknowledge the various helpful contributions of C. Nuese, D. Bergman, R. Ford, R. Jarl, G. Looney, P. Robinson, W. Romito, L. Skurkey, R. Stolzenberger, C. Wheatley, J. Wojslawowicz, and the staff of the Integrated Circuit Technology Center at RCA Laboratories. Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

References

- [1] M. L. Tarn, "On-Resistance Characterization of VDMOS Power Transistors", in IEDM Tech. Dig., 1981, pp 429-433.
- [2] C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High Breakdown Voltage", IEEE Trans. Electron Devices, Vol. ED-26, p 243, 1979.
- [3] B.J. Baliga, "Switching Lots of Watts at High Speeds", IEEE Spectrum, Vol. 18, p 42, Dec. 1981.
- [4] J. Tihanyi, "Functional Integration of Power MOS and Bipolar Devices", in IEDM Tech. Dig., 1980, p 75-78.
- [5] L. Leipold et al., "A FET Controlled Thyristor in SIPMOS technology", in IEDM Tech. Dig., 1980, pp 79-82.
- [6] H.W. Becke and C.F. Wheatley, "Power MOSFET With An Anode Region", U.S. Patent 4,364,073, issued Dec. 14, 1982 (expired).
- [7] H.W. Collins and B. Pelly, "HEXFET, A New Power Technology Cuts On-Resistance, Boosts Ratings", Electron. Des., Vol. 12, p 36, 1979.
- [8] S.M. Sze, Physics of Semiconductor Devices. 2nd Edition, New York; Wiley, 1981, p 120.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE _x [™]	FAST [®]	MICROWIRE [™]	SILENT SWITCHER [®]	UHC [™]
Bottomless [™]	FAST _r [™]	OPTOLOGIC [®]	SMART START [™]	UltraFET [®]
CoolFET [™]	FRFET [™]	OPTOPLANAR [™]	SPM [™]	VCX [™]
CROSSVOLT [™]	GlobalOptoisolator [™]	PACMAN [™]	STAR*POWER [™]	
DenseTrench [™]	GTO [™]	POP [™]	Stealth [™]	
DOME [™]	HiSeC [™]	Power247 [™]	SuperSOT [™] -3	
EcoSPARK [™]	I ² C [™]	PowerTrench [®]	SuperSOT [™] -6	
E ² CMOS [™]	ISOPLANAR [™]	QFET [™]	SuperSOT [™] -8	
EnSigna [™]	LittleFET [™]	QS [™]	SyncFET [™]	
FACT [™]	MicroFET [™]	QT Optoelectronics [™]	TinyLogic [™]	
FACT Quiet Series [™]	MicroPak [™]	Quiet Series [™]	TruTranslation [™]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative