Practical Feedback Loop Design Considerations for Switched Mode Power Supplies

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Abstract - Negative feedback control is used in switched-mode power supplies to regulate the output at a desired value. The optimum design of the feedback control loop starts with understanding the characteristics of the power stage, which can be analyzed using small-signal modeling. This paper explains the fundamental idea and meaning of small-signal modeling for power supplies and explores the small-signal transfer functions for basic converters and general compensation networks. It also discusses the practical issues with feedback loop design, including characteristics of the opto-coupler, effects of parasitic components, multiple output applications, and loop-gain measurement.

I. INTRODUCTION

Feedback control is a process of making a system variable conform to a particular desired value. This involves measuring the system variable, obtaining an error signal by comparing a system variable with the desired value and then influencing the value of the system variable using the error signal. Switched-mode power supply systems inevitably require feedback control to regulate the output voltage and/or current to a desired value. Fig. 1 shows a simplified feedback circuit for a boost converter. The output voltage should be kept constant, regardless of changes in the input voltage or load current. This is accomplished by building a feedback circuit that varies the converter control input (duty cycle of switch) in such a way that the difference between output voltage and desired reference value should be minimized.

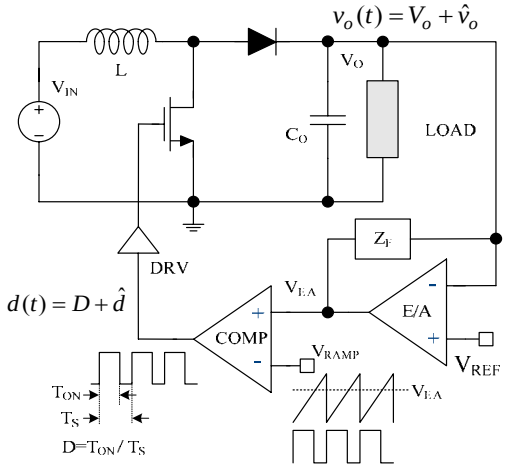


Fig. 1. Simplified feedback circuit of boost converter.

The output voltage of the boost converter running in steady state continuous conduction mode (CCM) is given as:

$$V_O = \frac{1}{1-D} V_{IN} \tag{1}$$

where D is the duty cycle and V_{IN} is the input voltage.

From Equation (1), it seems that the feedback compensation network only has to increase the duty cycle as output voltage decreases and vice versa. However, the output voltage does not always change in phase with the duty cycle. Assume that some AC variation is introduced in the converter duty cycle as:

$$d(t) = D + \hat{d}(t) = D + \hat{d}\sin(\omega t) \tag{2}$$

where the amplitude of AC variation $|\hat{d}|$ is much smaller than the steady-state duty cycle D.

Then, the output voltage is in a similar form as:

$$v_o(t) = V_O + \hat{v}_o(t) = V_O + \hat{v}_o \sin(\omega t + \phi) \tag{3}$$

where the amplitude of AC variation $|\hat{v}_o|$ is much smaller than the steady-state output voltage V_o and ϕ is the phase difference between duty cycle and output voltage variation.

Fig. 2 shows how the amplitude ratio and phase difference between the output voltage and duty cycle changes as frequency varies. Fig. 3 depicts how output voltage actually responds to the change of duty cycle at operating points A and B. When the duty cycle changes at a frequency of 1 kHz (point A), the output voltage changes in phase with the duty cycle. Output voltage changes in the reversed direction of duty cycle when the frequency of the AC variation is 10 kHz (point B). This means that the feedback system can be a positive feedback system, resulting in instability if the compensation network is not properly designed considering the frequency response of the power stage. That is why understanding the frequency response of the power stage is important for feedback loop design.

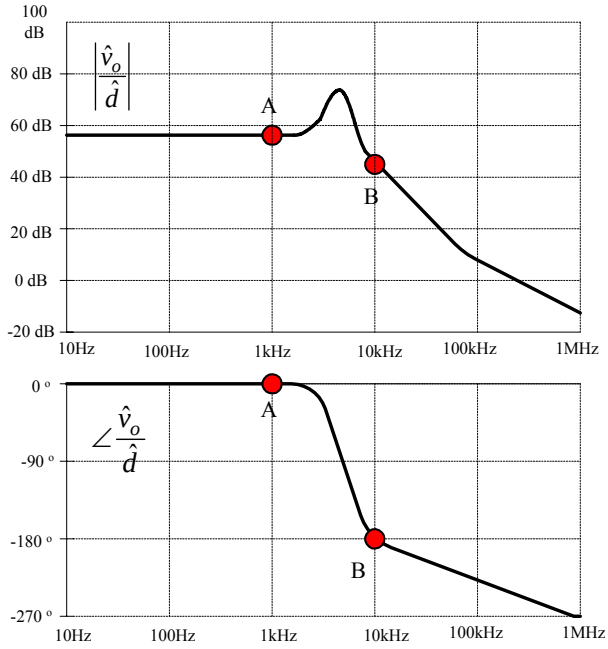


Fig. 2. Amplitude ratio and phase difference between the output voltage and duty cycle vs. frequency.

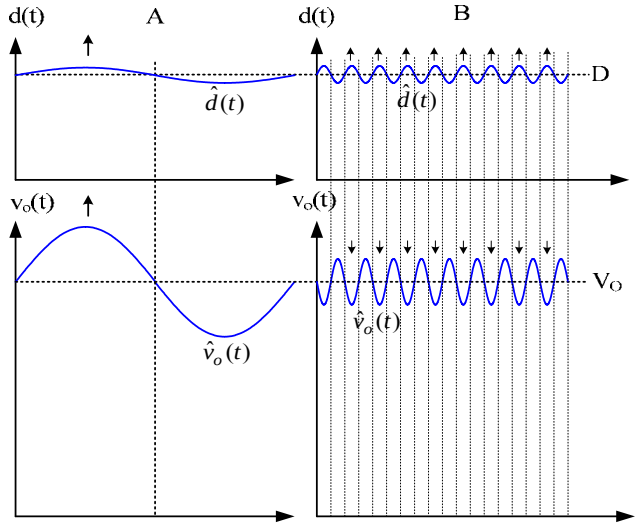


Fig. 3. Output voltage and duty cycle waveforms at operating points A, B.

To understand the frequency response, a dynamic model of the switching converter shows how variations in the input, the load current, or the duty cycle affect the output voltage according to the frequency. Even though the behavior of the SMPS is highly nonlinear, the system can be linearized using small-signal modeling, which is a common analysis technique in electrical engineering used to approximate the behavior of a nonlinear system with linear equations. This linearization is formed around a specific operating point and can be accurate for small excursions around this point. Any nonlinear system that can be described quantitatively, using a formula, can then be linearized about a bias point by taking partial derivatives of the formula with respect to all governing variables.

Small-signal modeling techniques include circuit averaging and state-space averaging methods. The key idea of these methods is to average converter waveforms over one switching cycle. This removes the switching harmonics and shows the low frequency AC components of the waveforms. A detailed discussion of small-signal modeling techniques is beyond the scope of this paper. This paper focuses on how to deal with the result of the small-signal modeling for feedback loop design.

II. STABILITY OF THE FEEDBACK LOOP

A converter with a feedback circuit can be modeled as shown in Fig. 4. The output of the converter is a function of input voltage, duty cycle, and output current. Since these three inputs are independent of each other, the output voltage variation can be expressed as a linear combination of the three inputs:

$$\hat{v}_o(s) = G_{vd}(s)\,\hat{d} + G_{vg}(s)\,\hat{v}_{in} - Z_{out}(s)\,\hat{i}_{load} \tag{4}$$

The transfer function from each input variation to the output voltage variation can be defined as:

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} \;:\; when\;\; \hat{v}_{in} = 0 \;\; and \;\; \hat{i}_{load} = 0 \tag{5}$$

$$G_{vg}(s) = \frac{\hat{v}_o}{\hat{v}_{in}} \;:\; when\;\; \hat{d} = 0 \;\; and \;\; \hat{i}_{load} = 0 \tag{6}$$

$$Z_{out}(s) = -\frac{\hat{v}_o}{\hat{i}_{load}} \;:\; when\;\; \hat{v}_{in} = 0 \;\; and \;\; \hat{d} = 0 \tag{7}$$

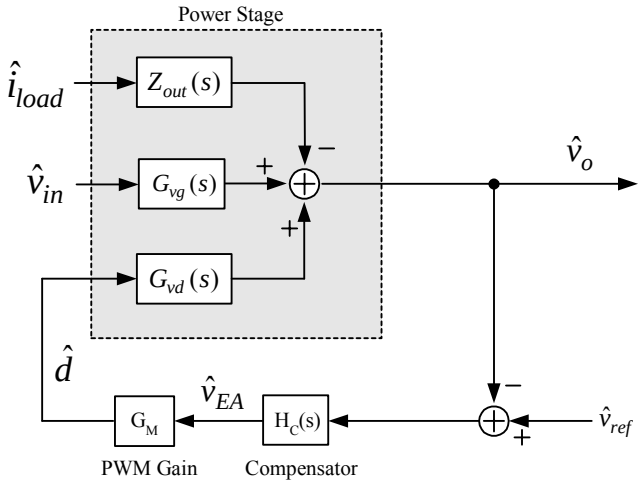


Fig. 4. Block diagram of converter with feedback.

Once the feedback loop is closed, the transfer functions from input voltage to output voltage and from output current to output voltage are expressed as:

$$\frac{\hat{v}_o}{\hat{v}_{in}} = \frac{G_{vg}(s)}{1+T(s)} : when\ \hat{i}_{load} = 0\ and\ \hat{v}_{ref} = 0 \quad (8)$$

$$\frac{\hat{v}_o}{\hat{i}_{load}} = -\frac{Z_{out}(s)}{1+T(s)} : when\ \hat{v}_{in} = 0\ and\ \hat{v}_{ref} = 0 \quad (9)$$

where T(s) is the loop gain, defined as the product of the gains along the path of the loop:

$$T(s) = G_{vd}(s)H_C(s)G_M \quad (10)$$

In Equations (8) and (9), the output variation can be reduced by increasing the loop gain. That is why the DC gain of the loop gain should be infinite to remove DC steady-state errors.

When the system is stable, the denominator, 1+T(s), has roots in the left half plane only. The Nyquist stability theorem is one method used to determine the stability of the feedback system since it tells how many right half plane poles exist in the feedback system. However, this method requires polar plot and it is, therefore, not easy to get design insight. Fortunately, the Nyquist method can be simplified as a phase margin method using bode plots if the loop gain T(s) has only one crossover frequency. Since converters inevitably employ low pass filter in the output stage, loop gain T(s) usually has only one crossover frequency and phase margin method is widely used for feedback loop design.

A bode plot is a plot of magnitude and phase of the transfer function as a function of frequency, where the magnitude is plotted in decibels and phase in degrees, respectively, while the frequency is shown on a logarithm scale. At a given frequency, the magnitude of product of two transfer functions is equal to the sum of the decibel magnitude of individual terms. Similarly, the phase of product of two transfer functions is equal to the sum of the phases of individual terms. This makes the bode plot a simple and powerful tool to illustrate and calculate the loop gain parameters.

Assuming the gain magnitude of loop gain T(s) crosses unity (0dB) only once, the system is stable if the phase lag at the crossover frequency is less than 180 degrees. At other frequencies, the phase lag may exceed 180 degrees and the system can be stable. The phase margin is the amount by which the phase lag at the crossover frequency is less than 180 degrees. The gain margin is the factor by which the gain is less than unity (0dB) at the frequency where phase lag is 180 degrees, as illustrated in Fig. 5. Typically, a phase margin of 45 degrees provides good response with little overshoot.

Even though the feedback system is stable when the phase lag is more than 180 degrees at frequencies below the crossover frequency; where the gain is greater than 0dB, it can be unstable when the loop gain decreases. This is "conditionally" stable and is not a good practice.

The characteristics of the power stage are determined by the choice of topology and control method, summarized in section III. The task of the feedback compensation network is to shape the loop gain such that it has a crossover frequency at the desired place with enough phase and gain margins for a good dynamic response, line and load regulation, and stability.

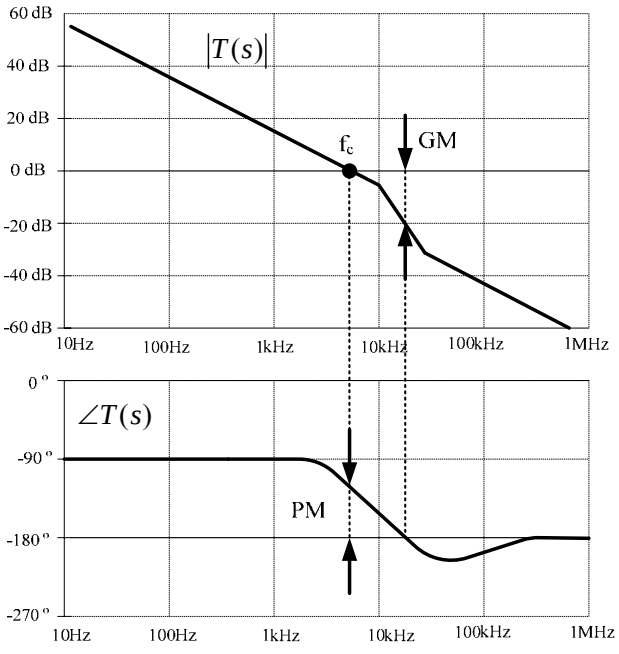


Fig. 5. Phase margin and gain margin.

III. CONTROL-TO-OUTPUT TRANSFER FUNCTIONS OF BASIC TOPOLOGIES

Among three transfer functions defined in the converter small-signal model in Fig. 4, the control-to-output transfer function is most important since it is directly related to the system stability, combined with the compensation network. Depending on the control method and operation mode, each converter has a different transfer function, which is discussed in this section. To simplify the analysis, the effective series resistances of the inductor and capacitor are ignored. The impact of effective series resistances are discussed in section V. The results of basic non-isolated converters can be adapted to the isolated version of the buck, boost, and buck-boost converters by introducing the turns ratio of the transformer.

It is worthwhile to note that the error amplifier output (v_{EA}) is used as a control input instead of duty cycle (d) in Table 1 and Table 2. It is to have a consistency when discussing the current-mode control, where duty cycle is not directly controlled. Instead, the peak of the inductor current is controlled by the output of the error amplifier. For voltage-mode control, the error amplifier output-to-duty-cycle transfer function is given as:

$$\frac{\hat{d}}{\hat{v}_{EA}} = \frac{1}{V_P} \tag{11}$$

where V_p is the peak-to-peak value of the sawtooth waveform shown in Fig. 6.

Voltage Mode Control in Continuous Conduction Mode (CCM)

Fig. 6 shows conceptually how voltage-mode control is implemented. The control input is the error amplifier output, which is compared to fixed sawtooth waveforms to generate the duty cycle. The control-to-output transfer functions of voltage-mode-controlled basic converters are summarized in Table 1. The buck converter exhibits control-to-output transfer function containing two poles. Meanwhile, the boost and buck boost converter exhibits two poles and a right-half-plane (RHP) zero. RHP zero causes the phase to drop by 90 degrees like a left half plane pole, while it increases the gain by 20 dB/decade, as a left half plane zero does. The right half plane zero moves with load condition and duty cycle, which makes it very difficult to have a high crossover frequency for a boost and buck boost converter operating in CCM as can be seen in the buck-boost converter example in Fig. 7. In Equations (13) and (14), the RHP zero is lowest at heavy load and low input voltage condition, which should be the worst case for the feedback loop design. Fig. 8 shows how the RHP zero affects the system dynamics using a buck boost converter example. Before the step change of the duty cycle is applied, the buck-boost converter operates in a steady state. When the step increase of the duty cycle takes place, the inductor current progressively increases. Initially, the average of the diode current decreases as the diode conduction time is reduced and the inductor current remains unchanged. This results in a dip in the output voltage temporarily, which is recovered as the inductor current increases to the steady state value. In this way, the presence of RHP zero causes the output to change in the opposite direction when the duty cycle changes fast, which limits the speed of the control loop.

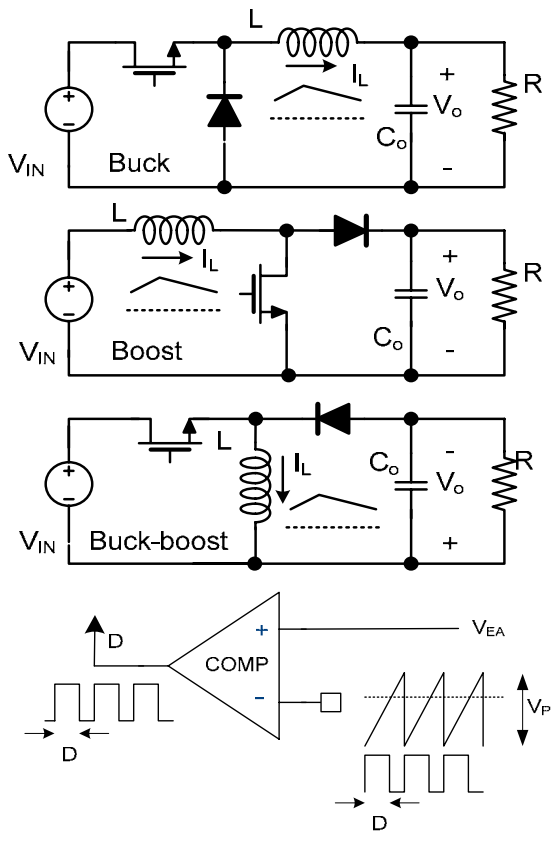


Fig. 6. Voltage-mode control of basic converters in CCM.

TABLE 1. CONTROL-TO-OUTPUT TRANSFER FUNCTIONS OF BASIC CONVERTERS (CCM, VOLTAGE-MODE CONTROL)

Topology	Control-to-Output Transfer Function	
Buck	$\frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{V_O}{V_P \cdot D} \cdot \frac{1}{1+\frac{s}{Q\omega_o}+(\frac{s}{\omega_o})^2}$ $\omega_o = 1/\sqrt{LC_o}\quad,\quad Q = R_L\sqrt{C_o/L}$	(12)
Boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{V_O}{V_P \cdot (1-D)} \cdot \frac{(1-s/\omega_{RHZ})}{1+\frac{s}{Q\omega_o}+(\frac{s}{\omega_o})^2}$ $\omega_{RHZ} = \frac{(1-D)^2 R_L}{L}$ $\omega_o = \frac{(1-D)}{\sqrt{LC_o}},\ Q = (1-D)R_L\sqrt{\frac{C_o}{L}}$	(13)
Buck-boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{V_O}{V_P \cdot D(1-D)} \cdot \frac{(1-s/\omega_{RHZ})}{1+\frac{s}{Q\omega_o}+(\frac{s}{\omega_o})^2}$ $\omega_{RHZ} = \frac{(1-D)^2}{D} \cdot \frac{R_L}{L}$ $\omega_o = \frac{(1-D)}{\sqrt{LC_o}},\ Q = (1-D)R_L\sqrt{\frac{C_o}{L}}$	(14)

Voltage Mode Control in Discontinuous Conduction Mode (DCM)

For DCM operation, the inductor current is reset to zero for every switching cycle, which makes the influence of inductor dynamics negligible. Therefore, the characteristics of DCM feature a single-pole transfer function as illustrated in Table 2. The right half plane zero does not exist for DCM operation since the inductor current is reset to zero for every switching cycle and a sudden change of the duty cycle does not cause temporary decrease of average diode current as shown in Fig. 9.

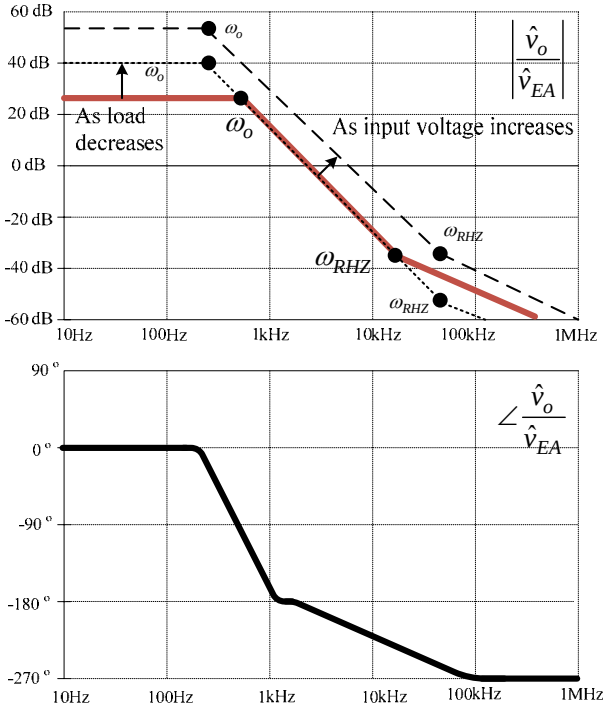


Fig. 7. Effect of RHP zero on control-to-output transfer function of buck boost converter

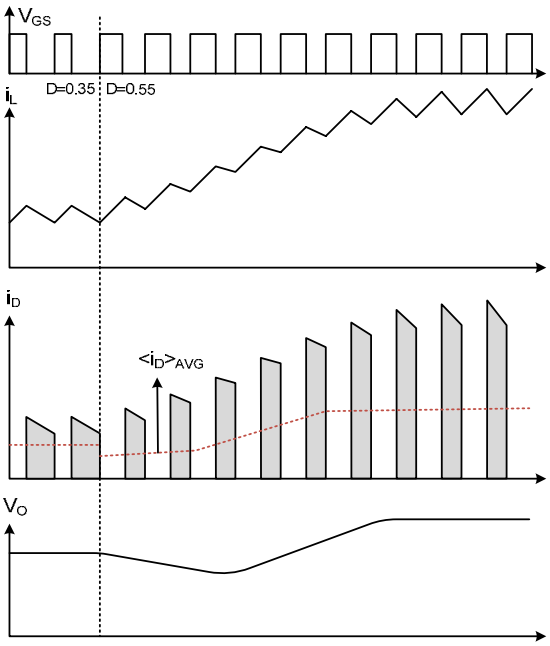


Fig. 8. Effect of RHP zero on system dynamics of buck-boost converter

TABLE 2. CONTROL-TO-OUTPUT TRANSFER FUNCTIONS OF BASIC CONVERTERS (DCM, VOLTAGE-MODE CONTROL)

Topology	Control-to-Output Transfer Function	
Buck	$\frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{2V_O}{V_P \cdot D} \cdot \frac{1-M}{2-M} \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{2-M}{1-M} \cdot \frac{1}{R_L C_O}$, $M = \frac{V_O}{V_{IN}}$	(15)
Boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{2V_O}{V_P \cdot D} \cdot \frac{M-1}{2M-1} \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{2M-1}{M-1} \cdot \frac{1}{R_L C_O}$, $M = \frac{V_O}{V_{IN}}$	(16)
Buck-boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{V_O}{V_P \cdot D} \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{2}{R_L C_O}$, $M = \frac{V_O}{V_{IN}}$	(17)

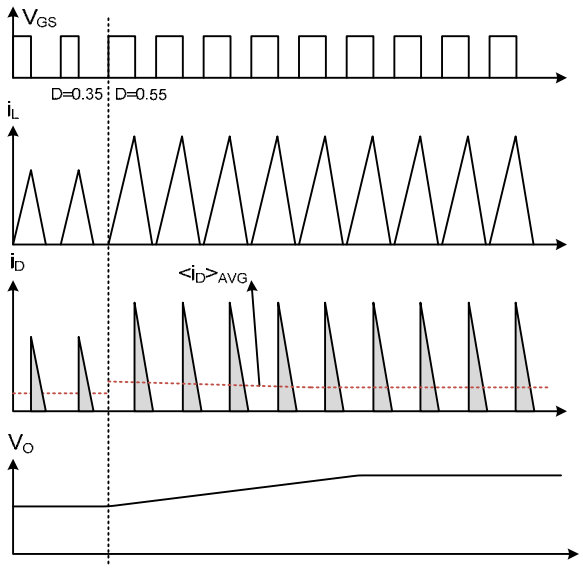


Fig. 9. No effect of RHP zero on system dynamics of a buck-boost converter

Current-Mode Control in CCM

Fig. 10 shows a simplified diagram for current-mode control. The error amplifier output determines the peak level of the switch current. A clock signal at the set input of the SR latch initiates the switching cycle and the switch is turned off when the sensed information of the switch current reaches the error amplifier output. Thus, the duty cycle is controlled indirectly.

The characteristics of current-mode-controlled topologies feature a single-pole transfer function as summarized in Table 3. It should be noted that the right half plane zero still exists for boost and buck-boost converters as long as these converters operate in CCM. The modulation gain K_M in Table 3 is defined as:

$$K_M = \frac{\Delta I_{DS}{}^{PK}}{\Delta V_{EA}} \tag{18}$$

When a sensing resistor is used to sense the current, the modulation gain is given as the conductance of the sensing resistor ($1/R_{CS}$).

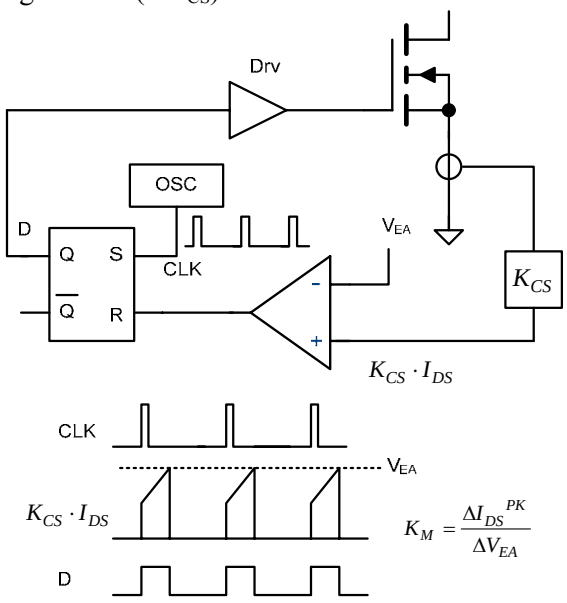


Fig. 10. Current-mode control of basic converters in CCM.

TABLE 3. CONTROL-TO-OUTPUT TRANSFER FUNCTION OF BASIC CONVERTERS (CCM, CURRENT-MODE CONTROL)

Topology	Control-to-Output Transfer Function	
Buck	$\frac{\hat{v}_o}{\hat{v}_{EA}} = K_M \cdot R_L \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{1}{R_L C_o}$	(19)
Boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = K_M \cdot \frac{(1-D)R_L}{2} \cdot \frac{(1-s/\omega_{RHZ})}{1+s/\omega_p}$ $\omega_{RHZ} = \frac{(1-D)^2 R_L}{L}$, $\omega_p = \frac{2}{R_L C_O}$	(20)
Buck-boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = K_M \cdot \frac{R_L \cdot (1-D)}{(1+D)} \cdot \frac{1-s/\omega_{RHZ}}{1+s/\omega_p}$ $\omega_{RHZ} = \frac{(1-D)^2}{D} \cdot \frac{R_L}{L}$, $\omega_p = \frac{(1+D)}{R_L C_O}$	(21)

Current-Mode Control in DCM

For current-mode control, DCM operation does not cause significant change in the transfer function. The characteristics of DCM feature a single-pole transfer function very similar to those with CCM operation as summarized in Table 4. The right half plane zero does not exist for DCM operation.

TABLE 4. CONTROL-TO-OUTPUT TRANSFER FUNCTION OF BASIC CONVERTERS (DCM, CURRENT-MODE CONTROL)

Topology	Control-to-Output Transfer Function	
Buck	$\frac{\hat{v}_o}{\hat{v}_{EA}} = 2K_M \cdot V_o \cdot \frac{1-M}{2-3M} \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{2-3M}{1-M} \cdot \frac{1}{R_L C_o}$	(22)
Boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = 2K_M \cdot V_o \cdot \frac{M-1}{2M-1} \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{2M-1}{M-1} \cdot \frac{1}{R_L C_o}$	(23)
Buck-boost	$\frac{\hat{v}_o}{\hat{v}_{EA}} = K_M \cdot V_o \cdot \frac{1}{1+s/\omega_p}$ $\omega_p = \frac{2}{R_L C_O}$	(24)

IV. COMPENSATION NETWORK

The task of the feedback compensation network is to shape the loop gain such that it has a crossover frequency at a desired place with enough phase and gain margins for good dynamic response, line and load regulation, and stability. As observed in the previous section, low-frequency gains (DC gains) of the control-to-output transfer functions are not infinite. Therefore, an integrator is inevitably required for the compensation network to make the loop gain infinite at zero frequency (DC). However, the integrator brings about a 90-degree phase drop; zeros should be employed in the compensation to compensate the phase drop.

According to the number of zeros and poles, the compensation network can be classified into three types.

Type-I Compensation

This is the simplest configuration, which is illustrated in Fig. 11. It contains only an integrator:

$$H_C(s) = \frac{\omega_I}{s} \tag{25}$$

where ω_I is the integrator gain.

Type I can be used only for the low-bandwidth applications because the crossover frequency is always limited below the pole of the power-stage transfer function, as shown in Fig. 11.

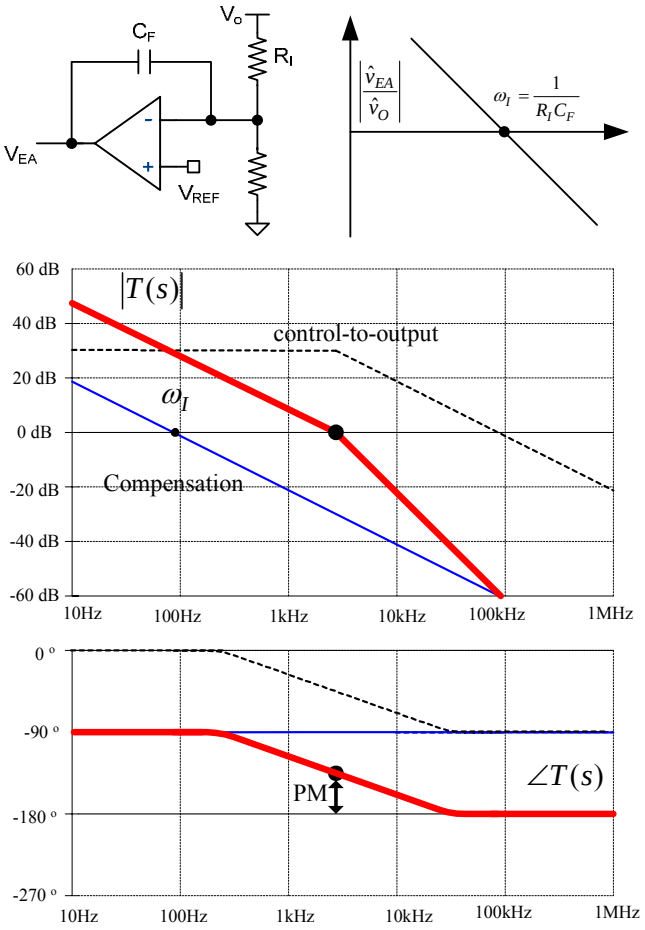


Fig. 11. Type-I compensation.

Type-II Compensation

It contains an integrator, one pole, and one zero, as depicted in Fig. 12. The transfer function is given as:

$$H_C(s) = \frac{\omega_I}{s} \cdot \frac{(1+s/\omega_{CZ1})}{(1+s/\omega_{CP1})} \tag{26}$$

where ω_I is the integrator gain, ω_{CZ1} is the compensation zero and ω_{CP1} is the compensation pole.

The zero is introduced to compensate the phase drop caused by the integrator, while the pole is used to attenuate the switching ripple. Type-II compensation is typically used for a system with a one-pole control-to-output transfer function. It can provide a maximum of 90° phase margin to the one-pole system with a crossover frequency at higher than the power stage pole, as shown in Fig. 12.

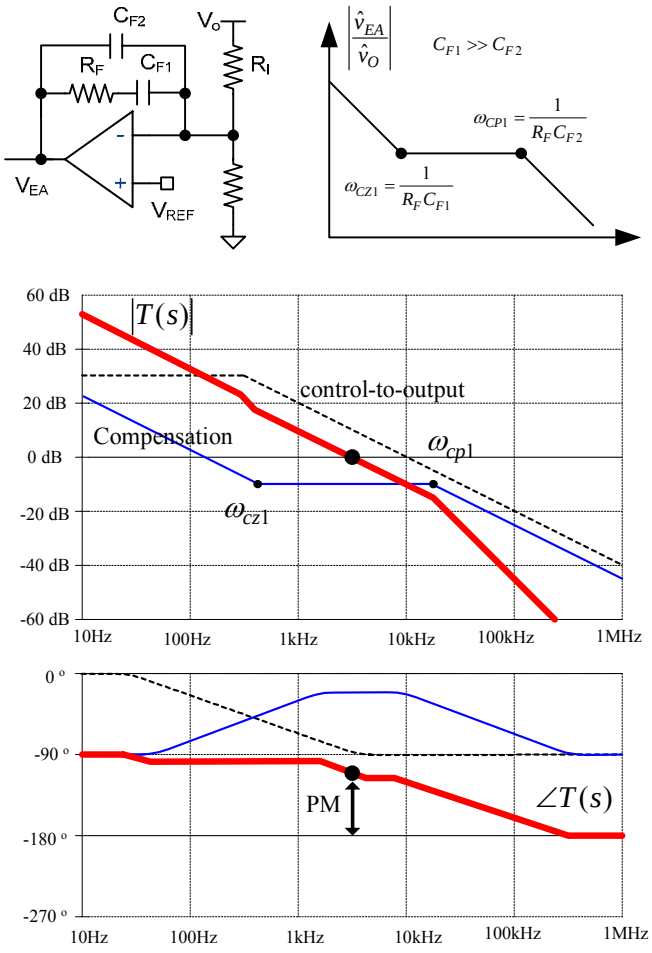


Fig. 12. Type-II compensation.

Type III is typically used for a double-pole control-to-output transfer function, where type-III compensation can provide a maximum of 90° phase margin with a crossover frequency higher than the double pole, as shown in Fig. 13.

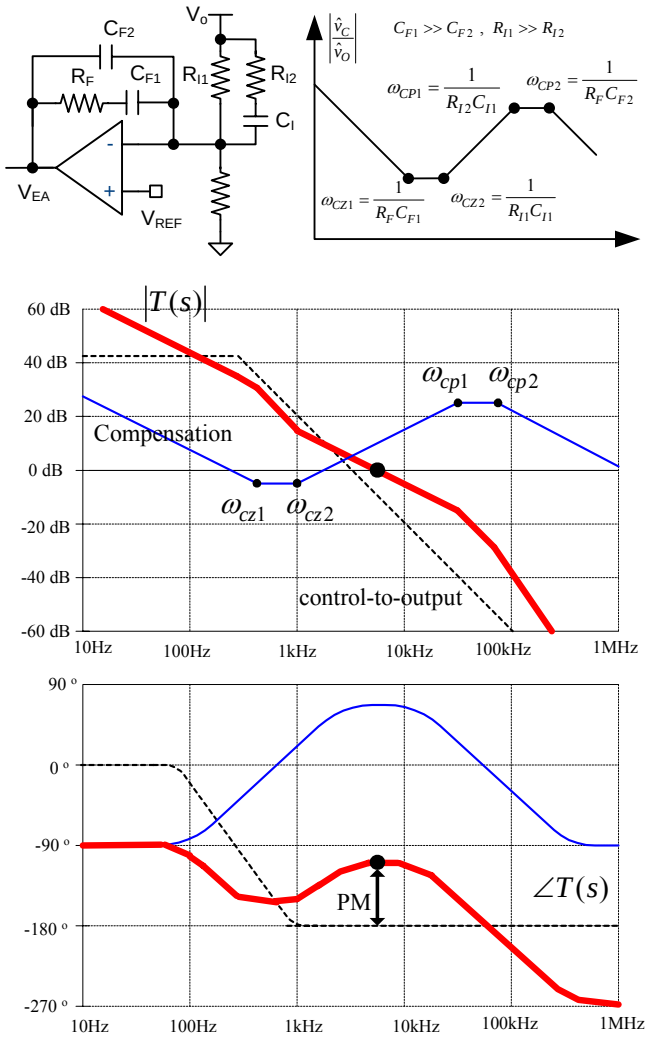


Fig. 13. Type-III compensation.

Type-III Compensation

It contains an integrator, two poles, and two zeros, as depicted in Fig. 13. The transfer function is given as:

$$H_C(s) = \frac{\omega_I}{s} \cdot \frac{(1 + s/\omega_{CZ1})}{(1 + s/\omega_{CP1})} \qquad (27)$$

where ω_I is the integrator gain, ω_{CZ1} and ω_{CZ2} are the compensation zeros and ω_{CP1} and ω_{CP2} are the compensation poles.

V. PRACTICAL ISSUES IN FEEDBACK LOOP DESIGN

Effective Series Resistance of a Capacitor

An electrolytic capacitor is widely used for the output capacitor of a converter power stage since large capacitance can be obtained at a relatively low cost. However, an electrolytic capacitor has a large effective series resistance (ESR) compared to other capacitors, such as film and ceramic. Some of the capacitor manufacturers provide dissipation factor (tanδ)

specifications rather than an actual ESR value. ESR can be approximated from:

$$R_C = \frac{\tan\delta}{2\pi f \cdot C} \tag{28}$$

where f is the frequency given in the datasheet for dissipation factor (usually 120Hz) and C is the capacitor value.

Usually the ESR calculated from Equation (28) is larger than the measured value at the switching frequency since the ESR contains a frequency-dependent part — the oxide layer resistance. Fig. 14 shows the typical impedance measurement of the electrolytic capacitor (Rubycon YXG family, 1000μF, 25V). Table 5 and Table 6 show the dissipation factor and ESR specification of the electrolytic capacitor (Rubycon YXG family).

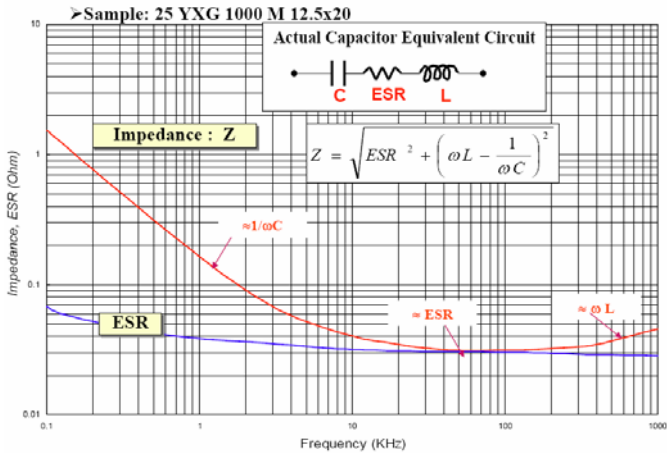


Fig. 14. Equivalent circuit and ESR of an electrolytic capacitor (Rubycon datasheet, YXG family).

TABLE 5. DISSIPATION FACTOR SPECIFICATION OF ELECTROLYTIC CAPACITOR (RUBYCON DATASHEET, YXG FAMILY)

Rated Voltage (V)	6.3	10	16	25	35	50	63	100
tan δ	0.22	0.19	0.16	0.14	0.12	0.10	0.09	0.08

TABLE 6. ESR SPECIFICATION OF AN ELECTROLYTIC CAPACITOR (RUBYCON DATASHEET, YXG FAMILY)

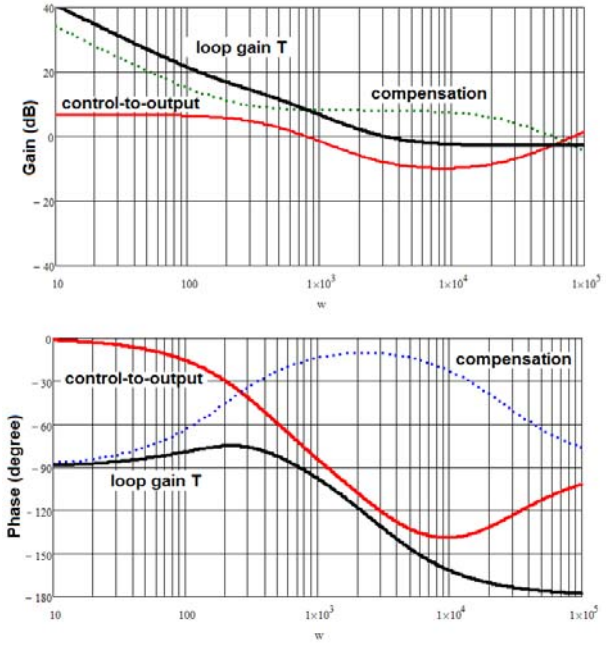
Rated capacitance (μF)	Size φD×L(mm)	Rated voltage 25V(1E) Impedance (Ω MAX) 20℃, 100kHz	−10℃, 100kHz
680	12.5×16	0.049	0.16
820	10×23	0.042	0.17
1000	10×28	0.031	0.12
■ 1000	12.5×20	0.035	0.12
1000	16×16	0.042	0.12
1200	18×16	0.043	0.11

The ESR of an output capacitor introduces an ESR zero (ω_{ERZ}) to the power-stage transfer function as:

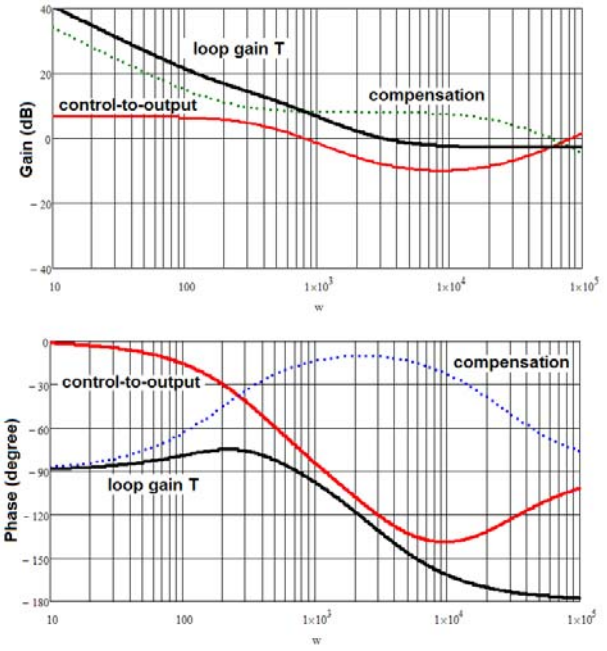
$$\left.\frac{\hat{v}_o}{\hat{v}_{EA}}\right|^{ESR} = \frac{\hat{v}_o}{\hat{v}_{EA}} \cdot \left(\frac{s}{\omega_{ERZ}} + 1\right) \tag{29}$$

where $\omega_{ERZ} = 1/(R_C C_O)$ and $\hat{v}_o/\hat{v}_{EA}$ is the control-to-output transfer function ignoring the ESR of the output capacitor, summarized in Table 1~Table 4.

The ESR zero occurs around or below the desired crossover frequency and has a wide range of variation, especially with the temperature as shown in Table 6. Fig. 15 shows how the ESR zero affects the system stability. At 25°C, the ESR zero (25krad/s) is much higher than the bandwidth (3krad/s) and the system is stable with a phase margin of 45°. However, at -10°C, the ESR zero moves down to 6.25krad/s making the system unstable. Therefore, enough gain margin should be considered when designing the feedback loop.



(a) Stable (PM=45°, ESR=0.035Ω, w_{ESR}=25krad/s at 25°C)



(b) Unstable (ESR=0.12Ω, w_{ESR}=6.25krad/s at -10°C)

Fig. 15. Effect of ESR zero variation on system stability (ESR=0.12Ω, w_{ESR}=6.25krad/s at 25°C)

The Effect of Post LC Filter Stage

Due to the relatively large ESR of electrolytic capacitors, additional LC filter stages (post filter) are typically used to meet the output ripple specification, as shown in Fig. 16. This method is more effective than using a number of capacitors in parallel to reduce the ESR. However, once an LC filter is added, it introduces a double pole in the control-to-output transfer function, reducing the phase by 180 degrees, as shown in Fig. 17. Considering the ESR of each capacitor, the control-to-output transfer function of the power stage is obtained as:

$$G_{PLC} = \left.\frac{\hat{v}_{op}}{\hat{v}_{EA}}\right|^{PLC} = \frac{\hat{v}_o}{\hat{v}_{EA}} \cdot \frac{1+\dfrac{1}{\omega_{ZER1}}}{1+\dfrac{s}{Q\omega_{op}}+\left(\dfrac{s}{\omega_{op}}\right)^2} \qquad (30)$$

$$\text{where } \omega_{op} = \sqrt{\frac{C_{O1}+C_{O2}}{L_P \cdot C_{O1}C_{O2}}}\ ,\ Q = \frac{R_{Load}}{L_P}$$

Even for current-mode controlled buck converters whose control-to-output transfer function is first order, this additional phase drop by 180° makes it almost impossible to place the crossover frequency above the double pole of the post LC filter. Thus, extra care should be taken not to place the corner frequency too low when using the post filters. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency to have a proper switching ripple attenuation while keeping reasonable bandwidth.

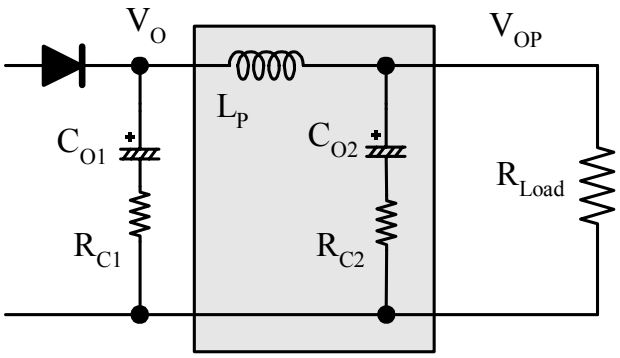


Fig. 16. Post LC filter.

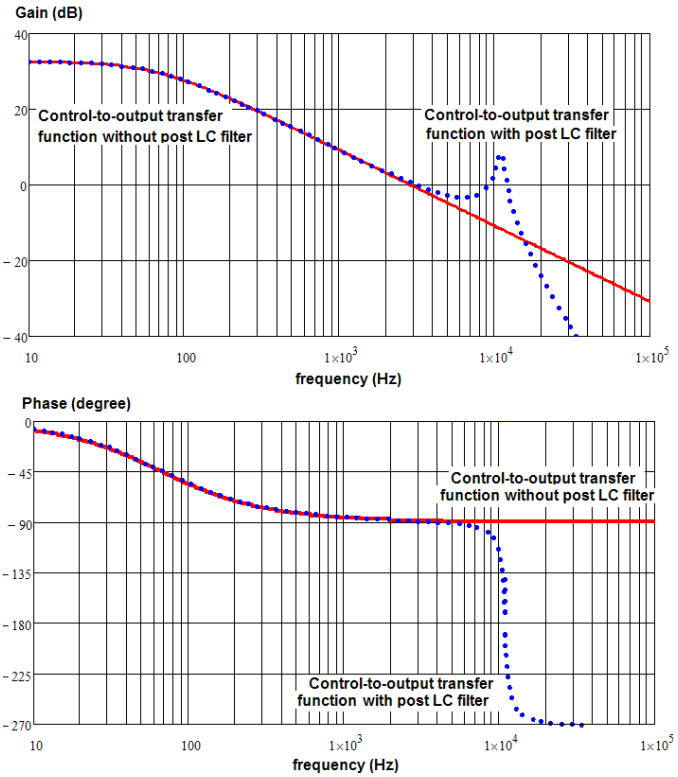


Fig. 17. Effect of post LC filter on the power-stage transfer function.

Characteristics of Opto-Couplers

For most off-line power supply applications, an opto-coupler is generally used to transfer output voltage information to the primary side where the PWM controller is located. The opto-coupler is usually modeled as an ideal current-controlled current source with a fixed current transfer ratio (CTR) for the feedback control design. However, extra care should be taken

when using an opto-coupler. First, the CTR is not a fixed value and has a large variation. For example, the CTR specification of the FOD817A is from 80 to 160 for a given bias current of 5 mA. Moreover, the CTR is highly dependent on the bias current, as shown in Fig. 18. There needs to be enough gain margin in the feedback loop design to accommodate the variation of CTR. Note that the opto-coupler introduces a mid-frequency pole due to the collector-emitter junction capacitance. Since the collector-base junction in a photo-transistor is used as a light detector, its area is relatively large, which introduces a large effective collector-emitter junction capacitance. The typical collector-emitter junction capacitance is 10~30 nF for the FOD817A, which brings a pole at around 10 kHz with a bias resistor of 1 kΩ. This pole can occur around the desired crossover frequency, making the system unstable. Therefore, this additional pole should be considered when designing the compensation network.

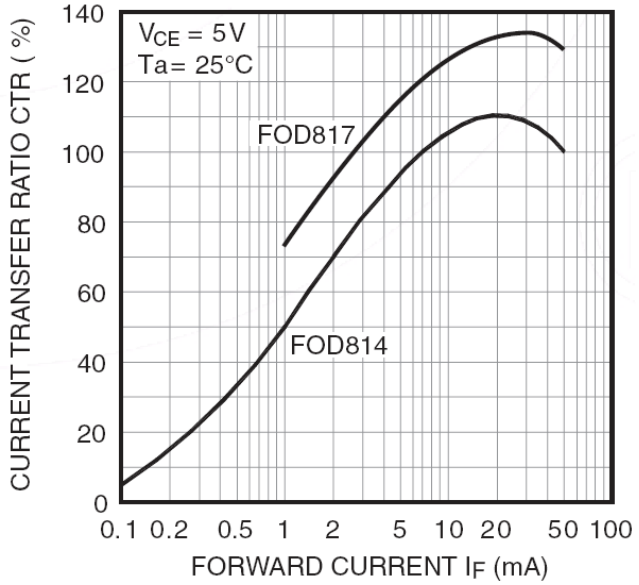
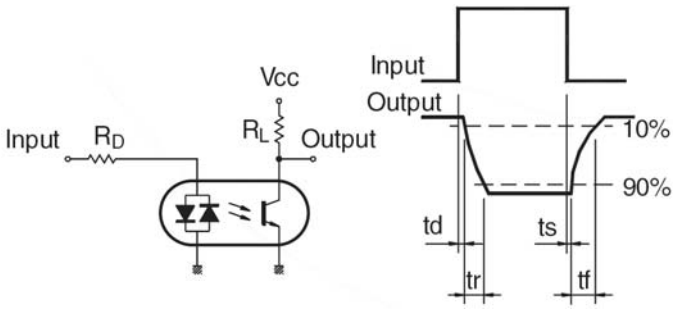


Fig. 18. Opto-coupler CTR variation with bias current.



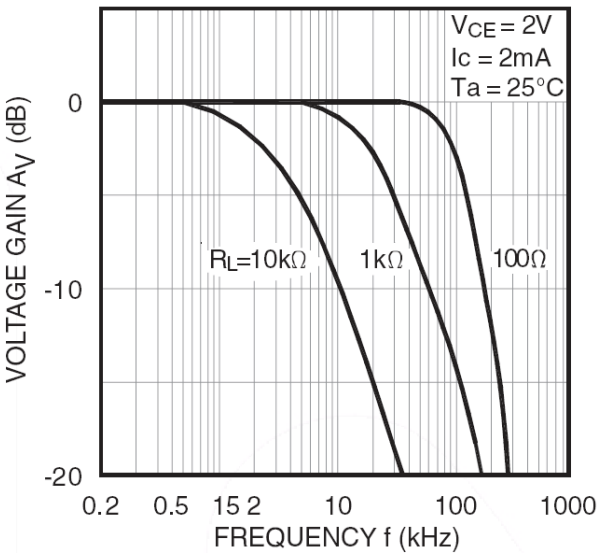


Fig. 19. Frequency response of opto-coupler and the test circuit.

Using Shunt Regulator KA431

Shunt regulator KA431 is widely used to implement a feedback compensation network for SMPS since it includes a reference, error amplifier, and driver in a small three-pin package. The current driver stage, especially, makes it very suitable to drive an opto-coupler for off-line SMPS applications. Fig. 20 shows a typical type-II compensation circuit, combined with an opto-coupler. The difference between the internal reference and the divided-down output voltage is amplified using the internal error amplifier. The output of the error amplifier is converted into current, which flows through the opto diode, transferring the error signal to the primary side. By sending the error signal instead of the output voltage information directly, the effect of the high-CTR variation can be minimized.

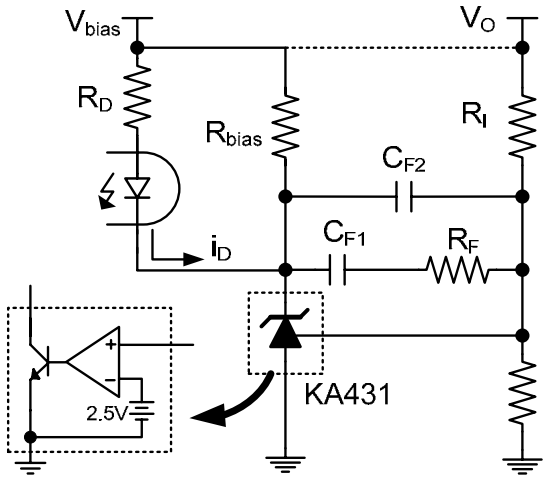


Fig. 20. Application circuit with KA431.

The bias voltage for the KA431 can be obtained from a stable DC voltage or output voltage, as illustrated in Fig. 20. Depending on where the bias voltage is obtained, the transfer function of the compensation network changes. The linearized small-signal equation for the opto-diode current and output voltage is given as:

$$\hat{i}_{D=}\frac{1}{R_D}\hat{v}_{bias}+\frac{(R_F+\frac{1}{sC_{F1}})//\frac{1}{sC_{F2}}}{R_D R_1}\hat{v}_o \tag{31}$$

When V_{bias} is a stable DC voltage independent of the output voltage, $\hat{v}_{bias}$ is zero and the transfer function of the compensation network is given as:

$$\frac{\hat{i}_D}{\hat{v}_o}=\frac{\omega_I}{s}\cdot\frac{s/\omega_{CZ1}+1}{s/\omega_{CP1}+1} \tag{32}$$

where $\omega_I=\frac{1}{R_1 R_D C_F}$, $\omega_{CZ1}=\frac{1}{R_{F1}C_F}$, and $\omega_{CP1}=\frac{1}{R_F C_{F2}}$ assuming C_{F1} is much larger than C_{F2}.

Whereas, when V_{bias} is connected to the output voltage, $\hat{v}_{bias}$ equals $\hat{v}_o$, introducing another proportional gain term and the transfer function of Equation (32) is changed to:

$$\frac{\hat{i}_D}{\hat{v}_o}=\frac{\omega_I}{s}\cdot\frac{(s/\omega_{CZ1}+1)\cdot(s/\omega_{CZ2}+1)}{s/\omega_{CP1}+1} \tag{33}$$

where $\omega_I=\frac{1}{R_1 R_D C_F}$, $\omega_{CZ1}=\frac{1}{R_F C_{F1}}$, $\omega_{CP1}=\frac{1}{R_F C_{F2}}$, and $\omega_{CZ2}=\frac{1}{R_I C_{F2}}$, assuming R_F is much larger than R_I.

As observed in Equation (33), using C_{F2} in parallel with R_F and C_{F1} (when V_{bias} is connected to the output voltage) introduces one more zero to type-II compensation. This configuration is not recommended because it makes the feedback compensation more complicated. Instead, it is typical to make a high-frequency pole using a capacitor and resistor in the primary side, as shown in Fig. 21. Then the compensation network becomes type II, calculated as:

$$\frac{\hat{v}_{EA}}{\hat{v}_o}=\frac{\omega_I}{s}\cdot\frac{(s/\omega_{CZ1}+1)}{(s/\omega_{CP1}+1)} \tag{34}$$

where $\omega_I=\frac{R_B}{R_1 R_D C_F}$, $\omega_{CZ1}=\frac{1}{R_F C_F}$, and $\omega_{CP1}=\frac{1}{R_B C_B}$.

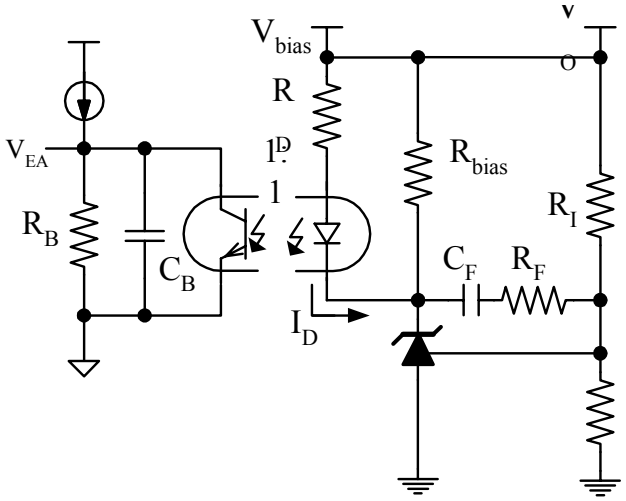


Fig. 21. Typical application circuit with KA431.

The compensation path through the resistor R_D also brings about very interesting features when a post LC filter is used and R_D is connected before the post filter stage, as shown in Fig. 22. The path through R_D allows proportional gain without the double pole caused by the post LC filter. This configuration is very effective in increasing the phase margin when the crossover frequency is close to the double pole of post LC filter.

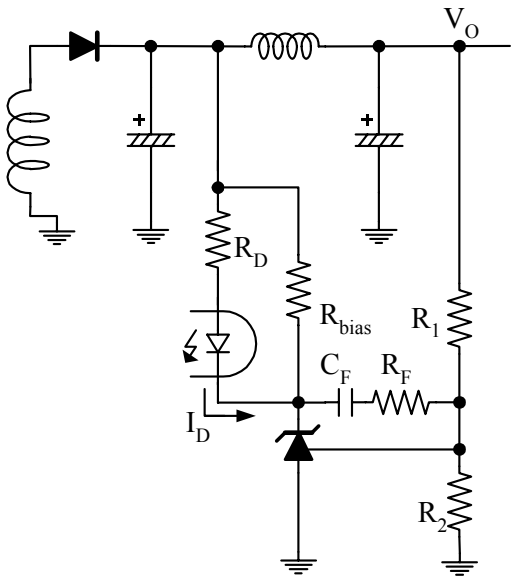


Fig. 22. Typical application circuit with KA431 using a post LC filter.

Multiple Outputs with Transformer Windings

When multiple outputs exist for a converter using multiple transformer windings, the control-to-output transfer functions in Table 1~Table 4 should be modified accordingly. For multiple output flyback converters, all

the outputs are in parallel from an equivalent circuit point of view since the magnetizing current should feed all the outputs. Therefore, all of the output impedances should be considered, even when only one output is sensed for feedback compensation, as shown in Fig. 23.

However, for multiple output forward converters, all the outputs are independent of each other from an equivalent circuit point of view since the input voltage source feeds all of the outputs. Thus, only the feedback controlled output needs to be considered for compensation network design as shown in Fig. 24.

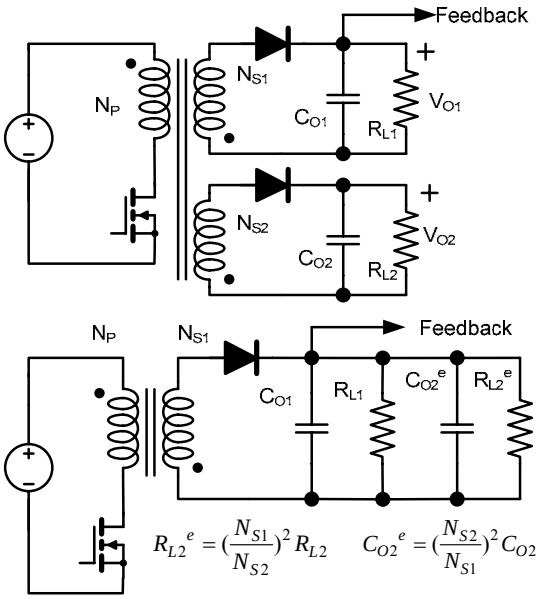


Fig. 23. Multiple output flyback converter.

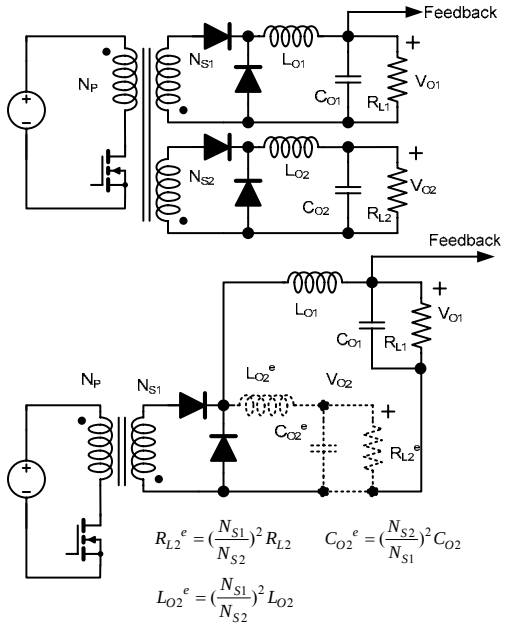


Fig. 24. Multiple output forward converter.

VI. MEASUREMENT OF TRANSFER FUNCTION AND LOOP GAIN

The control-to-output transfer function or the loop gain of the power stage can be measured using a network or frequency response analyzer. The network analyzer provides a sinusoidal output voltage of controlled amplitude and frequency. This signal can be injected into the system to be measured at any location. The analyzer also has two inputs: A and B. The network analyzer performs the function of a narrowband tracking voltmeter. It measures the components of A and B at the injection frequency and displays the magnitude and phase of B/A. The network analyzer can automatically sweep the frequency of the injection signal to generate the magnitude and phase bode plots of the transfer function B/A.

The signal injection point should be on the signal path, with a low source impedance, and high load impedance to minimize the impedance loading of the network analyzer. There can be two signal injection points (P-1 and P-2) in the path of the feedback loop, as shown in Fig. 25. Point P-1 is in series with the output and most widely used for single output applications. However, it becomes invalid with the inclusion of a multiple-feedback-loop system with multiple outputs. Meanwhile, point P-2 is between the voltage error amplifier and the pulse width modulator (PWM) comparator. This point is very useful for the multiple output feedback circuit since all the feedback signals are summed and passed through this point. It is also useful for high voltage output application since the network analyzer input voltage (A and B) is usually limited to below 20V. However, that point is usually internal to most PWM integrated circuits and therefore is not accessible. When point P-2 is not accessible, an alternative circuit configuration, such as the one shown in Fig. 26 can be used instead, which is equivalent to the configuration for point P-2 of Fig. 25. Fig. 27 shows another alternative configuration where the g_M amplifier is used for the error amplifier.

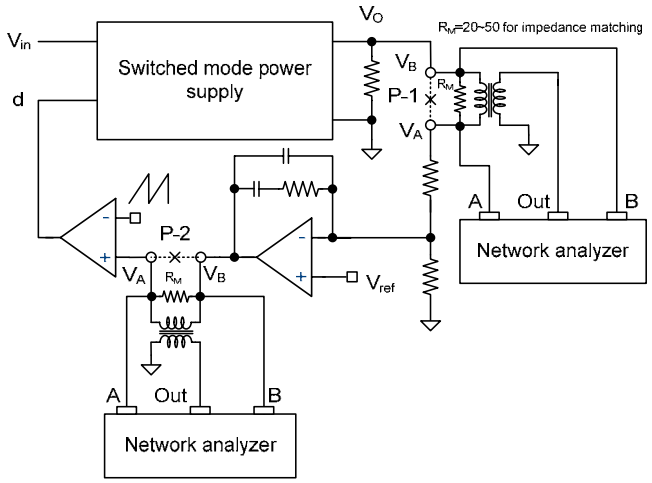


Fig. 25. Loop gain measurement.

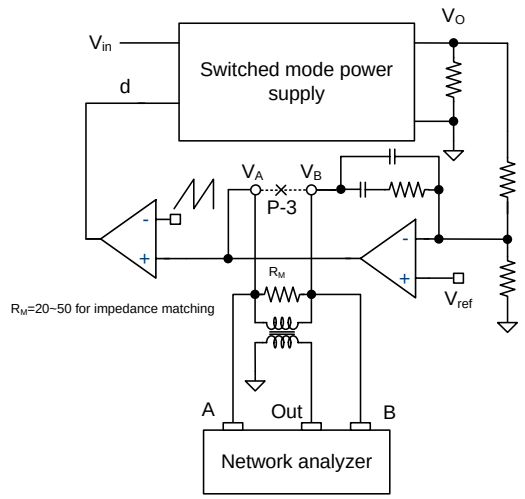


Fig. 26. Alternative measurement configuration for injecting signal at the output of error amplifier.

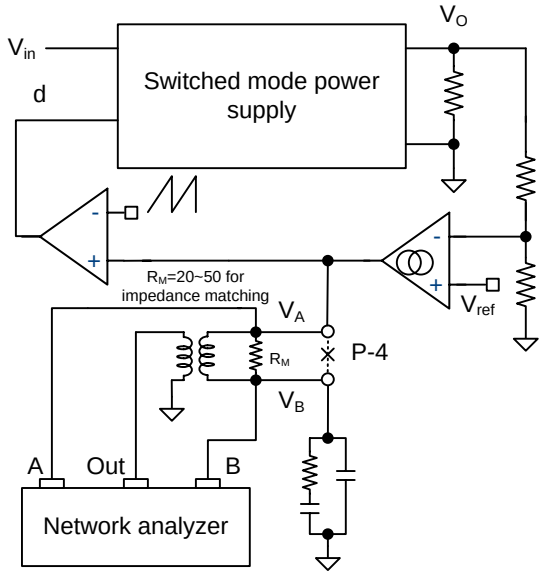


Fig. 27. Alternative measurement configuration for injecting signal at the output of error amplifier (g_M amplifier).

VII. CONCLUSION

The fundamental purpose of small-signal modeling of a power supply has been discussed. The small-signal transfer functions for basic converters and general compensation networks have been examined. The practical feedback loop design issues, such as consideration of opto-coupler characteristics, using shunt-regulator KA431, control loop design for multiple output application, and loop gain measurement have been considered and presented.

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Hangseok Choi received B.S., M.S., and Ph.D degrees in electrical engineering from Seoul National University in 1996, 1999, and 2002, respectively. From 2002 to 2007, he was employed as a system and application engineer of power conversion group at Fairchild Semiconductor Korea, where he was involved in development and technical support of Green Fairchild Power Switch (FPS™) families and power management ICs. He is currently working for Fairchild Semiconductor in Bedford, NH, USA, as a principal system and application engineer, where he is developing high-performance power management ICs. He has published more than 15 application notes for Fairchild Semiconductor and more than 15 technical papers for IEEE conferences and transactions. He has conducted Fairchild power seminars since 2007. His research interests include soft-switching techniques, modeling, and control of converters.