

Designing Auxiliary Power Supplies for High Efficiency and Low Standby Power

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Abstract — Auxiliary power supplies are required to have low standby power consumption at light-load conditions. These power supplies also require features such as low cost, high efficiency, and a Line Under-Voltage Lockout (UVLO) function to detect the input voltage so the main power supply does not operate at low input voltage ranges. Fairchild's FSQ510 has been specifically designed for low standby power consumption and valley switching control and is ideal for auxiliary power supplies. This paper outlines a design procedure for an auxiliary power supply using the FSQ510.

I. INTRODUCTION

The flyback topology is a popular choice for low power applications, such as auxiliary power supplies for personal computers and white goods. Due to its simplicity, the flyback can be implemented using one switching component and one transformer. Although converter topologies with one switching component have a lower total cost, switching losses are unavoidable in hard-switching mode. To improve active-mode efficiency, it is necessary to develop soft-switching techniques that can be used in low power applications or for a single-switching component.

In flyback topologies with a single switching component, quasi-resonant techniques are used to increase total efficiency by reducing switching losses. An example of a quasi-resonant technique is valley switching. When flyback topologies operate in discontinuous conduction mode (DCM), the drain-to-source voltage of the MOSFET resonates after the current of the secondary rectifying diode reaches zero. Using valley switching, the switching component turns on at the instant of the first minimum value of the drain-to-source voltage of the MOSFET. Valley switching exhibits good EMI (Electromagnetic Interference) and thermal performance, however, it has a significant problem in that the switching losses increase at light-load conditions due to the increased switching frequency

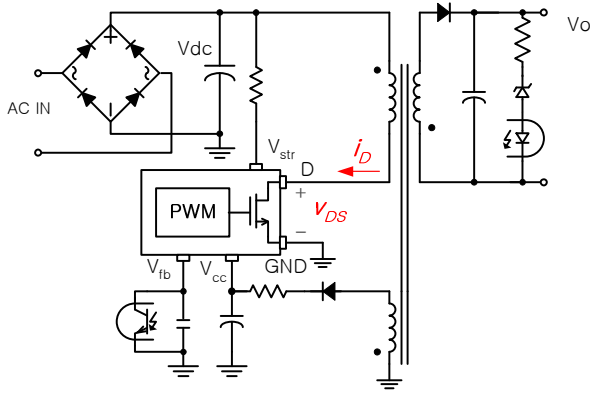
of always finding the first valley. This paper introduces some modifications to an existing valley switching method to improve this behavior.

Section II introduces the basic concept and advantages of window-valley-switching control, which allows for narrow switching frequency ranges even at light-load conditions. Fairchild's Green FPSTM *e-Series*TM, which utilizes window-valley-switching control, is also introduced in Section II. Section III presents a design procedure for auxiliary power supplies using the FSQ510, along with an external Line-UVLO circuit and a simple linear regulator which supplies voltages for other controllers. Experimental results proving the validity of the proposed design procedure are discussed in Section IV.

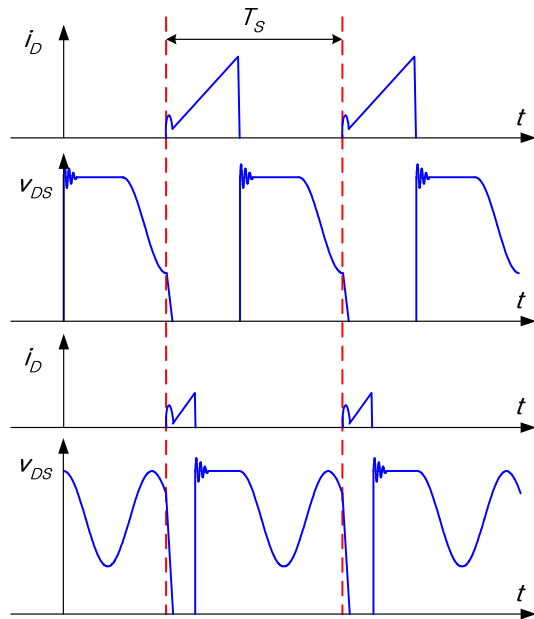
II. BACKGROUND

Figure 1 shows a conventional flyback-converter schematic diagram and its key waveforms. When the flyback operates in DCM with a fixed frequency, the drain-to-source voltage of the MOSFET at the instant of switch turn-on is arbitrary. As a result, the capacitive loss of the MOSFET during switch turn-on cannot be predicted or minimized. Because the capacitive loss is a large portion of the total losses in low power applications, it must be reduced in order to achieve higher efficiencies.

To reduce the capacitive loss, valley switching is introduced, which causes the switching to occur when the drain-to-source voltage of the MOSFET reaches its first minimum value, shown in Figure 2. This conventional valley switching method always finds the first (or second) valley of the drain-to-source voltage of the MOSFET for the next switching cycle^[1], but it has the drawback of wide operating frequency ranges depending on the input voltage and load current. Therefore the efficiency



(a) A conventional schematic of flyback



(b) Drain current and drain voltage

Fig. 1. A conventional flyback and its key waveforms.

decreases at light load since the high operating frequency increases the capacitive losses as shown in the last curve of Figure 2.

Window-valley switching adopts a blanking and window time which limits the operating frequency. Using the operating waveforms and frequencies in Figure 3, one can find a minimum value of the drain-to-source voltage and its frequencies controlled by the blanking time t_B and the window time t_W . Once the MOSFET turns on, the valleys are ignored during t_B ; that is, the next turn-on is prohibited during t_B . After t_B , the valley is detected only within duration of t_W . If no valley is detected during t_W , the MOSFET is forced to turn on when t_W

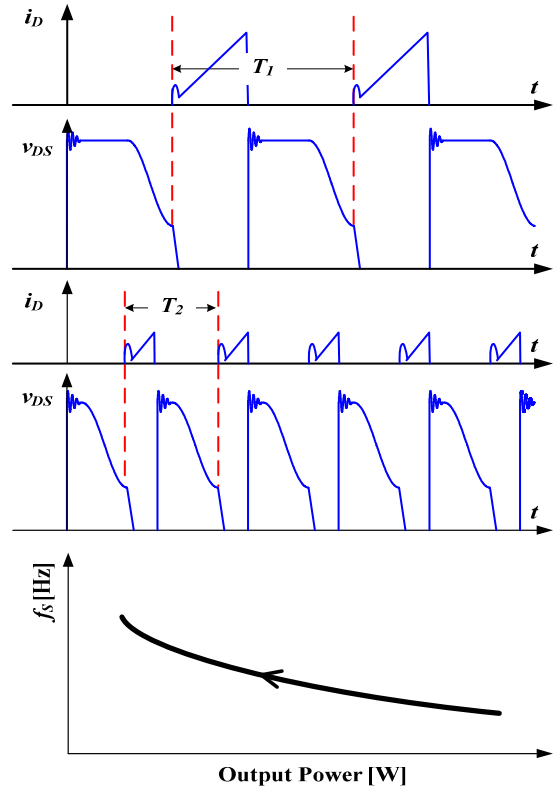


Fig. 2. Operating waveforms and frequencies of a conventional valley switching converter depending on the load variations.

ends, as shown in Figure 3(d). It enters continuous conduction mode (CCM) operation with constant operating frequency even if a lower input voltage is applied or output current is increased.

Consequently, the operating frequency of the window-valley-switching method is within a narrow range defined by t_B and t_W , compared to the conventional approach. Switching losses are not increased at light load conditions.

Figure 4 shows an external circuit to indirectly detect the valleys via the bias winding voltage (a) and its key waveforms (b~d). The bias winding voltage reflects the drain-to-source voltage without a DC offset, which corresponds to the input capacitor voltage, as shown in Figure 4(b). The shape of the drain-to-source voltage of several hundred volts is observed on the “Sync” pin with scaling down using the turns ratio N_a/N_p and the voltage divider R_a , R_b , and R_c , where N_a and N_p are the turns numbers of the bias and primary windings, respectively.

Since the control IC typically cannot withstand a negative voltage exceeding $-0.3V$ as an input, a diode, D_a , is needed to remove the negative parts from Figure 4(b). Therefore, a diode, D_a , is added and the voltage divider is composed of three vs. two resistors. The most important information, i.e. where the valleys are, disappears. Now capacitor C_a has a role. The observed voltage on the “Sync” pin is delayed by a time constant made by C_a and the voltage divider, as shown in Figure 4(d). Considering an internal delay time, t_{Sync} , of around 200ns as specified in the FSQ510 datasheet, adjust the instant where v_{Sync} reaches the low threshold voltage V_{SL} to the valley of the drain-to-source voltage of the MOSFET.

High efficiency and low EMI can be achieved using the window-valley-switching technique. This is due to the low drain-to-source voltage at the turn-on. A second reason is illustrated in Figure 5. In AC-DC converters, there should be a rectifying circuit in the input side, composed of rectifying diodes and a link capacitor. Therefore, there should be a voltage ripple of 120Hz (or 100Hz) on the link voltage that is twice that of line frequency, 60Hz (or 50Hz.) At the peak of the ripple, the drain current shows the steepest slope with a given input voltage so that the valley in t_W is detected early; that is, the converter operates at the highest operating frequency under given conditions. The slope of the drain current decreases as the input voltage decreases to the lowest point of the ripple, which causes the valley in t_W to move to the right, assuming that the feedback signal does not change. The operating frequency decreases until the AC source starts to charge the link capacitor. This operation repeats as long as there is ripple on the link voltage. The operating frequency shows a fluctuation periodically, according to the ripple, which is called an “Inherent Frequency Modulation Function”. It is helpful to reduce EMI with smaller filters.

Fairchild’s Green FPSTM *e-Series*TM adopts the above mentioned window-valley-switching technique to increase total efficiency. The FSQ510 is specially designed for low quiescent operating current of not more than 1 mA and advanced burst

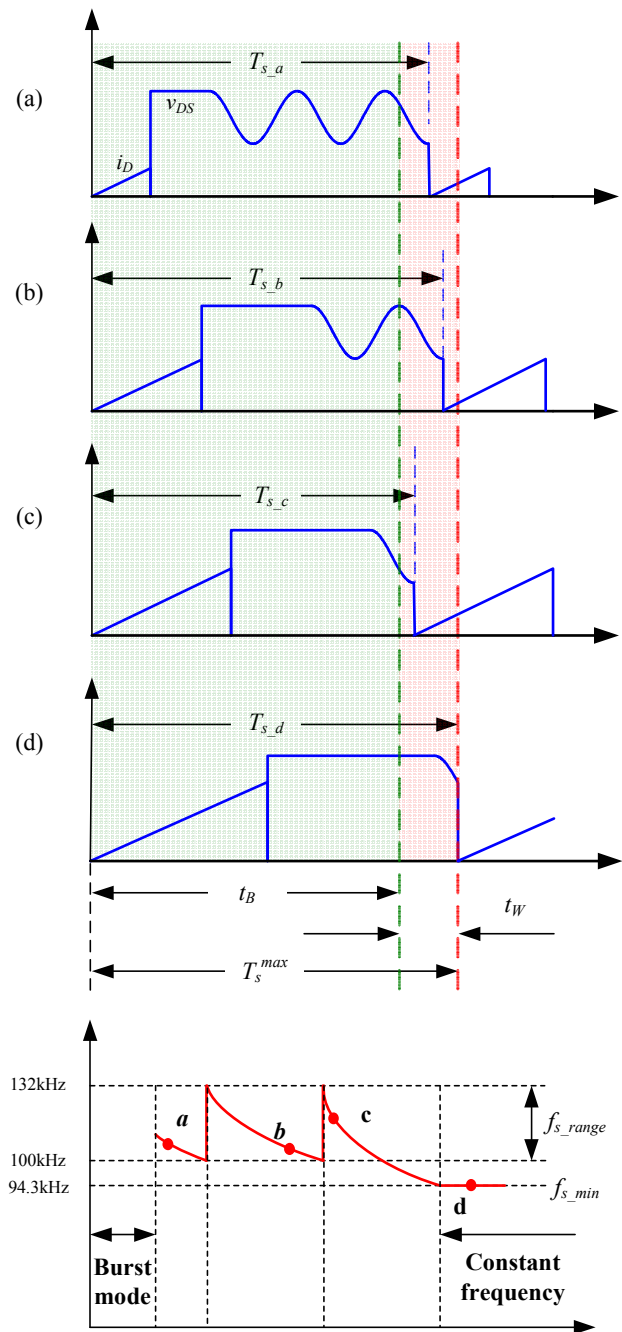
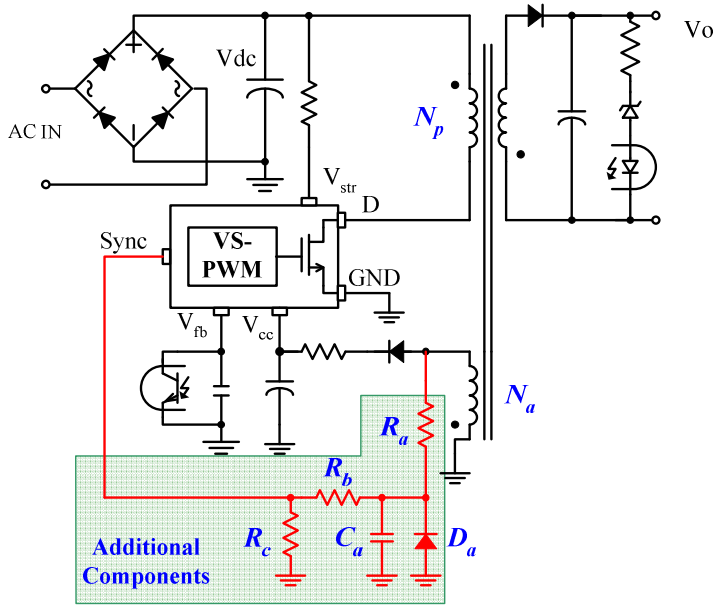


Fig. 3. Operating waveforms and frequencies of the window-valley-switching technique depending on the load conditions

mode operation. The FSQ510 achieves strict standby power consumption required by international guidelines such as Energy Star and California Energy Commission (CEC)^[2].

In the next section, a design procedure is provided for an auxiliary power supply using the FSQ510.



(a) An external circuit schematic to detect valleys

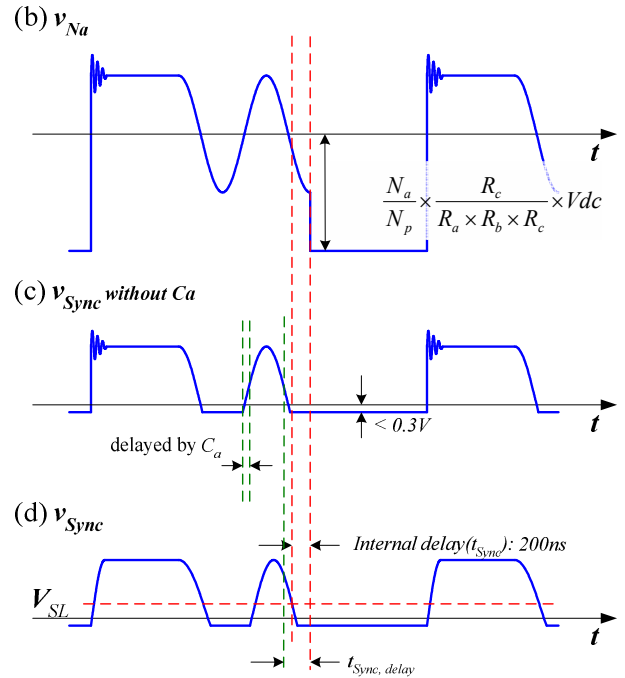


Fig. 4. External circuit for detecting valleys and key waveforms.

III. DESIGN PROCEDURES

TABLE I

ELECTRICAL SPECIFICATIONS FOR AN AUXILIARY POWER SUPPLY

Device	FSQ510
Input Voltage Range	85 ~ 265 V _{AC}
Rated Output Power	4.24 W
Rated Output Voltage / Output Current	5.1 V / 0.8 A 16 V / 10 mA
Application	Auxiliary Power Supply Unit with additional V _{CC2}

Fairchild application notes AN-4137 and AN-4150 provide a detailed design procedure for conventional flyback converters, including the design of the transformer and feedback loop, as well as the selection of an input capacitor and output filter^[3-4]. This section covers three topics with design examples: a simple design procedure of a transformer suitable for window-valley-switching flyback converters, a line-UVLO circuit, and a simple linear regulator circuit for other control ICs. The example electrical specifications are shown in Table I.

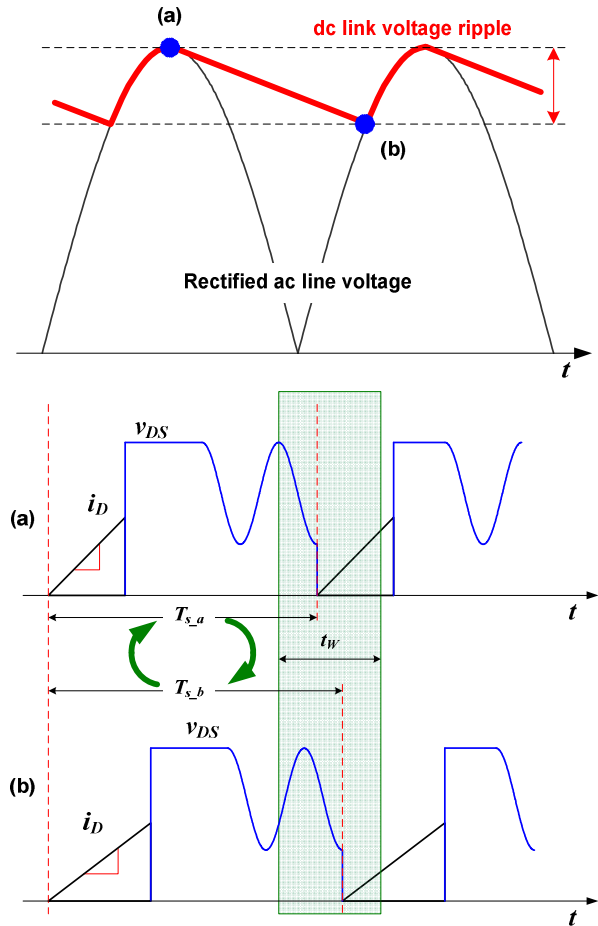


Fig. 5. Operating waveforms and frequencies depending on the input capacitor voltage ripples.

A. Transformer Design

Conventional valley-switching flyback converters should always be designed to operate in DCM since the main switch turns on at the first local minimum value of the drain-to-source voltage of the MOSFET. Window-valley-switching flyback converters can be designed to operate in either DCM or CCM depending on the input voltage and output load conditions, as illustrated in Figure 3. Compared to CCM operation, the magnetizing inductance (L_m) and transformer size for DCM operation are smaller, while conduction losses of the MOSFET increases due to the increased rms current of the primary side.

In practice, when designing for a rated output power less than 2~3W, it is preferable that the flyback converter only operate in DCM under an overall range of input voltage and load current. On the other hand, it is more advantageous to have the flyback converter operate in both modes for more than 3W from a total efficiency point of view.

The transformer design procedure follows.

Step 1. Turns Ratio

Schottky diodes are generally used for the secondary rectifying diode to reduce conduction losses from the forward voltage drop. The reverse voltage rating of the Schottky diode is, however, not more than 100V. It requires the turns ratio of the transformer to be limited. First, the turns ratio of the transformer needs to be determined. Second, the duty ratio must be below 0.5 to avoid a sub-harmonic oscillation of the drain current, since the FSQ510 uses a current-mode control method. Assuming the flyback converter operates in CCM at a minimum input voltage, the two limitations mentioned above would give the two boundaries of the transformer turns ratio as:

$$\frac{V_{in,max}}{\frac{V_{RRM}}{1+margin} - V_o} < n < \frac{V_{in,min}}{V_o} \times \frac{D_{max}}{1-D_{max}} \quad (1)$$

where D_{max} is a desirable maximum duty ratio; $V_{in,max}$ and $V_{in,min}$ are the maximum and minimum input voltages; V_{RRM} and $margin$ are the diode reverse voltage rating plus an appropriate margin and V_o is the rated output voltage.

Design Example

The proper D_{max} is generally 0.45~0.5^[3~4]. The minimum input voltage $V_{in,min}$ should be determined considering the ripple voltage on the input capacitor. The margin of the diode reverse voltage rating is generally 25%. The lower and upper boundaries for the turns ratio are calculated as:

$$\frac{V_{in,max}}{\frac{V_{RRM}}{1+margin} - V_o} = \frac{375V_{dc}}{\frac{40V_{dc}}{1+0.25} - 5V_{dc}} = 13.88 \quad (2)$$

$$\frac{V_{in,min}}{V_o} \times \frac{D_{max}}{1-D_{max}} = \frac{90V_{dc}}{5V_{dc}} \times \frac{0.45}{1-0.45} = 14.73 \quad (3)$$

Therefore, the turns ratio is selected as 14. In other words, when the turns ratio is 14, the Schottky diode with 40V of the reverse-voltage rating could be used with 25% of the margin.

After determining the turns ratio, the voltage stress on the MOSFET in the primary side needs to be checked. Notice that an excessive turns ratio increases reflected output voltage and voltage stress on the MOSFET. The maximum drain-to-source voltage of the MOSFET can be calculated as:

$$V_{DS,max} = V_{in,max} + n \times V_o + V_{lkg} \quad (4)$$

The appropriate $V_{DS,max}$ is generally selected as 70~80% of the maximum voltage rating of the MOSFET built-in the FSQ510.

Step 2. Magnetizing Inductance

The average power P_{in} and Δi in both operations of DCM and CCM can be calculated as:

$$P_{in} = V_{in} \times D \times (I_{pk} - \frac{\Delta i}{2}) [W] \quad (5)$$

$$\Delta i = \frac{V_{in} D}{L_m f_s} [A] \quad (6)$$

where V_{in} , D , and f_s are the input voltage, duty ratio, and operating frequency, respectively, and I_{pk} and Δi are the drain peak current and the increment of the drain current while the switch turns on, as illustrated in Figure 6.

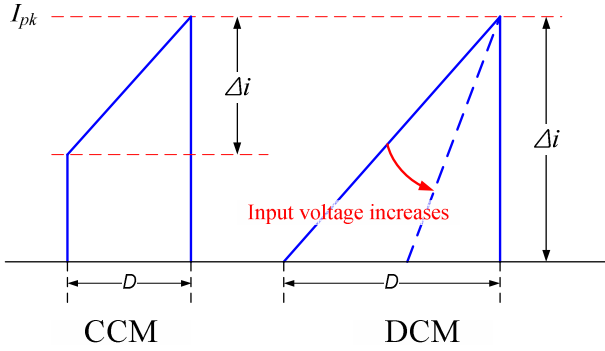


Fig. 6. Drain currents of the MOSFET in CCM (left) and DCM (right)

An appropriate magnetizing inductance can be obtained using Equations 5 and 6 as:

$$L_m = \frac{(V_{in,min} \times D_{max})^2}{P_{in} \times f_{s,min}} \times \left(\frac{I_{pk}}{\Delta i} - 0.5 \right) [H] \quad (7)$$

where $V_{in,min}$ and $f_{s,min}$ are the minimum input voltage and minimum operating frequency, respectively.

In Equation 7, the ratio of I_{pk} and Δi equals unity for DCM and larger than unity for CCM operation. To guarantee both DCM and CCM operation with the window-valley-switching technique, the typical value of this ratio should be around 1.1 ~ 1.4. It is noticeable that a ratio exceeding 1.4 causes efficiency to decrease. To obtain a large L_m , the layer of the transformer primary winding should be increased. This results in the increase in capacitive losses at high input voltages even though the conduction loss decreases as the rms current of the primary side decreases with the large L_m .

Design Example

The ratio of I_{pk} and Δi is selected as 1.2 and the recommended I_{pk} value is about 80~90% of $I_{LIM,min}$, the minimum value of the pulse-by-pulse current limit specified in the FSQ510 datasheet. $f_{s,min}$ is 94.3kHz ($= 1/(t_B+t_W)$). Assuming the desired total efficiency is 80%, input power P_{in} is around 5.3 W. As a result:

$$L_m = \frac{(90V_{dc} \times 0.45)^2}{5.3W \times 94.3kHz} \times \left(\frac{0.24A}{0.2A} - 0.5 \right) = 2.30mH \quad (8)$$

The required input power must be sufficiently guaranteed with the calculated L_m using equation:

$$\begin{aligned} P_{in} &< \frac{1}{2} L_m (I_{pk}^2 - (I_{pk} - \Delta i)^2) f_{s,min} \\ &= \frac{1}{2} \times 2.3mH \times (0.24A^2 - 0.04A^2) \times 94.3kHz \\ &= 6.1W \end{aligned} \quad (9)$$

The proper L_m can be chosen as 2.3 mH.

Step 3. Minimum Primary Turns Number

The minimum primary turns number to avoid the transformer core saturation can be calculated as:

$$N_{pri,min} = \frac{1.2 \times I_{LIM,max} \times L_m}{B_{max} \times A_e \times 10^6} [turns] \quad (10)$$

where the coefficient 1.2 should be added with consideration of a margin of $I_{LIM,max}$, the maximum value of the pulse-by-pulse current limit of the FSQ510. A_e is the effective cross-sectional area of the used core and B_{max} is a maximum flux density, which should be chosen as 0.25~0.3 [Tesla], considering temperature features.

Design Example

The EPC25 is selected, whose effective cross-sectional area is 46.4mm² according to the datasheet provided by the manufacturer.

$$N_{pri,min} = \frac{1.2 \times 0.36A \times 2.3mH}{0.27T \times 46.4mm^2 \times 10^6} = 79.3 turns \quad (11)$$

The primary turns number is 84, assuming the secondary turns number can be an integer. The secondary winding can be calculated as:

$$N_s = \frac{N_p}{n} = \frac{84turns}{14} = 6 [turns] \quad (12)$$

To conclude, the schematic and electrical characteristics of the transformer are summarized in Figure 7 and Table II. To enhance the coupling between the primary and secondary winding, the sandwich winding method is used: the secondary and bias windings are enclosed by the half of the primary winding.

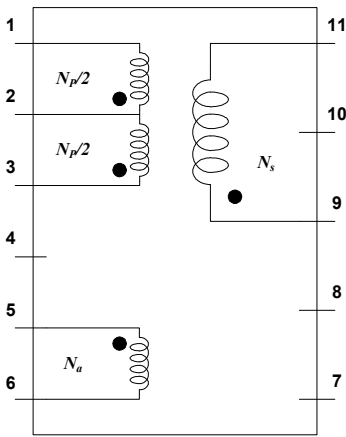


Fig. 7. Transformer schematic.

TABLE II
 ELECTRICAL SPECIFICATIONS FOR THE DESIGNED TRANSFORMER

Winding Specification			
Winding	Wire	Turns	Winding Method
$N_p/2$	$0.16\phi \times 1$	42	Solenoid Winding
N_a	$0.16\phi \times 1$	18	Solenoid Winding
N_s	$0.6\phi \times 1$	6	Center Solenoid Winding
$N_p/2$	$0.16\phi \times 1$	42	Solenoid Winding

Electrical Characteristic		
	Specification	Remark
Magnetizing Inductance	$2.3 \text{ mH} \pm 5\%$	100 kHz, 1 V
Leakage Inductance	$< 30 \mu\text{H max.}$	Short all other pins (100 kHz, 1 V)

B. Line-UVLO Circuit Design

Figure 8 shows a line-UVLO circuit that consists of Zener diodes, P- and N-type transistors, and other passive components.

The FSQ510 starts when the applied voltage on the “ V_{str} ” pin exceeds the minimum value to enable the internal startup circuit. When an appropriate Zener diode is used, the FSQ510 does not operate under the line input voltage, as shown below:

$$V_{Line,start} = V_{Z1} + V_{STR,min} [V_{dc}] \quad (13)$$

where V_{Z1} is the Zener voltage of ZD_1 and $V_{STR,min}$ is the minimum value to operate the internal startup circuit, which is typically $27V_{dc}$, as described in the datasheet of the FSQ510.

The FSQ510 can be disabled by Q_1 , Q_2 , and ZD_2 . When the voltage of Node A becomes lower than Node B by V_{BE} of Q_1 as the input voltage decreases, Q_1 turns on. The base current of Q_2 is supplied from V_{CC} , which results in the turn-on of Q_2 . The feedback voltage of the FSQ510 is pulled down to zero by Q_2 . The line input voltage for disabling the device, $V_{Line,stop}$, can be obtained as:

$$V_{Line,stop} = (V_{Z2} - V_{BE}) \cdot \left(\frac{R_1}{R_2} + 1 \right) \quad (14)$$

where V_{Z2} is the Zener voltage of ZD_2 , V_{BE} is the threshold voltage between the base and emitter of Q_1 (typically 0.7V), and R_1 and R_2 are illustrated in Figure 8.

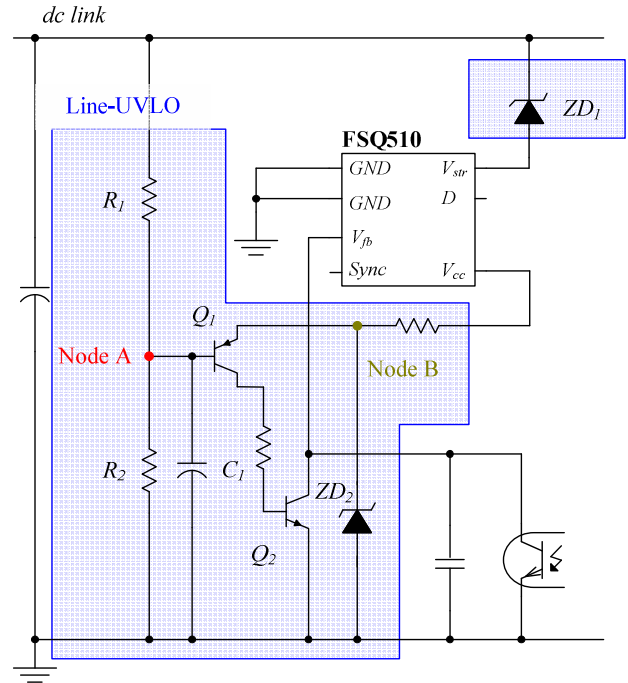


Fig. 8. A Line-Under-Voltage Lockout circuit for FSQ510.

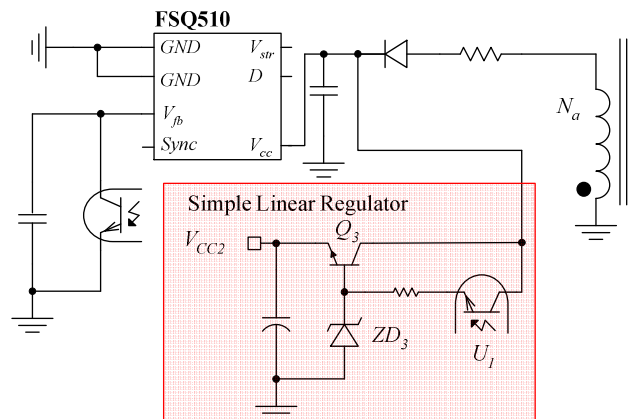


Fig. 9. Simple linear regulator circuit.

Design Example

Assuming that 1N4764 ($V_z=100V$) is used for ZD_1 ; R_1 , R_2 , and ZD_2 are $6M\Omega$, $390k\Omega$, and 1N5234 ($V_z=6.2V$), respectively:

$$V_{Line,start} = 100 + 27 = 127 [V_{dc}] \quad (15)$$

$$V_{Line,stop} = (6.2V - 0.7V) \cdot \left(\frac{6M\Omega}{390k\Omega} + 1 \right) = 90 [V_{dc}] \quad (16)$$

C. Simple Linear Regulator for Additional V_{CC2}

The additional V_{CC2} is needed for other controllers on the primary side, such as a Power Factor Correction (PFC) circuit controller. It can be supplied from either an additional winding coupled with the windings of the transformer or the V_{CC} of the FSQ510, as shown in Figure 9. The additional V_{CC2} can be enabled and disabled by an optocoupler controlled externally. The V_{CC2} is regulated by the n-type transistor Q_3 and the Zener diode ZD_3 . The V_{CC2} is obtained as:

$$V_{CC2} = V_{ZD3} - V_{BE} \quad (17)$$

D. External Circuit for Valley Detection

The window-valley-switching technique requires external components to detect valleys of the drain-to-source voltage, as shown in Figure 10. Normally, Schottky diodes or ultra-fast recovery diodes are used for the clamp diode D_1 . The roles of three resistors and the diode are not only to attenuate the voltage across the winding N_a to less than the maximum voltage rating of the “Sync” pin, but also to clamp the negative part to within $-0.3V$. Capacitor C_2 gives a delay time to align turn-on with the exact position of each valley. The delay time can be obtained as:

$$t_{Sync,delay} = \frac{R_3 \times (R_4 + R_5)}{R_3 + R_4 + R_5} \times C_2 + 200ns [sec] \quad (18)$$

where $t_{Sync,delay}$ is the delay time, shown in Figure 3. Sometimes the internal delay time of 200ns specified in the datasheet is enough to synchronize the instant when v_{Sync} reaches V_{SL} with the valleys of the drain-to-source voltage.

Design Example

Notice that the absolute maximum rating of the “Sync” pin is 6.5V and there are two threshold voltages, such as 0.7V and 0.1V, typically specified in the datasheet. To detect the valleys, the voltage on the “Sync” pin should exceed 0.7V and then be lower than 0.1V. The three resistors can be obtained considering the voltage across the winding N_a and

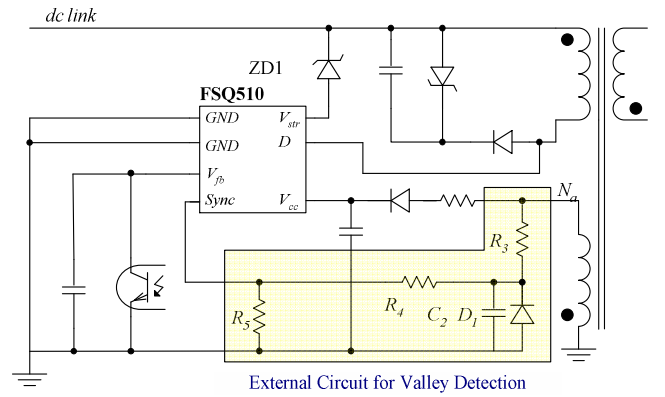


Fig. 10. External circuit for valley detection.

the absolute maximum rating of the “Sync” pin 6.5 V. The results are:

$$R_3 = 27k\Omega \text{ and } R_4 = R_5 = 6.2k\Omega \quad (19)$$

No additional delay time is required.

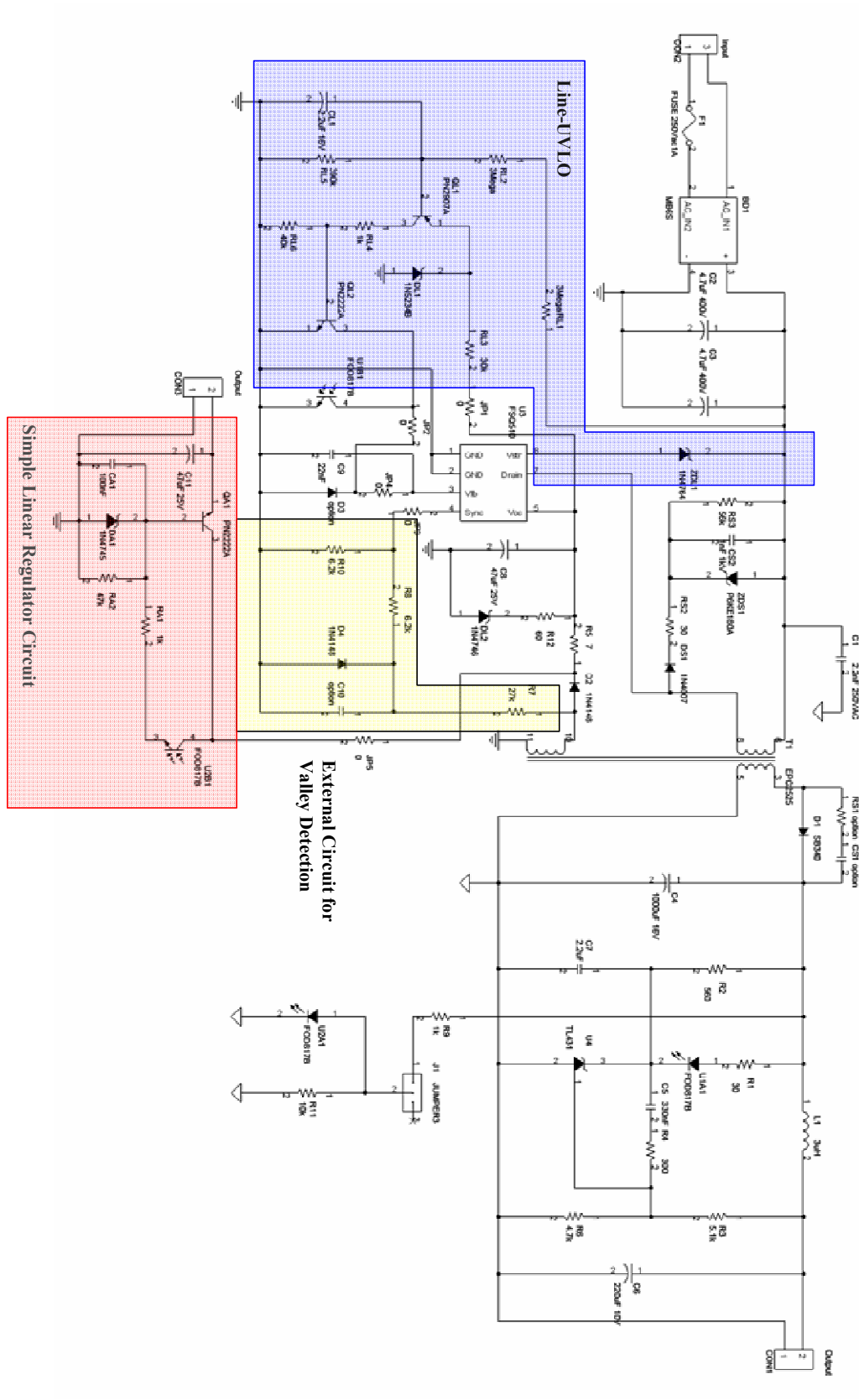


Fig. 11. Total schematic of the demo board using FSQ510.

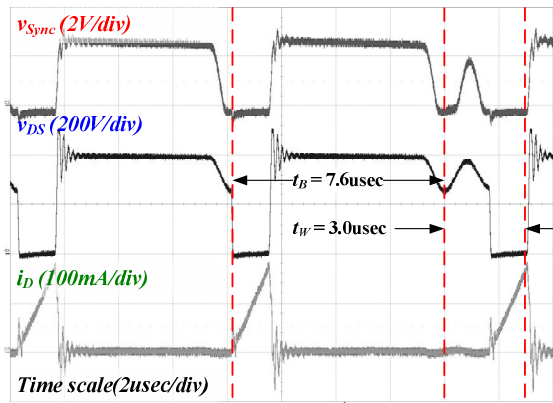


Fig. 12. Key waveforms at 230 V_{AC} and full-load condition.

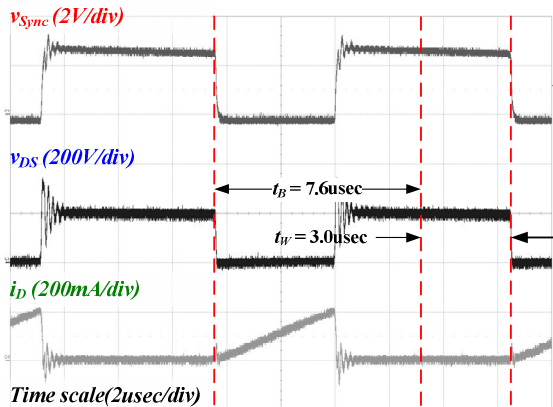


Fig. 13. Key waveforms at 85 V_{AC} and full-load condition.

IV. EXPERIMENT RESULTS

To verify the validity of the proposed design procedure, a demo board of 4.24W using the FSQ510 was designed. Its total schematic and components' values are shown in Figure 11.

Figures. 12 and 13 show the key waveforms of the demo board. At 230V_{AC} input voltage and full-load condition, the MOSFET of the FSQ510 turns on at the valleys, shown in Figure 11. In Figure 12, the CCM operation is shown at 85 V_{AC} input voltage and full-load condition because no valley is found during t_W .

Figure 14 shows the variation of the switching frequencies as the load current increases. The operating frequency does not change significantly even at the light-load condition.

Figure 15 shows the drain current and the drain-to-source voltage of the MOSFET captured by persistence view function of the oscilloscope and the histogram of the switching frequency variation

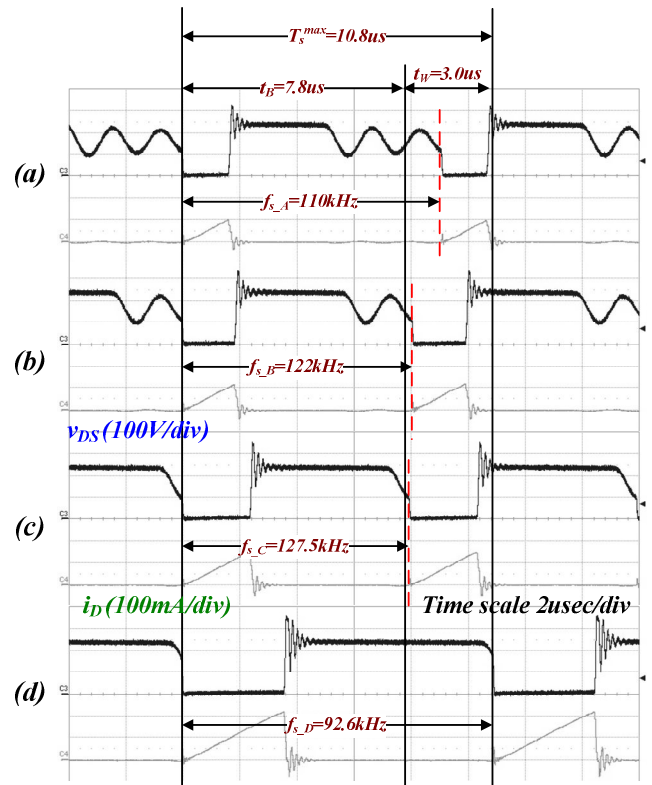


Fig. 14. Drain current and voltage waveforms and operating frequencies depending on the load increase from (a) to (d).

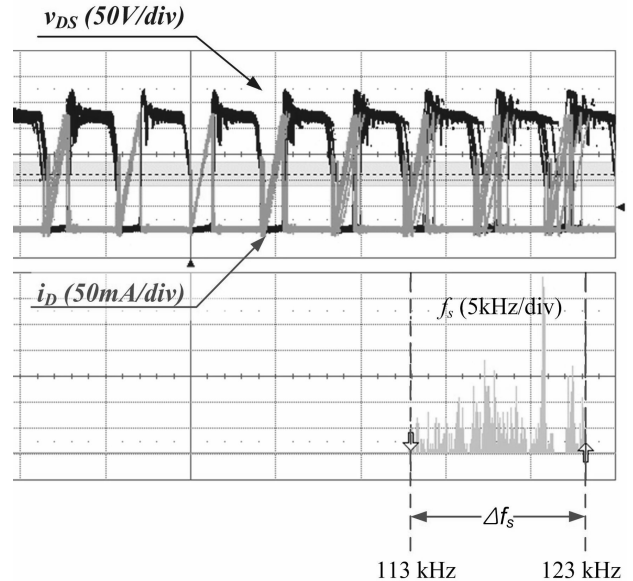


Fig. 15. Operating waveforms (top) and histogram of the switching frequency variation (bottom) depending on the input capacitor voltage ripple.

depending on the input voltage ripple at 115V_{AC} input voltage and full-load condition. The switching frequency varies between 113kHz and 123kHz. It improves EMI.

Figure 16 shows the standby power consumption versus input voltage at no-load condition. Less than 40mW and 70mW is achieved when the sensing resistors for line-UVLO function are removed and added, respectively. Figure 17 shows the input power increases as the load current increases at 230V_{AC}.

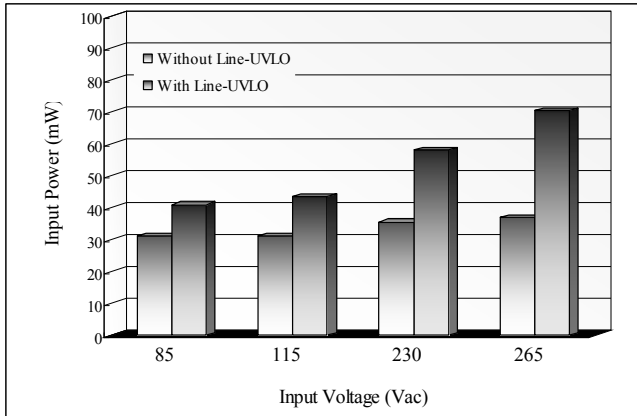


Fig. 16. Standby power consumption depending on the input voltage at no-load condition: without line-UVLO function (red bar) and with line-UVLO function (blue bar).

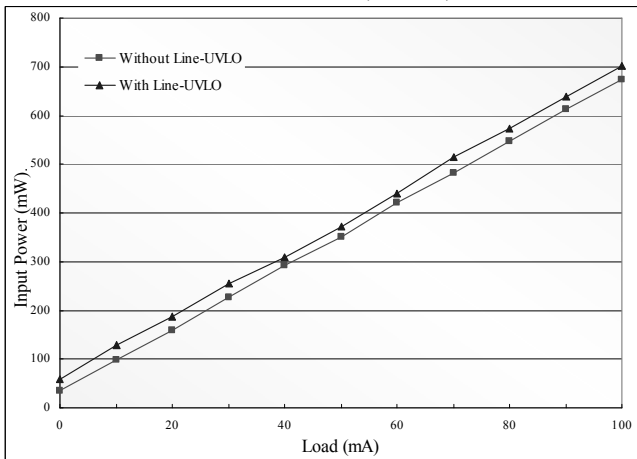


Fig. 17. Input power depending on the load current at 230 V_{AC} input voltage condition: without line-UVLO function (red line) and with line-UVLO function (blue line).

Figure 18 shows the measured efficiency for both cases: with and without line-UVLO function. With the sensing resistors for line-UVLO, the efficiency at full load condition is more than 82.4% and the maximum efficiency is more than 83.2% at 115V_{AC}. The efficiency at 230V_{AC} and full-load condition is more than 82% including the sensing resistors for line-UVLO.

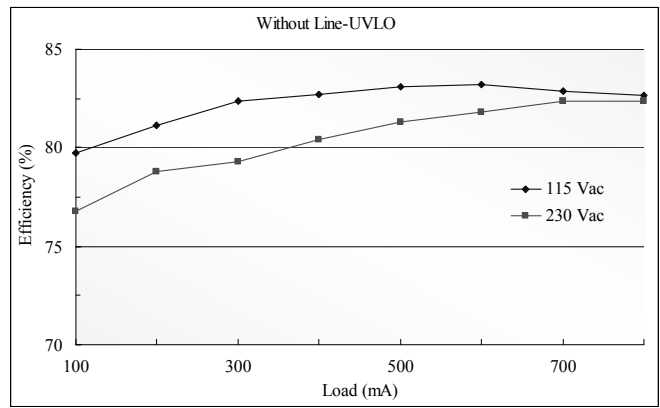


Fig. 18. Measured efficiencies of the demo board

Figure 19 shows the temperature of each component on the demo board when the input voltage is 230V_{AC} and the load current is 800mA. The temperature of the FSQ510 and the secondary rectifying diode are 41.6°C and 49.7°C, respectively.

Figure 20 shows the performance of the line-UVLO function. The FSQ510 starts when the input capacitor voltage reaches around 122V_{DC} and stops operation when the input capacitor voltage reaches 90V_{DC}. The components' tolerance for line-UVLO

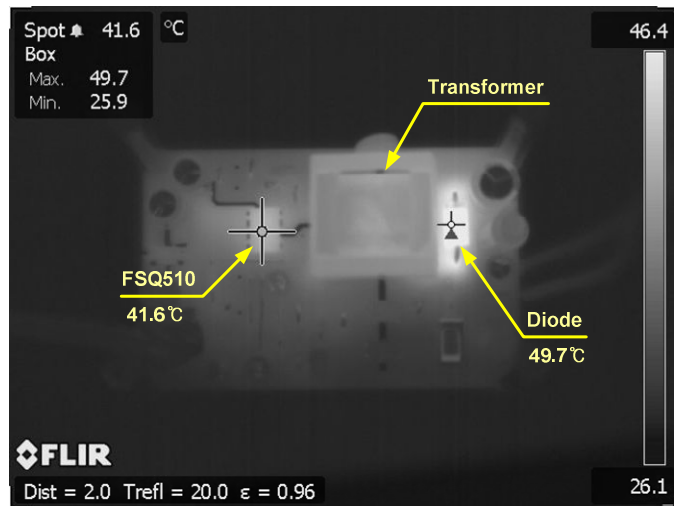


Fig. 19. Measured temperatures of each component of the demo board.

may make a difference between the measured value and the value of $V_{Line,start}$ shown in the design procedure.

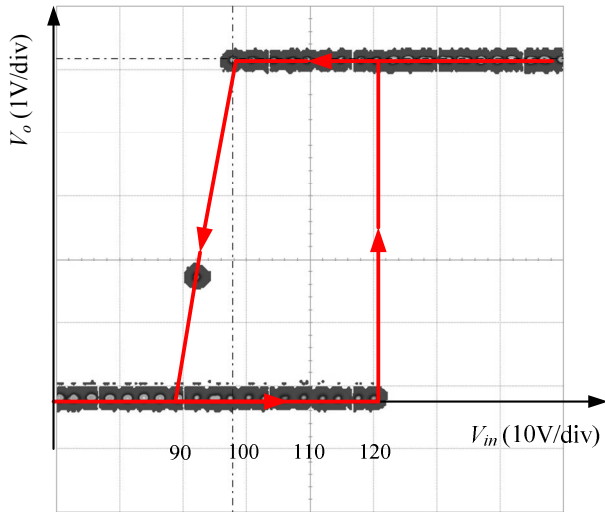


Fig. 20. Line-UVLO performance: input voltage V_{in} versus output voltage V_o .

V. CONCLUSION

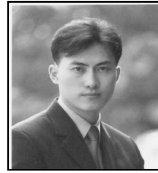
A design procedure for auxiliary power supplies using the FSQ510 was explained in this paper. An external line-UVLO circuit and simple linear regulator circuit for additional V_{CC2} were also described. To verify the validity of the proposed design procedure, a demo board of 4.24W using the FSQ510 was designed and constructed. Its standby power, efficiency, thermal performance, and the performance of line-UVLO function were examined and measured. Less than 70mW of the standby power and more than 82% of the maximum efficiency were achieved, which meets international regulations, such as CEC and Energy Star[®]. The temperature of the FSQ510 was not more than 42 °C at full-load condition. It is expected that the proposed design procedure can help design auxiliary power supplies using the FSQ510, including the line-UVLO and the linear regulator circuit.

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