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Parallel Operation Of Semiconductor Switches

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In uninterruptable power supplies demands for current handling capability to meet load current In uninterruptable power supplies demands for current handling capability to meet load current requirements plus margins for overload and reliability purposes often exceed the capability of the largest semiconductor device type considered and paralleling may become an attractive alternative. All switching power semiconductors starting with SCR's [1], bipolar transistors [2-4] darlingtons [5] and field effect transistors [6-10], have been successfully paralleled, but proper precaution had to be taken. We will review some of these methods, describe the characteristics of the insulated gate transistors, and show the proper methods to operate this relatively new family of devices in parallel.

All semiconductor circuits using parallel connected devices to switch a higher load current can easily be analyzed by using Kirchoff's law. As long as all voltage drops in the parallel branches are equal, the currents through the branches are equal.

This sounds sensible and logical, but as soon as we consider the different stages every switching device has to assume and we consider the parameters of each switching device which guarantees equal voltage drops in the branches over the required temperature range and over the duration of the switching cycle, complications begin to appear.

At first glance, each switching device has only two functional states, an "off- state" and an "on-state". But by closer examination, we have to consider how we get from "off" to "on" and back to "off", the "dynamic" area of the switching waveform (Figure 1). The dynamic area is only a fraction of the total waveform, but it is by far the most important when it comes to parallel operation.

In power electronics, there are three different load types; resistive, capacitive, and inductive. The resulting waveforms are sufficiently different to require either different switching devices or the circuit designer may have to change the switching circuit to meet the different requirements, especially when devices are operated in parallel.

Off-State

The off-state is probably the least demanding state in parallel operation of semiconductor devices. As long as leakage current is low, even differences of more than 100% would not create any difficulties.

On-State

The on-state is again a relatively uncritical and uneventful period (Figure 2). Most devices in switching applications are overdriven and differences in gain or transconductance do not translate into proportional output current.

Even if a bipolar device takes a larger share of the total current, the rapid fall-off in gain and the increase in V_{SAT} as it takes the higher share will prevent disaster. Thermal runaway in bipolar applications is not as frequent as we may believe [2-4].

For bipolar devices, the parameter having a clear negative temperature coefficient is V_{BE}. $V_{CE(SAT)}$, on the other hand, can have positive or negative temperature coefficient depending on the device type (npn or pnp) and operating point.

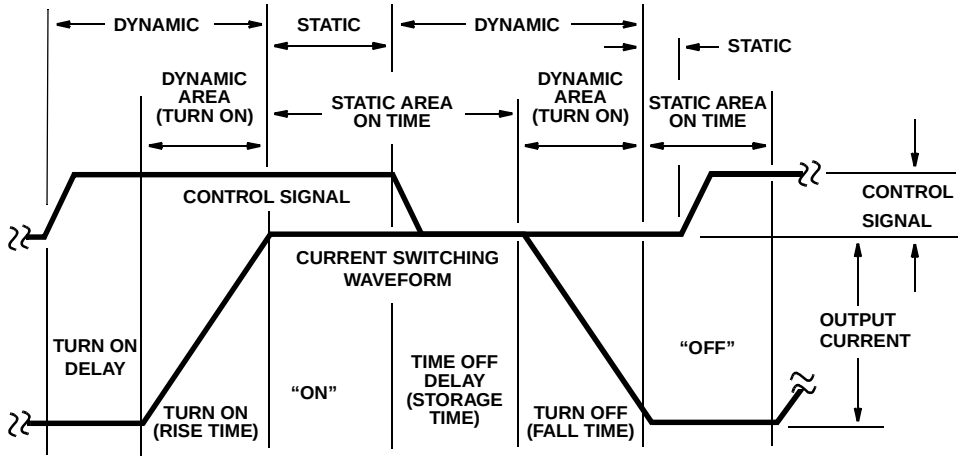

FIGURE 1. SWITCHING WAVEFORM DEFINITIONS

The ease of paralleling of power FETs has been pointed out by many authors [6-9], and has been demonstrated in many applications, although each application requires analysis of both dynamic and static sharing.

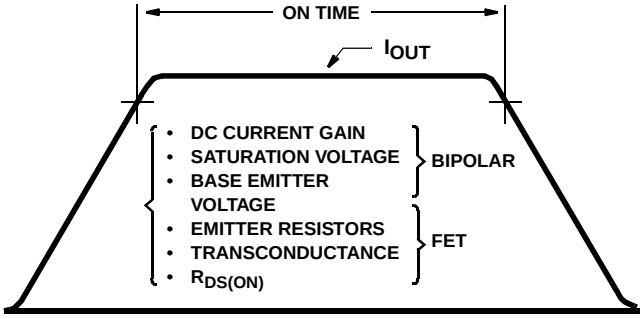

FIGURE 2. ON TIME OF SWITCHING WAVEFORM AND CONTROLLING PARAMETERS

Turn-On Delay Time

Turn-on delay time is the time from where the control signal is applied, reaches 10% amplitude, to the point where the switched current rises to the 10% amplitude (Figure 3).

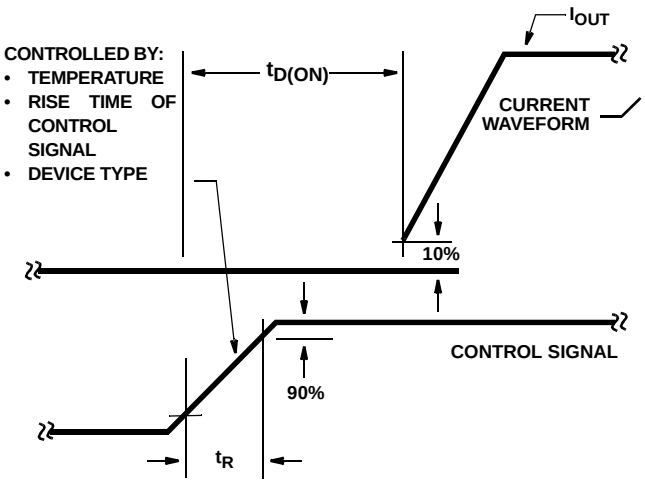

FIGURE 3. DEFINITION OF TURN-ON, DELAY TIME, $t_{D(ON)}$ AND CONTROLLING PARAMETERS

Fortunately, differences is turn-on delay are relatively small. Although this delay is significant in large-area SCR's, but it is much less a problem with bipolars or power FET's. It is less important when switching inductive loads, but should be monitored when devices to be paralleled switch resistive load, discharge capacitor or have to carry the recovery current of a diode.

Needless to say, it is desirable to have small turn-on delays for parallel operation. To reduce deltas in $t_{D(ON)}$, it is advisable to drive devices with fast rising control signals and use devices from the same mask design. The same device type number does not guarantee that they are made from the same mask design. Therefore, devices from different manufacturers should not be intermixed.

Rise Time

Rise time is an interesting part of the switching waveform (Figure 4). The device operates in an analog domain, although for a very short time, but nevertheless, analog.

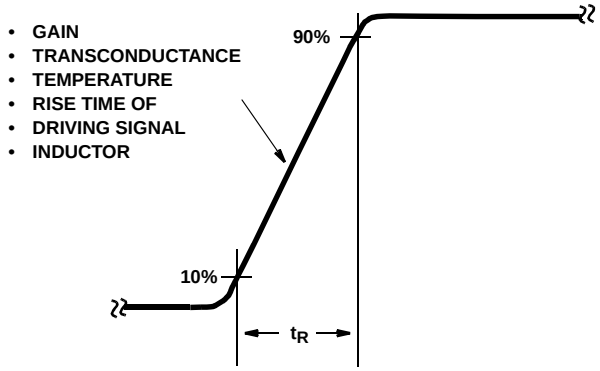

FIGURE 4. RISE TIME OF L_{OUT} WAVEFORMS AND PARAMETERS INFLUENCING IT

Again, transconductance and junction temperature become important considerations, but junction temperature differences as a result of rise time differences are relatively small. Inductors inserted into the emitter lead on bipolars, source lead on FET's or cathode lead on diodes, can be extremely effective [3]. All differences in turn-on delay and rise time become visible at thin part of the waveform. Differences which may exist, although small, require the evaluation of the forward biased safe operating area (FBSOA).

In most cases, transistors have almost rectangular FBSOA for the short durations they remain in the analog domain of the turn-on period. Problems seldom exist, but precautions should not be ignored either.

Note that the device with the shortest turn-on delay and the shortest rise-time will take most of the current. Most transistors have a negative temperature coefficient of input voltage and Miller effect feedback which can cause current begging if power dissipation is high during turn on.

Turn-Off Delay Time (Storage Time)

Turn-off delay time is the prelude to the most important part of the switching waveform, especially on bipolar devices (Figure 5). On bipolar devices, it is important to remove the stored charge as fast as possible, which may require more expensive drive circuitry. Especially on large power darlingtons, negative bias or baker clamps result in significant reduction of storage time and improve parallel operations. The transition time of the base current signal from positive to negative (npn device) is important in the removal rate of the stored charge.

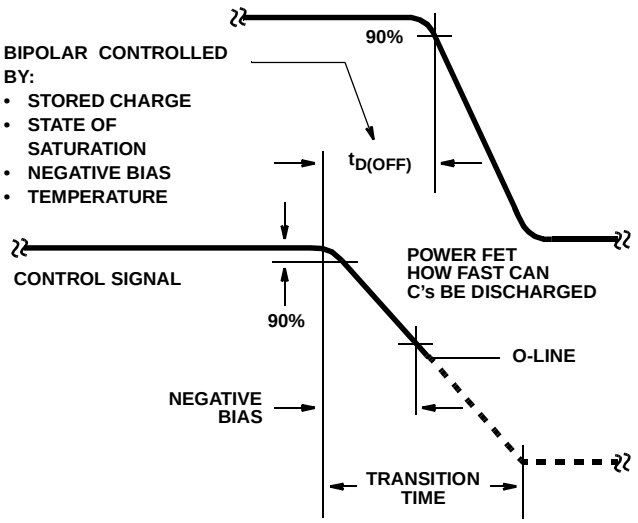

FIGURE 5. TURN-OFF WAVEFORM AND PARAMETERS INFLUENCING IT

Fall Time

Parameters which reduce storage time will also reduce fall time (Figure 6). For paralleled devices, differences in turn-off delay or storage time will have a noticeable effect on fall time.

When inductive loads are turned off, the reverse biased safe operating area (RBSOA) must be considered on bipolar devices. Hot spot formation [11] which results in sudden reduction of the V_{BE} and further increase in I_B could result in permanent damage.

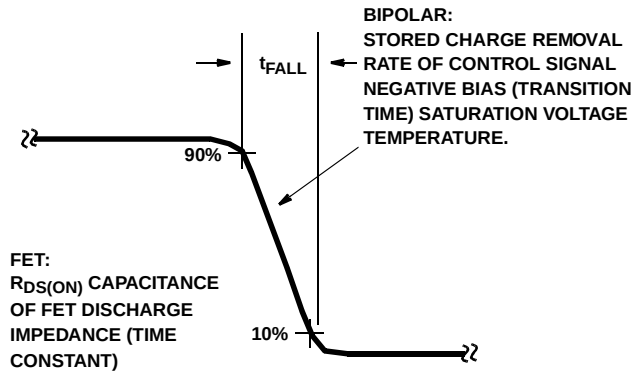

FIGURE 6. FALL TIME AND INFLUENCING PARAMETERS

The Insulated Gate Transistor

The insulated gate transistor (IGT) combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors, making it an ideal device for many power electronics switching control applications.

IGT Structure and Operation

The basic device structure is illustrated by the unit cell cross section of Figure 7. Like the MOSFET, the IGT consists of many individual cells connected in parallel. Processing of the IGT is similar to the vertical D-MOS technology used in MOSFETs. In the steady state, the n-channel IGT may be modeled as a bipolar pnp driven by an n-channel MOSFET. The MOSFET supplies base current to the pnp thus the MOSFETs gate voltage controls the total current.

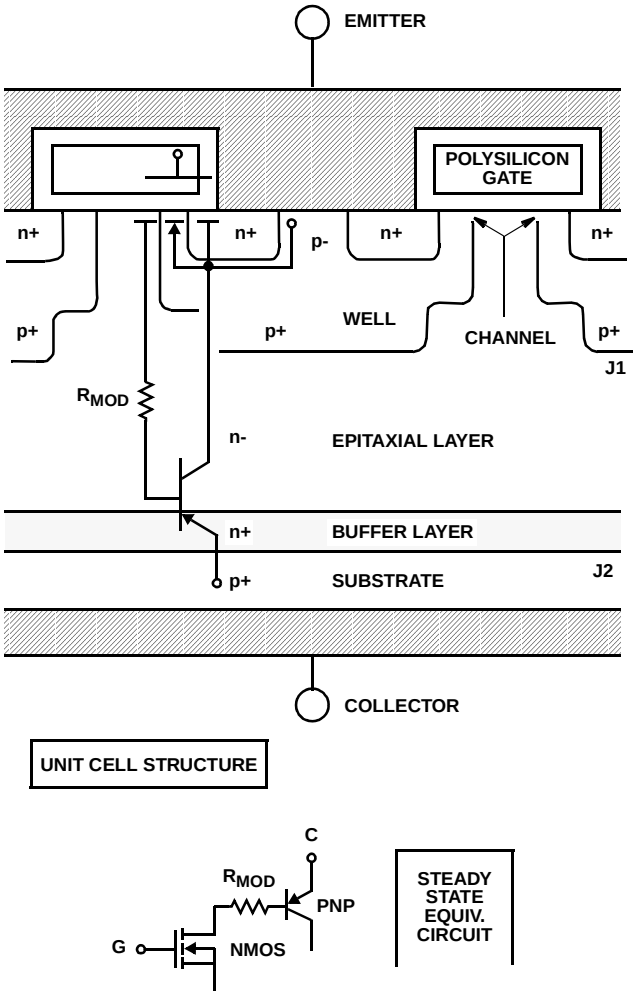

FIGURE 7. UNIT CELL CROSS SECTION AND STEADY STATE EQUIVALENT CIRCUIT OF IGT TRANSISTOR.

In normal operation, the emitter is grounded, the collector biased positive and with no gate-emitter voltage applied; J1 is reverse biased. The device is in the forward blocking mode. When a positive voltage is applied to the gate with respect to the emitter, an inversion channel is formed under the gate and MOSFET current flows from the n+ source region into the n-epi-layer to become the base current for the pnp. Junction J2 becomes forward biased and the device enters the conduction state. Holes are injected from the bot-

tom percent region into the n-epi-layer. The injected minority carrier density is 100 to 1000 times higher that the doping level of the n-type epi-region. This conductivity modulation allows the IGT to operate at a forward conduction current density 20 times that of an equivalent MOSFET. It is primarily in the thick epi, high-voltage devices where conductivity modulation has its major impact to reduce on-resistance.

The typical output characteristics and the symbol of the IGT are shown in Figure 8. Like on MOSFETs, the output characteristics curves are generated by plotting collector emitter currents, collector emitter voltage. Unlike the MOSFET, there is an offset voltage generated by the collector emitter junction of the npn-transistor. However, once this offset is overcome, the effective on-resistance in the saturation region is much lower for the IGT than for the MOSET.

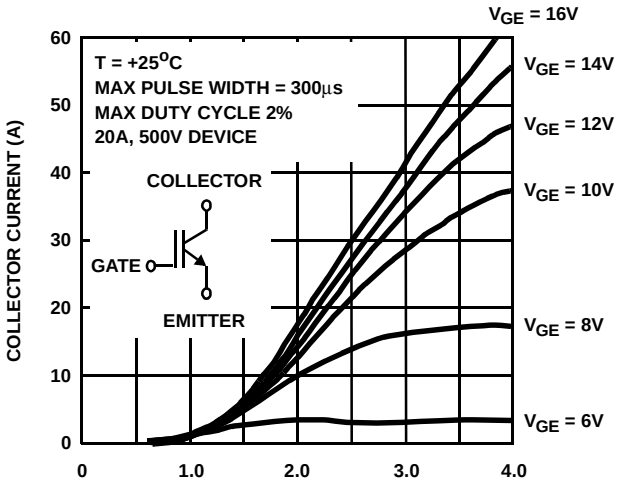

FIGURE 8. OUTPUT CHARACTERISTICS AND CIRCUIT SYMBOL FOR N-CHANNEL IGT TRANSISTOR

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