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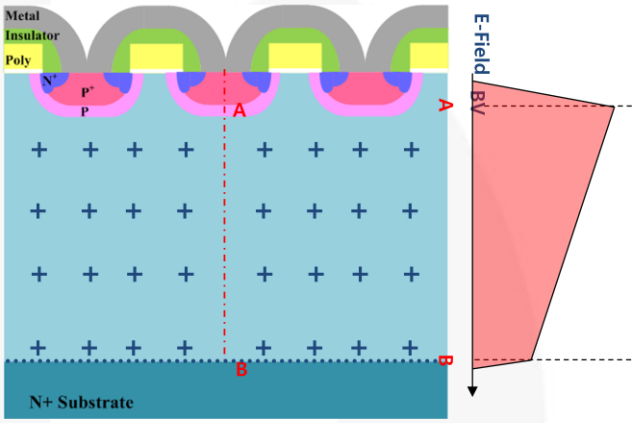
New Generation Super-Junction MOSFETs, SuperFET® II and SuperFET® II Easy Drive MOSFETs for High Efficiency and Lower Switching Noise

Introduction

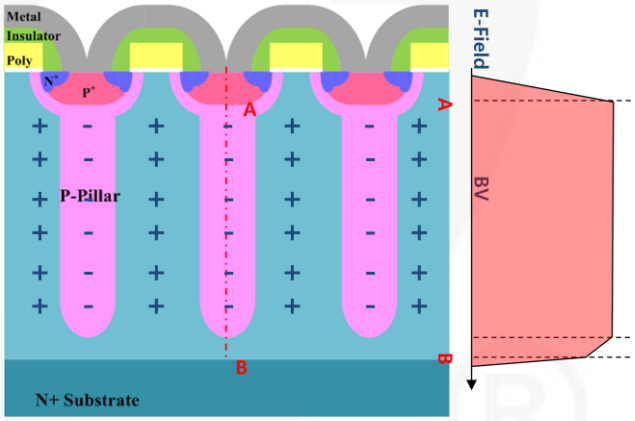
Power MOSFET technology has developed toward higher cell density for lower on-resistance. The super-junction device utilizing charge balance theory was introduced to semiconductor industry ten years ago and it set a new benchmark in the high-voltage power MOSFET market[1]. The Super-Junction (SJ) MOSFETs enable higher power conversion efficiency. However, the extremely fast switching performance of super-junction MOSFETs creates unwanted side effects, like high voltage or current spikes or poor EMI performance. Based on recent system trends, improving efficiency is a critical goal and using a slow switching device just for EMI is not an optimized solution. Fairchild recently added a SuperFET® II MOSFET family using the latest super-junction technology to the high-voltage power MOSFET portfolio. With this technology, Fairchild provides high performance in high-end, AC-DC SMPS applications such as servers, telecom, computing, industrial power supply, UPS/ESS, solar inverter, and lighting applications; as well as consumer electronics, which require high power density, system efficiency, and reliability. Utilizing an advanced charge-balance technology, Fairchild helps designers achieve more efficient and high-performance solutions that consume less board space and improve EMI and reliability by introducing the 600 V N-channel SuperFET® II MOSFET family.

Super-Junction MOSFET Technology

The $R_{DS(ON)} \times Q_G$, Figure Of Merit (FOM) is generally considered the single most-important indicator of MOSFET performance in Switching-Mode Power Supplies (SMPS). Therefore, several new technologies have been developed to improve the $R_{DS(ON)} \times Q_G$ FOM. Figure 1 shows vertical structure and electric field profile of a planar MOSFET and a super-junction MOSFET. Breakdown voltage of the planar MOSFET is determined by drift doping and its thickness. The slope of electric field distribution is proportional to drift doping. Therefore, thick and lightly doped epi is needed to support higher breakdown voltage.



Planar MOSFET



Super-Junction MOSFET

Figure 1. Vertical Structure and Electric Field Profile of Power MOSFETs

The major contribution to on-resistance of high-voltage MOSFET comes from the drift region: the on-resistance exponentially increases with the light doping and thick drift layer for higher breakdown voltage. In high-voltage MOSFET technologies, the most remarkable achievement for on-resistance reduction is super-junction technology shown in Figure 2. Super-junction technology has deep p-type pillar-like structure in the body in contrast to the well-like structure of conventional planar technology. The effect of the pillars is to confine the electric field in the lightly doped epi region. Thanks to this p-type pillar, the resistance of n-type epi can be dramatically reduced compared to the conventional planar technology, while maintaining same level of breakdown voltage[2]-[4]. This new technology broke silicon limits in terms of on-resistance and achieves only one-third specific on-resistance per unit area compared to planar processes. This technology also achieved unique non-linear parasitic capacitance characteristics and therefore enabled reduced switching power losses.

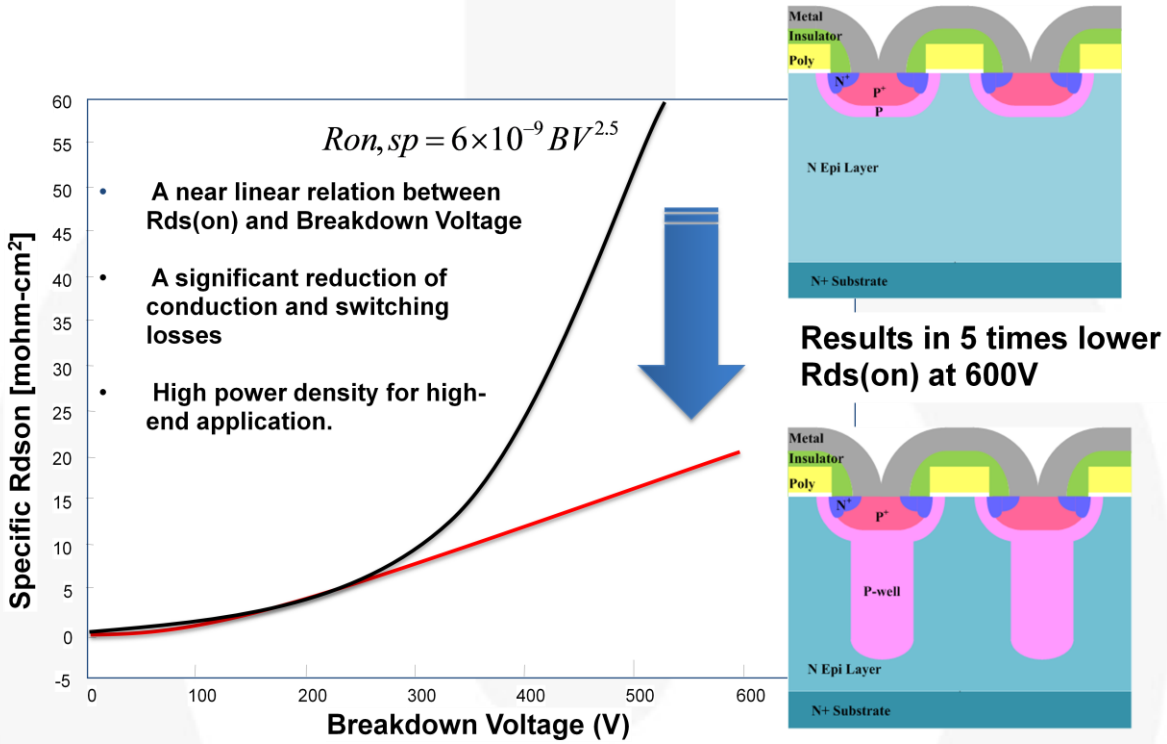


Figure 2. Specific $R_{DS(ON)}$ of Planar MOSFET / SJ MOSFET as Function of Breakdown Voltage

Table 1 shows the Fairchild super-junction MOSFET history. Fairchild's first super-junction MOSFET, the SuperFET® I MOSFET, surpassed performance of the planar MOSFET introduced during 2003. It has lower switching loss, robust body diode, and controlled dv/dt and di/dt characteristics under abnormal conditions. The fast-recovery SuperFET® I MOSFET with improved body diode performance was released at 2005. In 2009, the second-generation SJ MOSFET, SupreMOS® MOSFET, achieved much higher active cell density with simpler processes. Together with its fewer process steps, the on-resistance per specific area of SupreMOS® MOSFET is less than 40% of SuperFET® I MOSFET. A fast-recovery SupreMOS® MOSFET, suitable for resonant converters, was released in 2010. A new-generation SuperFET® II MOSFET offers in two product families: the SuperFET® II series is optimized for high-performance applications, similar to the SupreMOS® MOSFET, and SuperFET® II Easy Drive series is optimized for ease of use and low EMI noise, similar to the SuperFET® I MOSFET.

Table 1. Fairchild Super-Junction MOSFET Family and History

Product Family	Release	V_{th}	Characteristics	Internal R_g	Q_{rr}
SuperFET® I MOSFET	2003	4 V	Fast switching speed Best-in-class body diode ruggedness Ease of use	Small	Large
Fast-Recovery SuperFET® I MOSFET	2005	4 V	Fast recovery & robust body diode For resonant converter/inverter topologies	Small	Small
SupreMOS® MOSFET	2009	3 V	Extremely fast switching speed Lowest FOM for high efficiency	Small	Large
Fast-Recovery SupreMOS® MOSFET	2010	4 V	Fast recovery & robust body diode For resonant converter / inverter topologies	Small	Small
SuperFET® II MOSFET	2011	3 V	Maximized system efficiency Fast switching speed, but reduced dv/dt Improved body diode ruggedness	Small	Large
SuperFET® II MOSFET Easy Drive	2012	3 V	Ease of use Controlled di/dt and dv/dt at abnormal conditions Improved body diode ruggedness	Large	Large
Fast-Recovery SuperFET® II MOSFET	2012	4 V	Fast recovery & robust body diode For resonant converter / inverter topologies Enables 650 V rating	Small	Small

SuperFET® II MOSFET Family

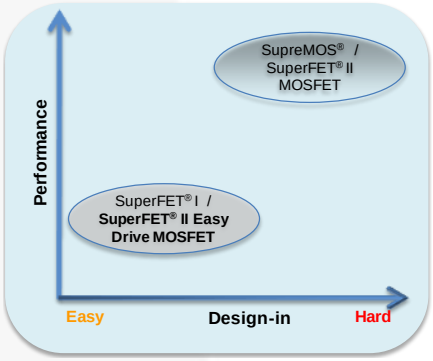


Figure 3. SuperFET® II MOSFET Concept

Figure 3 shows the SuperFET® II MOSFET concept. SuperFET® II series, which has excellent switching performance, can directly replace to SupreMOS® MOSFET. Switching dv/dt is lower than SupreMOS® MOSFET due to optimized gate charge and capacitances. SuperFET® II "Easy Drive" series, which has optimized switching performance, can directly replace the SuperFET® I MOSFET. It comes with an integrated gate resistor and optimized capacitance to achieve self-limiting di/dt and dv/dt characteristics. SuperFET® II Easy Drive series simplify implementation and enable low noise levels. Table 2 shows features and benefits of SuperFET® II MOSFETs.

Table 2. Features & Benefits of SuperFET® II MOSFET Technology

SuperFET II ® Easy Drive Series 600V	SuperFET II ® Series 600V
• Suffix "E" • Built-in Internal R_g • Optimized C_{gd} • Lower E_{oss} • Good body diode dv/dt	• No suffix • Reduced Q_g • Lower E_{oss} • Good body diode dv/dt
• Easy to design • Controllable dv/dt • Less gate oscillation and low EMI • Higher efficiency for light load conditions • Reliable operation for resonant converters	• Fast switching performance • High efficiency • Increased power density • Higher efficiency for light load conditions • Reliable operation for resonant converters

SuperFET® II Easy Drive Series

Internal Gate Resistor & Gate Charge

Super-Junction MOSFETs based on charge-balance technology offers outstanding performance with respect to reduced on-resistance and parasitic capacitance, which usually are in trade-off. With smaller parasitic capacitances, the SJ MOSFETs have extremely fast switching characteristics and reduced switching losses. However, without dv/dt control, the drain-source voltage slew rate can reach up to 100 V/ns, which can lead to EMI problems and unstable operation related to the stray parasitics in devices or printed circuit board and non-linear parasitic capacitances of SJ MOSFET in SMPS. The new-generation super-junction MOSFET, SuperFET® II device, enables optimized switching and low switching noise to achieve high efficiency and low EMI in applications due to optimized design. The high switching speed of SJ MOSFETs is reduces switching losses, but can have negative effects; such as increased EMI, gate oscillation, and high peak drain-source voltage in applications. A critical control parameter in gate-drive design is the external series gate resistor (R_g). This dampens the peak drain-source voltage and prevents gate ringing caused by lead inductance and parasitic capacitances of the power MOSFET. It also slows down the rate of rise of the voltage (dv/dt) and current (di/dt) during turn-on and turn-off. R_g also affects the switching losses in MOSFETs. Controlling these losses is important as devices must achieve the highest efficiency in the target application. From an application standpoint, selecting the correct value for R_g is very important. As shown in Figure 4, SuperFET® II Easy Drive series employs an integrated gate resistor, which is not Equivalent Series Resistor (ESR), but is a gate resistor, placed in gate pad, to reduce gate oscillation and control switching dv/dt and di/dt under high current conditions. The value of integrated gate resistance is optimized with gate charge.

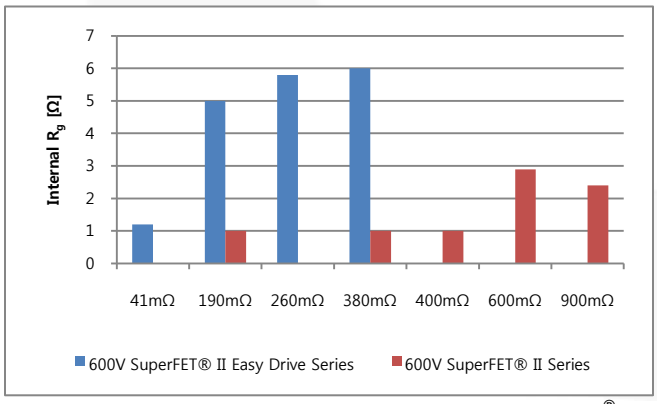


Figure 4. Internal Gate Resistor of 600 V SuperFET® II MOSFET Family

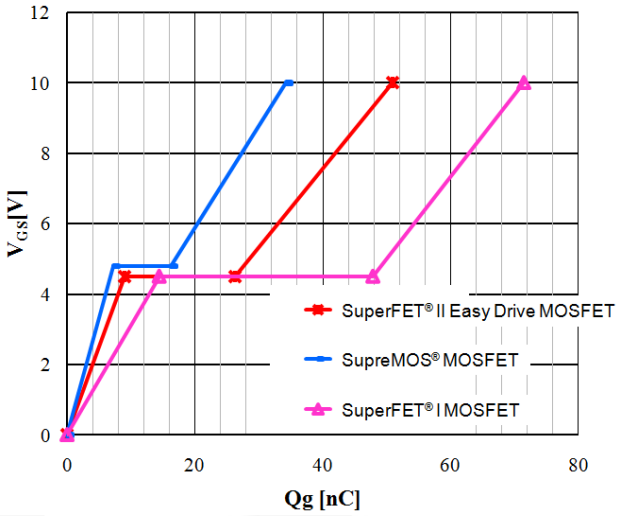


Figure 5. Comparisons of Gate Charge: 600 V/190 mΩ SuperFET® II Easy Drive MOSFET vs. 600 V/190 mΩ Previous-Generation SJ MOSFETs

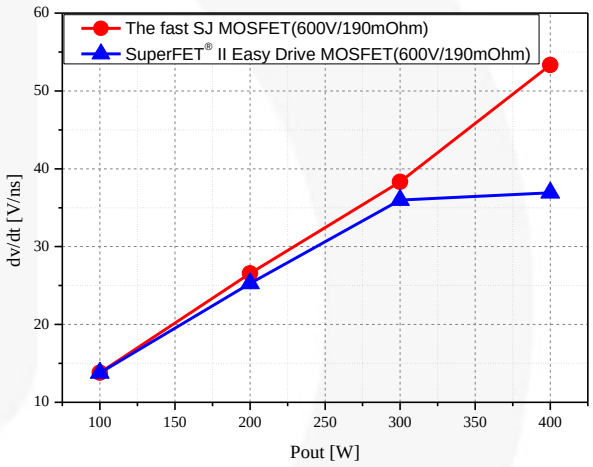


Figure 6. Comparison of Measured dv/dt: Fast SJ MOSFETs vs. SuperFET® II Easy Drive MOSFET during Turn-Off Transient in PFC Circuit (V_{IN}=100 V_{AC}, P_{OUT}=400 W, Rg=3.3 Ω)

The C_{oss} of super-junction MOSFET becomes strongly non-linear, decreasing very rapidly around 50 V drain-source voltage in the super-junction MOSFET. This allows an extremely fast dv/dt and di/dt. The reverse-transfer capacitance (C_{gd}), often referred to as Miller capacitance, is one of the major parameters affecting voltage rise and fall times during switching. C_{gd} provides a negative feedback effect from the drain voltage, and it must be discharged by the gate drive current supplied through R_g. The oscillations are related to several causes, such as high switching dv/dt and di/dt, parasitic C_{gd}, and the value of the drain current. Figure 5 shows a gate charge measurement of the SuperFET® II Easy Drive MOSFET and the previous generation of SJ MOSFETs with V_{DS}=480 V, V_{GS}=10 V, and I_D=10 A. As shown in Figure 5, the gate charge of the SuperFET® II Easy Drive MOSFET is optimized to improve the trade-off between switching losses and switching noise.

Due to optimized switching behavior of the SuperFET® II Easy Drive MOSFET in both gate-controlled and C_{gd}-limited switching, the SuperFET® II Easy Drive MOSFET can optimize efficiency while assuring reliable MOSFET operation and reducing EMI noise. Figure 6 shows an actual MOSFET dv/dt, comparing the fast SJ MOSFETs and SuperFET® II Easy Drive MOSFET during turn-off transient in PFC circuit from 100 W to 400 W under the same driving conditions. The linear rise of turn-off dv/dt in the fast SJ MOSFET shows that the dv/dt cannot be controlled in the PFC circuit with small gate resistance (3.3 Ω). The SuperFET® II Easy Drive MOSFET reduces the increase of turn-off dv/dt compared to the fast SJ MOSFET, but is still linearly increased under 300 W load condition. Under full load condition, dv/dt is controlled at 36 V/ns, which is reduced about 30.8% compared to the fast SJ MOSFET.

Stable Operation under Abnormal Conditions in SuperFET® II Easy Drive

Since a MOSFET is an uni-polar device, parasitic capacitances are the only limiting factors in the switching transient. The charge-balance principle lowers on-resistance per specific area and enables reduction in the chip size at the same $R_{DS(on)}$ compared to standard MOSFET technology. Figure 7 shows capacitances of SJ MOSFET and planar MOSFET. The C_{oss} of standard MOSFET shows moderately linear change, but C_{oss} curve of SJ MOSFET is highly non-linear. The initial value of C_{oss} of SJ MOSFET is much higher due to higher cell density, but C_{oss} decreases very rapidly around 50 V drain-source voltage in the SJ MOSFET, as shown in Figure 7. These effects allow an extremely fast dv/dt and di/dt and can cause voltage and current oscillation when SJ MOSFETs are used as a switching device for PFC or DC-DC converters.

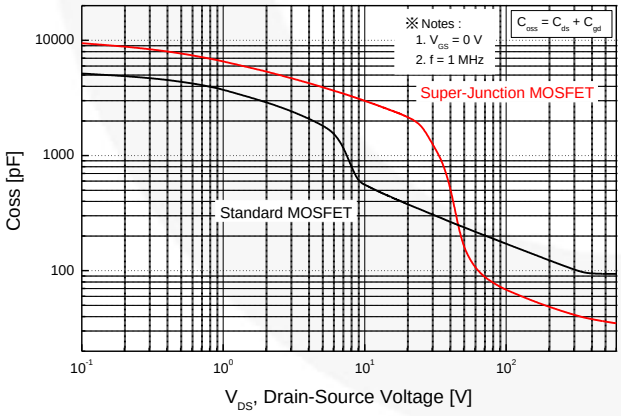


Figure 7. Comparisons of Output Capacitance between Planar MOSFET and Super-Junction MOSFET

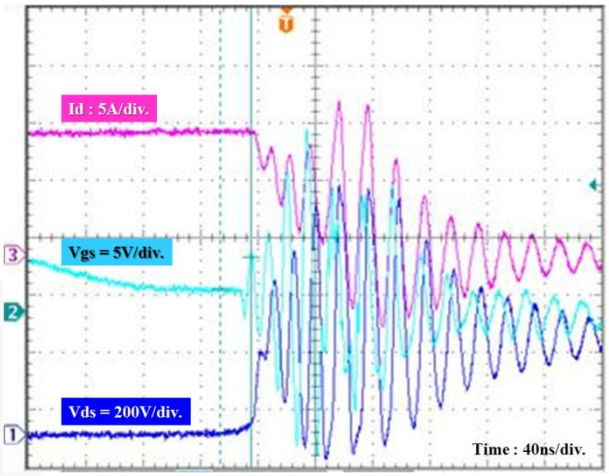


Figure 8. Severe Oscillation Waveforms in PFC Circuit Using Super-Junction MOSFET

Figure 8 shows observed oscillation waveforms in PFC circuit during turn-off transient of SJ MOSFET. Increasing gate resistance dampens the peak drain-source voltage and prevents gate oscillation caused by lead inductance and parasitic capacitances of the SJ MOSFET. It also slows down the rate of rise of the voltage (dv/dt) and current (di/dt) during turn-on and turn-off. External R_g also affects the switching losses in MOSFETs. Controlling these losses is important as devices must achieve the highest efficiency on the target application. From a general perspective, there are several oscillation circuits that affect the switching behavior of the MOSFET, including internal and external oscillation circuits[4]-[6]. Figure 9 shows a simplified schematic of a PFC circuit with both internal parasitics of the power MOSFET and external oscillation circuits given by the external coupling capacitance, $C_{gd\_ext.}$, and parasitic inductance of drain, source, and gate of the board layout. Parasitic components in the devices and boards are involving switching characteristics more as the switching speed is getting faster. In Figure 9, L, C_o, and D_{boost} are the inductor, output capacitor, and boost diode in PFC circuit. C_{gs}, C_{gd_int}, and C_{ds} are parasitic capacitances of the power MOSFET. L_{d1}, L_{s1}, and L_{g1} are the parasitic lead inductances of drain, source, and gate; including wire bonding of the power MOSFET. R_{g_int} and R_{g_ext} are the internal gate resistors of the power MOSFET and the external gate driving resistor of circuit. C_{gd_ext} is parasitic gate-drain capacitance of the circuit. L_D, L_S, and L_G are the drain, source, and the gate copper trace stray inductances of the printed circuit board. Gate parasitic oscillation occurs in a resonant circuit by gate-drain capacitance, C_{gd}, and gate lead inductance, L_{g1} when MOSFET is turned on and off. When the resonance condition ($\omega L = 1/\omega C$) occurs, an oscillation voltage much larger than drive voltage $V_{gs(in)}$ is generated in V_{gs} between the gate and source because the voltage oscillation due to resonance changes in proportion to the selectivity $Q(=\omega L/R = 1/\omega CR)$ of the resonant circuit in Figure 10. The voltage across the capacitor and inductor, V_C and V_L, respectively, is given by Equations (1) and (2).

$$V_C = \frac{I}{2\pi fC} = \frac{V}{\omega CR} = Q \cdot V \quad (1)$$

$$V_L = I \cdot 2\pi fL = \frac{V \cdot \omega L}{R} = Q \cdot V \quad (2)$$

where,

$$Q = \frac{\omega L}{R} = \frac{1}{\omega CR}$$

Oscillation voltage in drain-source of the MOSFET passes through gate-drain capacitance, C_{gd}, due to load wiring inductance L_D when MOSFET switching is getting fast, and particularly when it is turned off. A resonant circuit with gate lead inductance, L_{g1}, is formed. As gate resistor is extremely small, the oscillation circuit, Q, becomes large. When the resonance condition occurs, a large oscillation voltage is generated between that point and C_{gd} or L_{g1} and parasitic oscillation is caused. The voltage drop across L_S and L_{s1}, which can be represented by (3), is cause by negative drain current in turn-off transient. This voltage drop across stray source inductances generates oscillation in gate-source voltage. The parasitic oscillation can cause gate-source breakdown, bad EMI, large switching losses, losing gate control, and can lead to MOSFET failure.

$$\Delta V_{GS} = (L_S + L_{s1}) \cdot \frac{di_d(t)}{dt} \quad (3)$$

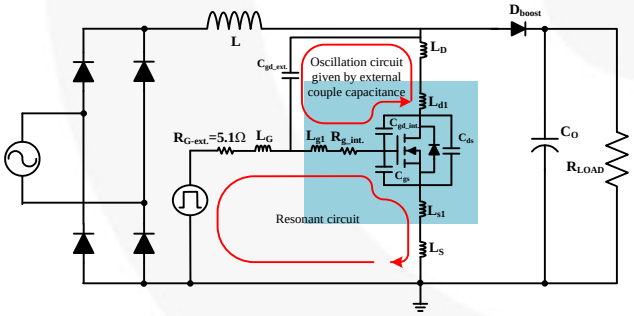


Figure 9. PFC Circuit with Internal and External Parasitic Components of Power MOSFET

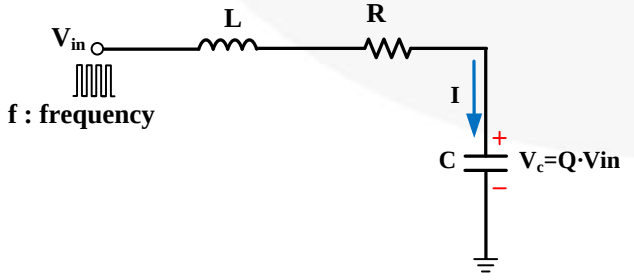
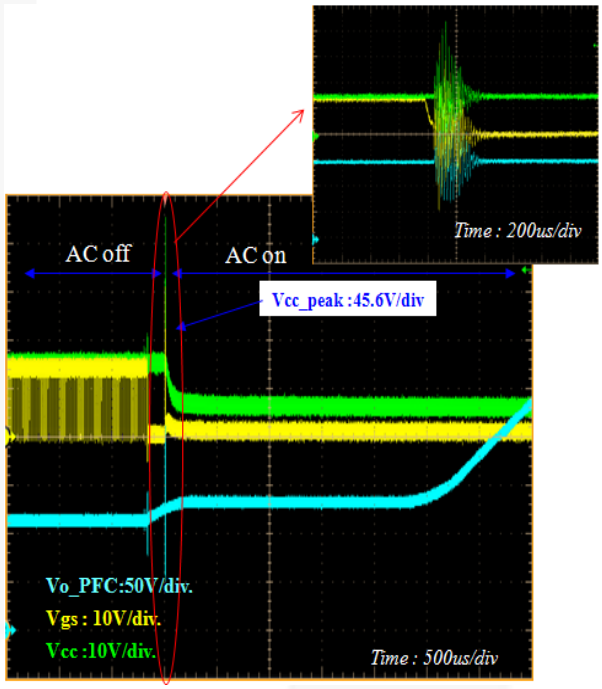
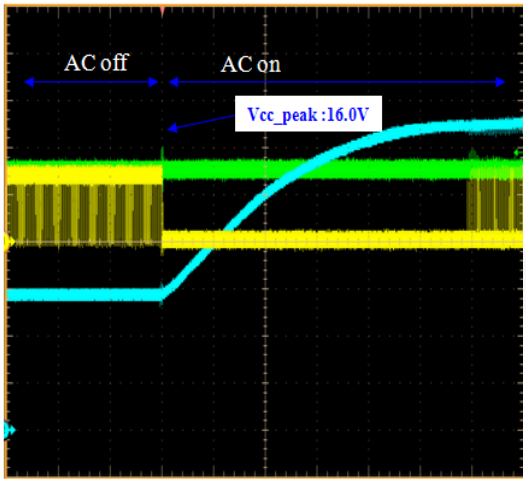


Figure 10. Resonant Circuit of R, L, and C

Experiment results verify the stable operation of SuperFET® II Easy Drive MOSFET in a PFC circuit. Measurements were taken in a PFC boost stage at the same input voltage, V_{IN}=110 V_{AC}, and output power level, P_{OUT}=300 W, during AC on/off test. Figure 11 presents waveforms comparing the difference in gate oscillations, V_{GS} (yellow line) at startup between the fast SJ MOSFET and SuperFET® II Easy Drive MOSFET. With fast SJ MOSFET, high peak gate oscillation, exceeding 45 V, is generated. It causes over-voltage latch-up and leads to absence of gate signal of the power MOSFET, as shown in Figure 11(a). The peak V_{CC} voltage is greatly reduced by up to 16 V and the latch-up problem is removed with SuperFET® II Easy Drive MOSFET, as shown in Figure 11(b).



(a) Fast Super-Junction MOSFET

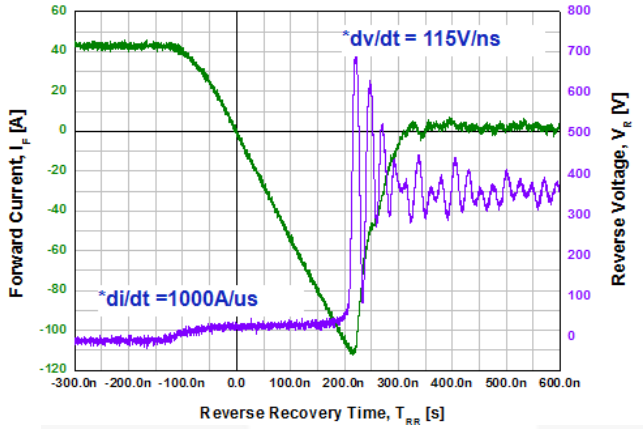


(b) SuperFET® II Easy Drive MOSFET

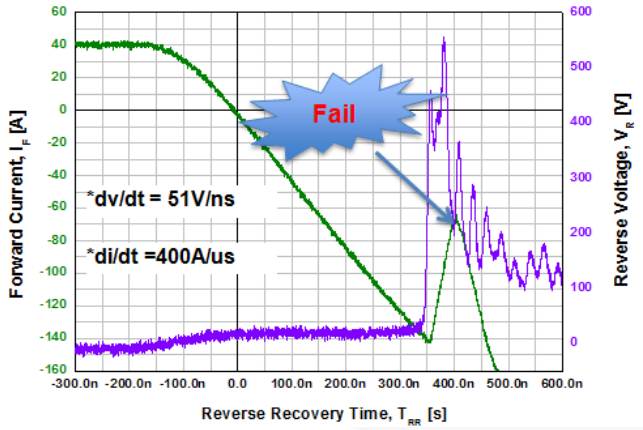
Figure 11. Comparisons of Waveforms during Startup State in PFC Circuit (V_{IN}=110 V_{AC}, P_{OUT}=300 W, V_{OUT}=380 V, 600 V/190 mΩ SJ MOSFET)

SuperFET® II Easy Drive Body Diode Performance

Figure 12 shows body diode reverse-recovery ruggedness, comparing the SuperFET® II Easy Drive MOSFET, FCH041N60E, and a 600 V/41 mΩ competitor. The SuperFET® II Easy Drive showed robust body diode compared to the competitor. The reverse-recovery measurements show that competitor fails at a di/dt of 400 A/µs and a dv/dt of 51 V/ns, where the SuperFET® II Easy Drive MOSFET survives >1000 A/µs and 115 V/ns. This type of failure is observed in many resonant topologies. The failing devices destroy themselves during the reverse-recovery phase where the voltage is high and current and di/dt is still high. The SuperFET® II Easy Drive MOSFETs provide high dv/dt ruggedness of the body diode for higher system reliability in ZVS topologies, such as phase-shifted full-bridge converters or LLC resonant half-bridge converters under abnormal conditions.[7]



(a) SuperFET® II Easy Drive MOSFET - FCH041N60E (600 V/41 mΩ)



(b) 600V/41 mΩ Competitor

Figure 12. Measured Body Diode Reverse-Recovery Ruggedness Waveforms Comparing FCH041N60E and 600 V / 41 mΩ Competitor

Stored Energy in Output Capacitance (E_{oss}) of SuperFET® II Easy Drive

In the soft-switching topologies, zero voltage turn-on is achieved by using the energy stored in inductor, the leakage, and series inductance or magnetizing inductance of the transformer to discharge the output capacitance of the switches through resonant action. The inductance should be precisely designed to prevent hard switching causing additional power losses. The following equations are basic requirements for zero voltage switching.

$$\frac{1}{2} L_{lk} I^2 > C_{eq} V_{in}^{\ 2} + \frac{1}{2} C_{TR} V_{in}^{\ 2}$$

where:

L_{lk} = Transformer leakage inductance;

C_{eq} = Output capacitance of the MOSFET; and

C_{TR} = Transformer output capacitance. (4)

$$L_m \le \frac{t_{dt}}{16 \cdot C_{eq} \cdot f_{s,\max}}$$

where:

L_m = Transformer magnetizing inductance;

t_{dt} = Dead time duration; and

$f_{s,\max}$ = Maximum switching frequency . (5)

Equation (4) is for phase-shifted full-bridge topology[8] and Equation (5) is for LLC resonant half-bridge topology.[9] The output capacitance plays an important role in both equations. If output capacitance is assumed too large in Equation (4), the equation gives larger inductance. The large inductance lowers primary di/dt and reduces effective duty of power converter. Too small output capacitance results in smaller inductance and unwanted hard switching. Too large output capacitance in Equation (5) limits magnetizing inductance and causes an increase in circulating current. Obtaining the exact output capacitance of the switches is critical to optimum design of soft-switching converters. Conventional assumptions for the equivalent output capacitance tends to use larger values. Designers should adjust the power converter after selecting inductance from Equation (4) or (5). Several design iterations are required because everything is related: for instance; turn ratio, leakage inductance, and effective duty cycle. The output capacitance of the power MOSFET is also varied by drain-source voltage.

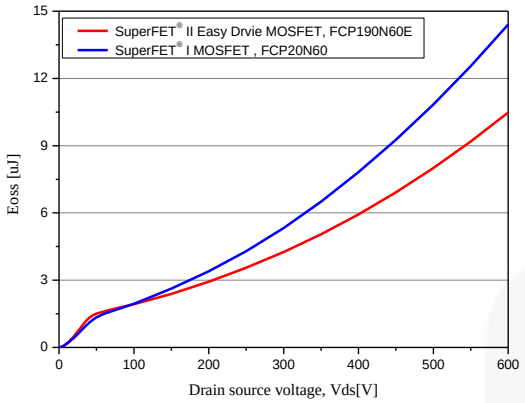


Figure 13. Comparisons of E_{OSS}: 600 V/190 mΩ SuperFET® II Easy Drive MOSFET vs. 600 V/190 mΩ SuperFET® I MOSFET

An output capacitance giving equivalent stored energy at the working voltage of power converter is the best alternative for these applications. MOSFET capacitance is nonlinear and depends on the drain-source voltage because its capacitance is essentially a junction capacitance. Among the parasitic elements, an output capacitance is a crucial parasitic parameter to set power converter design in ZVS topologies. It determines how much inductance is required to provide ZVS conditions because MOSFET output capacitance can be used as a resonant component in ZVS topologies. Therefore, if the stored energy in output capacitance of MOSFET is small, less resonant energy required to achieve soft switching without increasing the circulating energy. In hard-switching applications, the MOSFET channel conducts higher current than load current during turn-on, because of the additional discharging current of output capacitance. Therefore, E_{oss} of the MOSFET during turn-off is internally dissipated through the MOSFET channel during turn-on. The stored energy in output capacitance, E_{oss} of the MOSFET, is very critical in hard-switching applications, such as power factor correction (PFC), especially at light loads, because it is fixed and independent of load. A SuperFET® II Easy Drive, FCP190N60E, has approximately 20% less stored energy in output capacitance than SuperFET® I MOSFET FCP20N60 (for a typical switching power supply bulk capacitor voltage), as shown in Figure 13.

Table 3. Key Parameter Comparison of Fairchild Super-Junction MOSFET Family

Generation / Product	FCP20N60	FCP16N60N	FCP190N60E	FCP190N60
Specification	SuperFET® I MOSFET	SupreMOS® MOSFET	SuperFET® II Easy Drive Series MOSFET	SuperFET® II Series MOSFET
BV_{DSS} at T_J=25°2	600 V	600 V	600 V	600 V
I_D	20.0 A	16.0 A	20.6 A	20.2 A
FOM [$R_{DS(ON)}$×Q_G]	14.25 Ω nC	8.00 Ω·nC	11.97 Ω·nC	11.34 Ω nC
$R_{DS(ON)}$ Max.	190 mΩ	199 mΩ	190 mΩ	199 mΩ
$V_{GS(th)}$	3~5 V	2~4 V	2.5~3.5 V	2.5~3.5 V
Q_g	75.0 nC	40.2 nC	63.0 nC	57 nC
Q_{gs}	13.5 nC	6.7 nC	10.0 nC	9.0 nC
Q_{gd}	36.0 nC	12.9 nC	24.0 nC	21.0 nC
Int.R_g or ESR	1.5 Ω (ESR)	2.9 Ω (ESR)	5.0 Ω (Internal R_g)	1.0 Ω (ESR)
E_{OSS} at 400 V	7.8 µJ	5.4 µJ	5.9 µJ	5.9 µJ
Body Diode, Q_{RR}	10.5 µC	4.4 µC	3.8 µC	3.8 µC
Peak Diode Recovery dv/dt	4.5 V/ns	20.0 V/ns	20.0 V/ns	20.0 V/ns
MOSFET dv/dt		100 V/ns	100 V/ns	100 V/ns

SuperFET® II Series

SuperFET® II series is designed for high efficiency and power density applications. Based on experimental results, SuperFET® II series provides higher system efficiency by reduced gate charge and small ESR. SuperFET® II series provides superior switching performance and withstands extreme dv/dt rate. The SuperFET® II series is suitable for various AC-DC power conversion in switching-mode operation for system miniaturization, higher efficiency, and cooler thermal performance.

Gate Charge & Switching Behavior: SuperFET® II Series vs. SuperFET® II Easy Drive Series

Table 3 shows the key parameter comparison of Fairchild SJ MOSFET family. Reduced Miller capacitance is one of the advantages of SuperFET® II series, lowering switching and driving losses. It also reduces driving current capability. As shown in Figure 14, Q_g of the SuperFET® II series is about 10% less than the SuperFET® II Easy Drive series.

Figure 15 shows the measurement of E_{on} and E_{off} comparisons for 600 V SuperFET® II series vs. 600 V SuperFET® II Easy Drive series under V_{DD}=380 V, V_{GS}=15 V, R_G=4.7 Ω in various I_D conditions. Switching losses of SuperFET® II series are dramatically reduced compared to that of SuperFET® II Easy Drive series. E_{off} is 49% less for SuperFET® II series (FCP190N60) compared to that of SuperFET® II Easy Drive series (FCP190N60E). E_{on} is 47% less for SuperFET® II series (FCP190N60) compared to that of SuperFET® II Easy Drive series (FCP190N60E) under V_{DD}=380 V, V_{GS}=15 V, R_G=4.7 Ω, as shown in Figure 16.

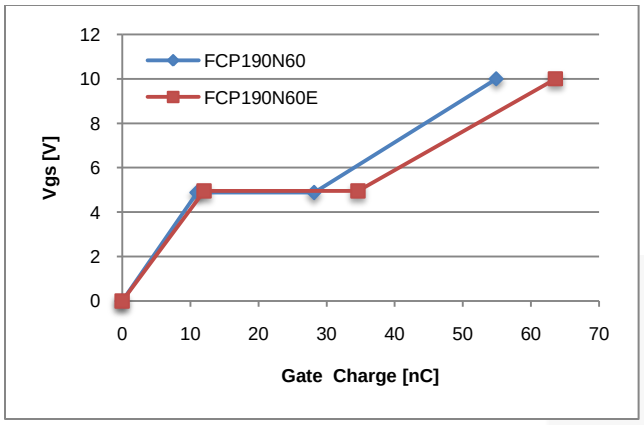
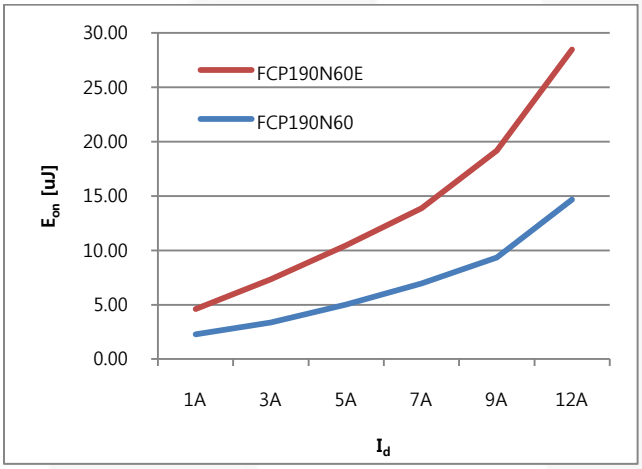
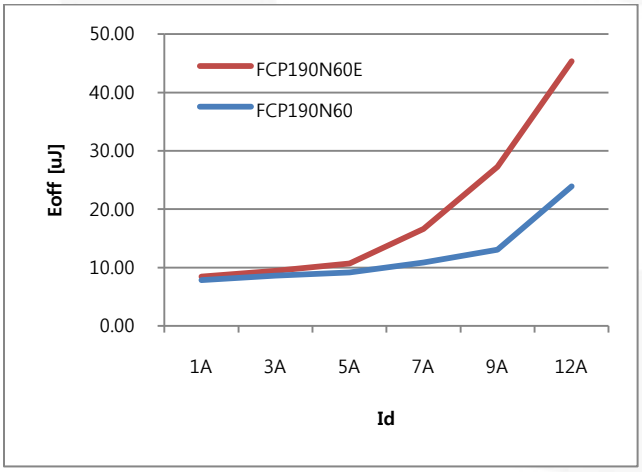


Figure 14. Gate Charge: 600 V SuperFET® II Series vs. 600 V SuperFET® II Easy Drive Series: FCP190N60 vs. FCP190N60E

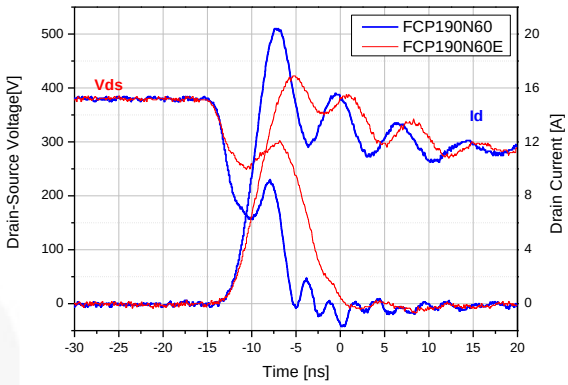


(a) E_{on} Comparison: FCP190N60 vs. FCP190N60E

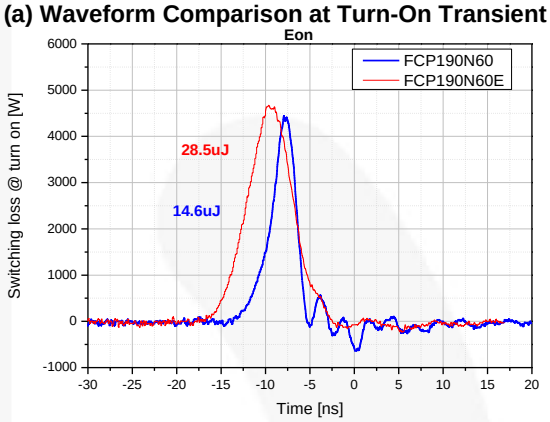


(b) E_{off} Comparison: FCP190N60 vs. FCP190N60E

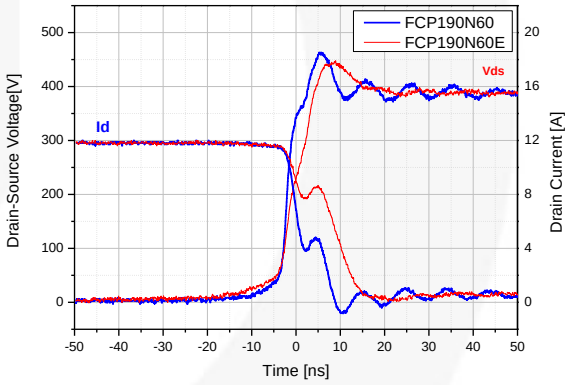
Figure 15. 600 V SuperFET® II Series vs. 600 V SuperFET® II Easy Drive Series under V_{DD}=380 V, V_{GS}=15 V, R_G=4.7 Ω: FCP190N60 vs. FCP190N60E



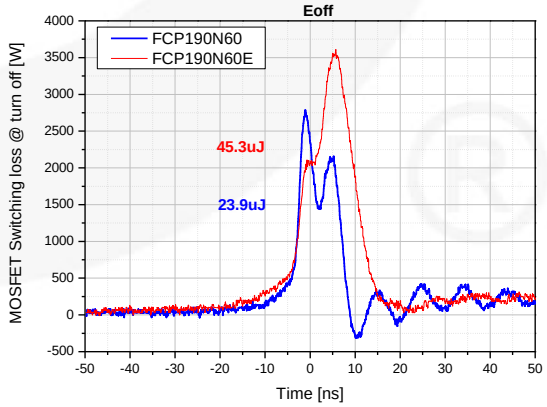
(a) Waveform Comparison at Turn-On Transient



(b) Turn-On Switching Loss Comparison



(c) Waveform Comparison at Turn-Off Transient



(d) Turn-Off Switching Loss:

Figure 16. FCP190N60 vs. FCP190N60E Switching Waveforms and Losses under V_{DD}=380 V, I_D=12 A, V_{GS}=15 V, R_G=4.7 Ω

Efficiency Comparison in 400 W CCM PFC

400 W CCM PFC is used to compare the efficiency of the SuperFET® II series vs. the SuperFET® II Easy Drive series. Input voltage of this rectifier is 100 V_{AC} and output voltage and current are set to 400 V and 1 A, respectively. Switching frequency is 95 kHz and gate resistor for turn-on is 10 Ω and turn-off is 3.3 Ω. The efficiency measurements are shown in Figure 17. Efficiency of SuperFET® II MOSFET (FCP190N60) increases about 0.2% compared to SuperFET® II Easy Drive MOSFET (FDP190N60E) at full-load condition. The major reason for higher efficiency is the reduced switching and driving loss because of lower Miller capacitance and Q_g. The faster switching of the power MOSFETs enable higher power conversion efficiency. However, parasitic components in the devices and boards are involving switching characteristics more as the switching speed is getting faster.

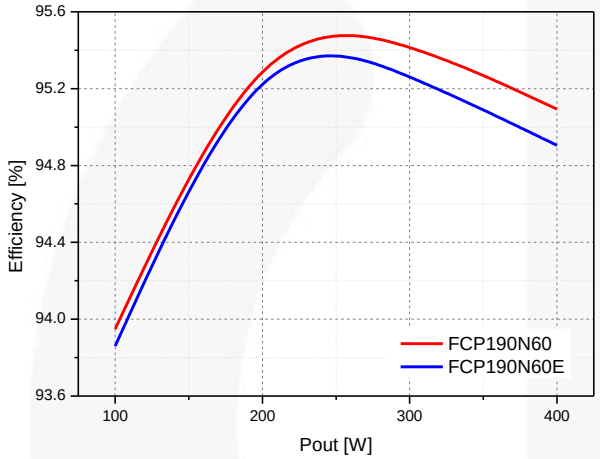


Figure 17. Efficiency Comparisons at 400 W CCM PFC

Layout Requirements for SuperFET® II Series

This creates unwanted side effects, like high voltage or current spikes or poor EMI performance. To achieve balance, it is important to have optimized gate drive circuitry because a power MOSFET is a gate-controlled device. Minimizing of parasitic inductance and capacitance on PCB board is also important.

Oscillation Mechanism of Power MOSFET at Turn-off Transient

To explain oscillation mechanism, transient switching behavior is simulated using analytical PSPICE simulation, focusing on the impact of parasitic inductances, L_G and L_S, in a power MOSFET and printed circuit board layout during turn-off transient. Figure 18 shows the PSPICE simulation waveforms of the gate-to-source voltage, V_{GS}; the internal gate-to-source voltage, V_{GS_int}; the drain-to-source voltage, V_{DS}; the current channel of MOSFET, $I_{channel}$; and the drain current, I_D, in clamped inductive load switching circuit. To explain the gate oscillation of the power MOSFET with the effect of parasitic inductances, the turn-off transient is divided into two intervals (t_1~t_2). Figure 19 shows the MOSFET equivalent circuit including parasitic inductances.

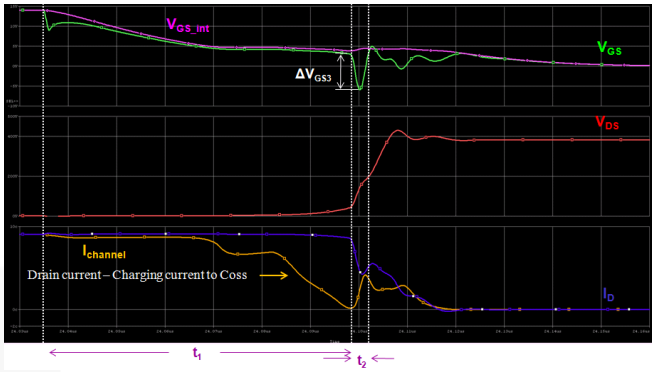
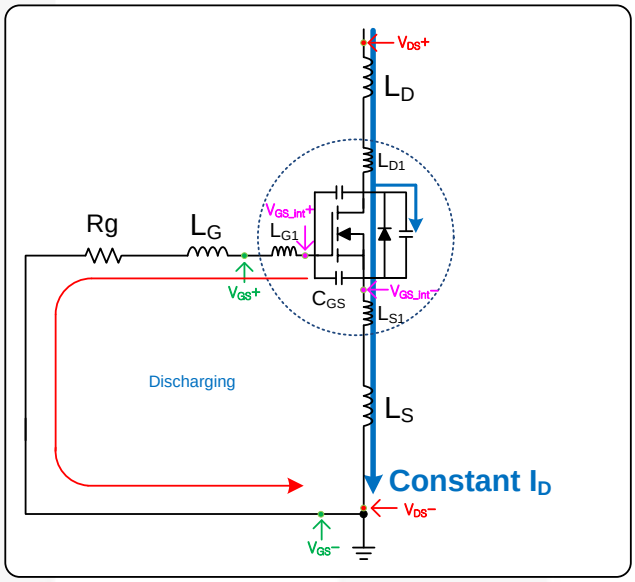
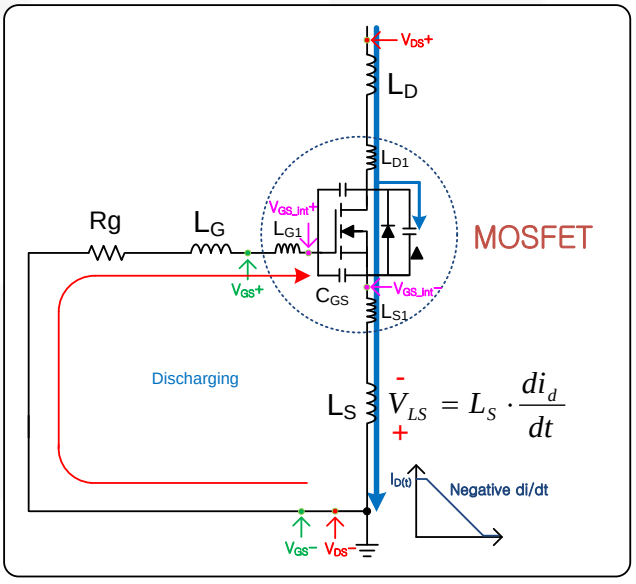


Figure 18. Simulation Waveforms at Turn-Off Transient



(a) MOSFET Operation during t_1



(b) MOSFET Operation during t_2

Figure 19. MOSFET Equivalent, including Parasitic Inductances

During Time Interval t_1

The voltage V_{GS} decreases exponentially due to discharging of input capacitance, which the gate-to-source capacitance, C_{GS}, and the gate-to-drain capacitance, C_{GD}, via the gate resistance, R_g, as shown in Figure 19(a). When the gate voltage reaches the gate plateau voltage, the channel current in the MOSFET is reduced due to output characteristics in MOSFET, which is a characteristic curve between the gate voltage and drain current. At the same time, the output capacitance is charged up slowly.

During Time Interval t_2

The C_{oss} of the SJ MOSFET becomes strongly non-linear, that is, C_{oss} decreases very rapidly around 30~50 V drain-source voltage in the SJ MOSFET. These effect give an extremely fast dv/dt and di/dt, as shown in Figure 18. At the same time, the voltage drop across the common-source inductance L_S is caused by negative drain current slope ($-di_D/dt$). This voltage drop leads to negative gate voltage. Due to this effect, the discharged current flows in the opposite direction, as shown in Figure 19(b). In this time, this equivalent circuit can be expressed as R-L-C series resonance circuits. Two different values of gate inductance are compared in a clamped inductive load switching circuit. A circuit with a low value for L_G has lower peak gate negative voltage ($\triangle V_{GSA}$). A circuit with a high L_G value shows much higher peak gate negative voltage ($\triangle V_{GSB}$), as shown in Figure 20. To achieve optimized gate waveform, reduce gate inductance L_G and common-source inductance L_S.

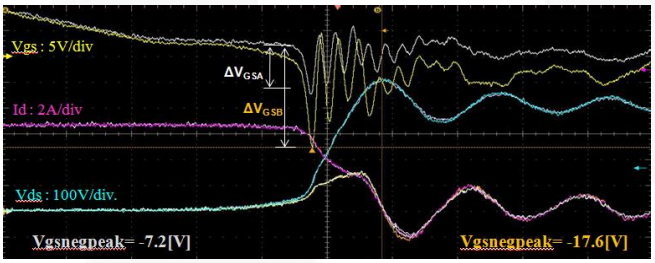


Figure 20. Gate Oscillation Comparison According to L_G

External Parasitic Inductances

Inductances and current loops have an influence on performance in any given application. Currents run in a loop and create a magnetic field. If a change in the current occurs, the magnetic field changes and creates an inductive voltage, V_L. With Faraday's law, the value of V_L can be calculated by:

$$V_L = -\frac{d\phi}{dt} = -L\frac{di}{dt} \; with \; \phi = \int_A B \cdot dA = L \cdot \quad (6)$$

Therefore, L depends also on the geometry of the loop. The bigger area of the current loop, the larger inductance, L. If the change in the current (di/dt) is stable, but higher inductance comes from the current loop, V_L increases. Enclosed current loops with high di/dt values should be minimized. The source and gate inductance must be minimized to avoid poor EMI and switching behaviors. For example, a 1 cm track on a PCB is almost the same, with 6-10 nH inductive impedance. The most important means of avoiding oscillation is minimizing the inductances. A configuration of gate drive circuitry is also important to switching characteristics. In Figure 21 and Figure 22, two types of gate drivers are considered. One is a diode turn-off speed-up gate drive circuit (Figure 21) that is most popular for fast speed turn-off. The fast turn-off transient causes high di/dt and high voltage drop across the source inductance (Ldi/dt) generates gate oscillation. The other is a PNP transistor turn-off gate drive circuit (Figure 22) that minimizes the turn-off loop.

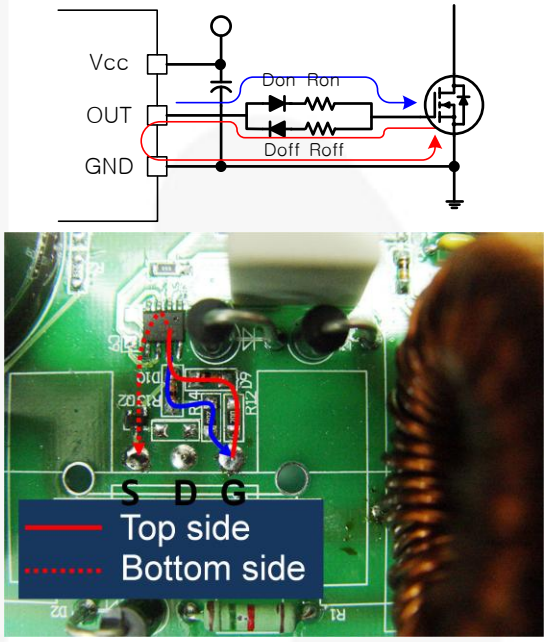


Figure 21. Diode Turn-Off Speed-up Gate Drive Circuit and Layout

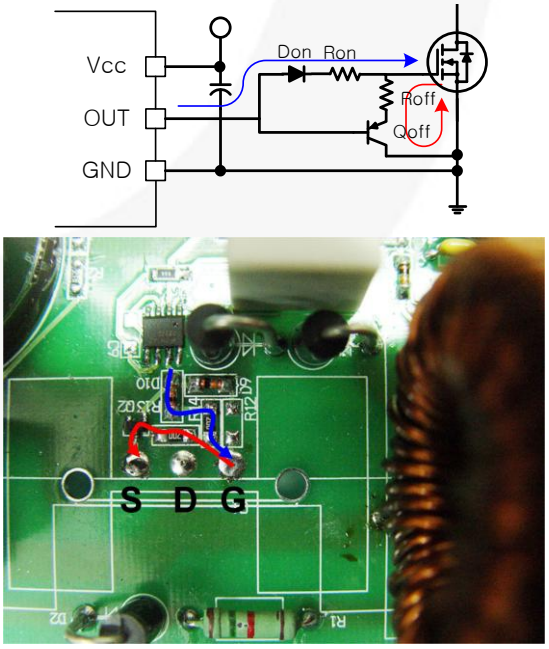


Figure 22. PNP Transistor Turn-Off Gate Drive Circuit and Layout

This configuration can minimize source inductance in the gate drive loop and fast turn-off. Figure 23 and Figure 24 show the gate-source waveforms with diode turn-off speed-up gate drive and PNP transistor turn-off gate drive. As shown in Figure 24, the PNP transistor turn-off circuit is the better configuration for reduced gate oscillation and switching loss.

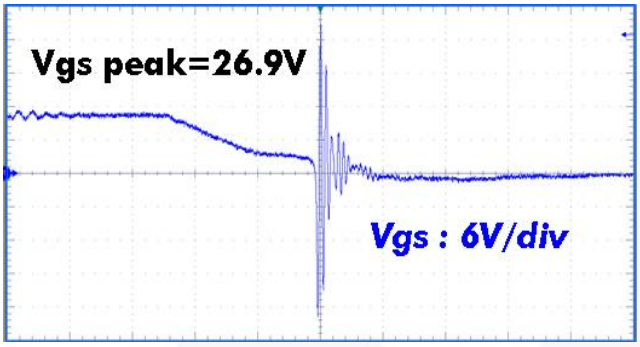


Figure 23. Gate-Source Voltage Waveform with Diode Turn-Off Speed-up Gate Drive Circuit

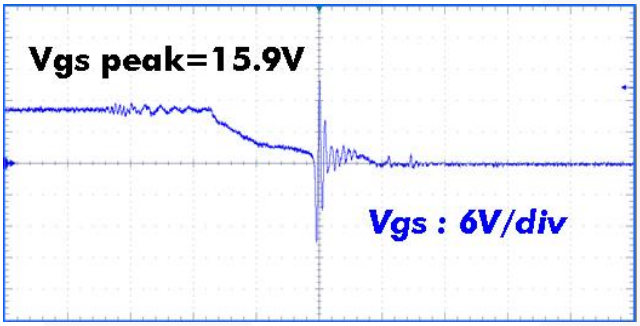


Figure 24. Gate-Source Voltage Waveform with PNP Transistor Turn-Off Gate Drive Circuit

External Parasitic Coupling Drain-Source Capacitances

External coupling C_{gd} is one of the root causes for ringing affected by the device and PCB layout.

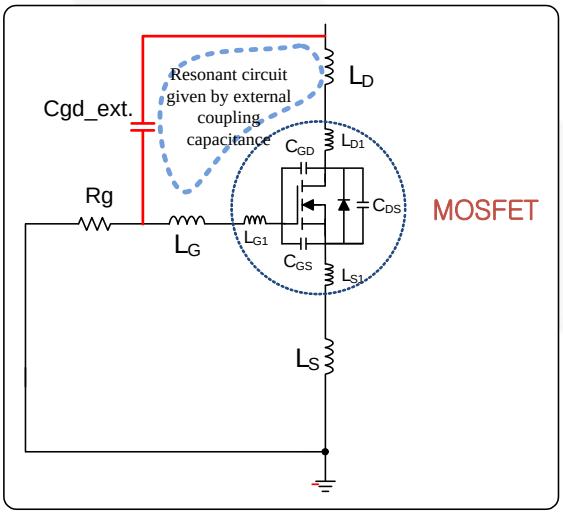


Figure 25. MOSFET Equivalent, Including Parasitic Coupling Capacitance

Figure 25 shows the MOSFET equivalent circuit, including resonant circuit with coupling gate-drain capacitance. External gate-drain capacitance is coupled through parasitic inductances, leading to resonance, causing gate oscillation with gate and drain inductance when MOSFET switching speed is fast. It could lead to the gate oscillation at turn-on and turn-off, destruction of gate oxide, or out–of-control or poor EMI performance. External coupling C_{gd} must be reduced as much as possible to reduce gate oscillation. The capacity between traces can be calculated by Equation (7):

$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{d} \quad (7)$$

Figure 26 and Figure 27 show layout examples with high external C_{gd}. Figure 28 and Figure 29 show layout solutions with reduced external C_{gd}. The difference in oscillations is shown in Figure 30 and Figure 31. V_{GS} (green line) and V_{DS} (magenta line) are during turn off. The experimental waveforms show the effect of the high and low external C_{gd} in a given layout. The oscillation effect can be forced by increasing the output power level or decreasing the input voltage at the same output power.

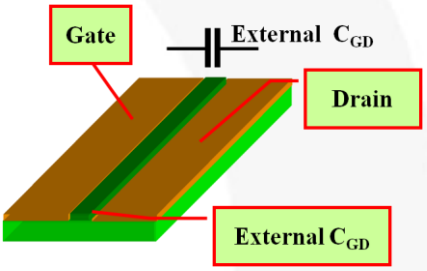


Figure 26. Single Layer Layout Example with Increased External C_{gd}

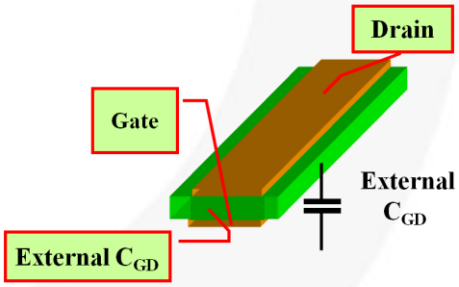


Figure 27. Double-Layer Layout Example with Increased External C_{gd}

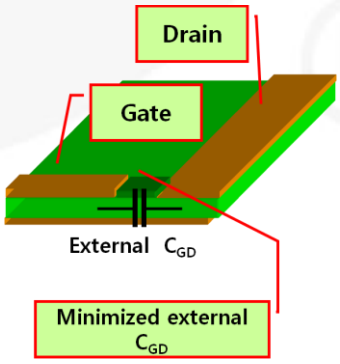


Figure 28. Single-Layer Layout Example with Reduced External C_{GD}

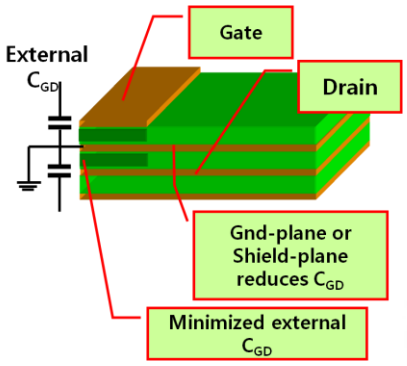


Figure 29. Double-Layer Layout Example with Reduced External C_{GD}

This can also occur after an AC line drop out: when line voltage is back, the boost stage charges up the bulk capacitor to nominal voltage. During the time when the MOSFET turns off, the drain current is quite high. The drain current commutates to the output capacitance, C_{oss}, of the MOSFET and charges it up to DC bus voltage. The voltage slope is proportional to the load current and inversely proportional to the value of the output capacitance. The value of C_{oss} is high at low V_{DS} and low at high V_{DS}. As a result, dv/dt values of drain-source voltage change during turn-off. The high dv/dt values lead to capacitive displacement currents due to all the parasitic capacitances.

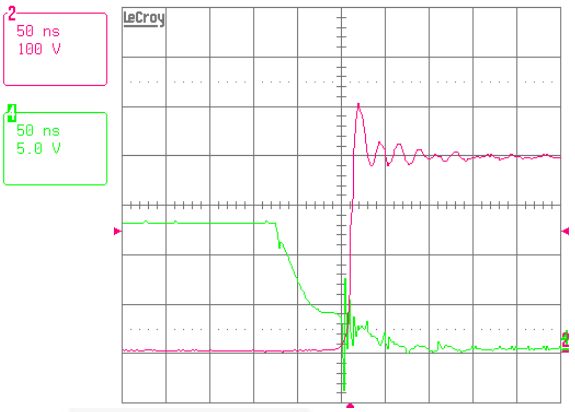


Figure 30. Turn-Off Waveforms with High C_{GD_EXT}

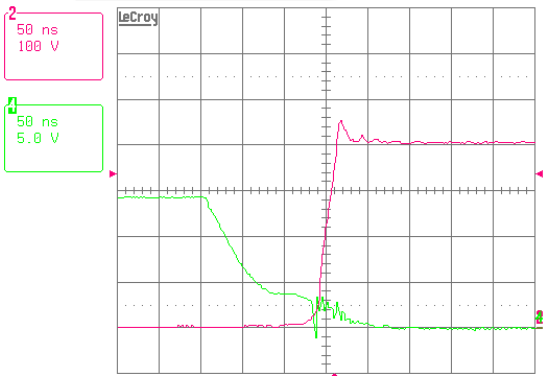


Figure 31. Turn-Off Waveforms with Low C_{GD_EXT}

Figure 32 and Figure 33 show bad and good PCB layout examples. To drive fast switching super-junction MOSFETs in different applications, it is necessary to understand the influence of parasitics in layout. There are many considerations to design PCB layout with fast switching MOSFETs. The below recommendation are important to achieve both high efficiency without voltage spikes and lower EMI with fast switching MOSFETs.

Layout Guideline Summary for Fast Super-Junction MOSFETs

- To achieve the best performance of SJ MOSFETs, optimized layout is required.
- Gate driver and R_g must be placed as close as possible to the MOSFET gate pin.
- Separate POWER GND and GATE driver GND.
- Minimize parasitic C_{gd} capacitance and source inductance on PCB.
- For paralleling SJ MOSFETs, symmetrical layout is mandatory.
- Slow down dv/dt, di/dt by increasing R_g or using a ferrite bead.

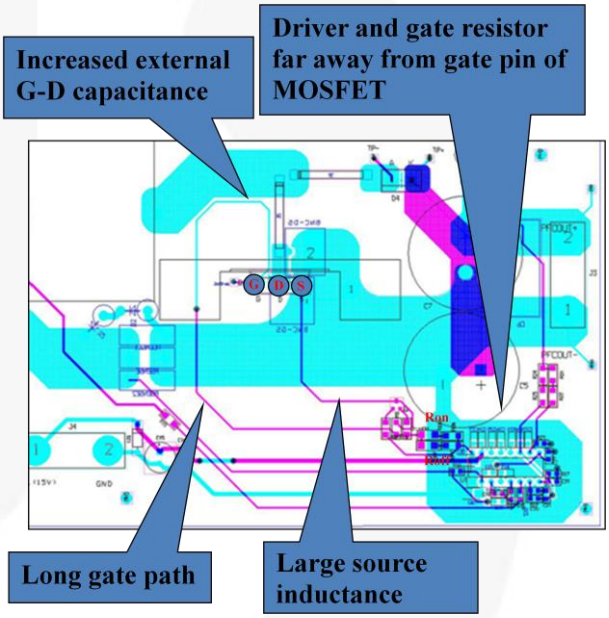


Figure 32. Bad Layout Example

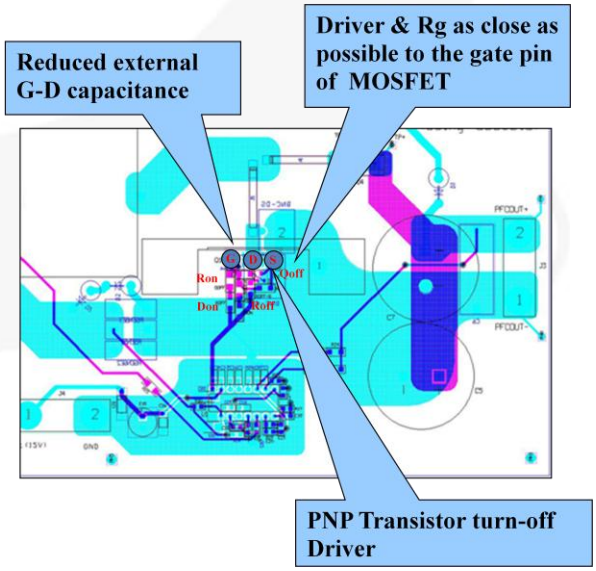


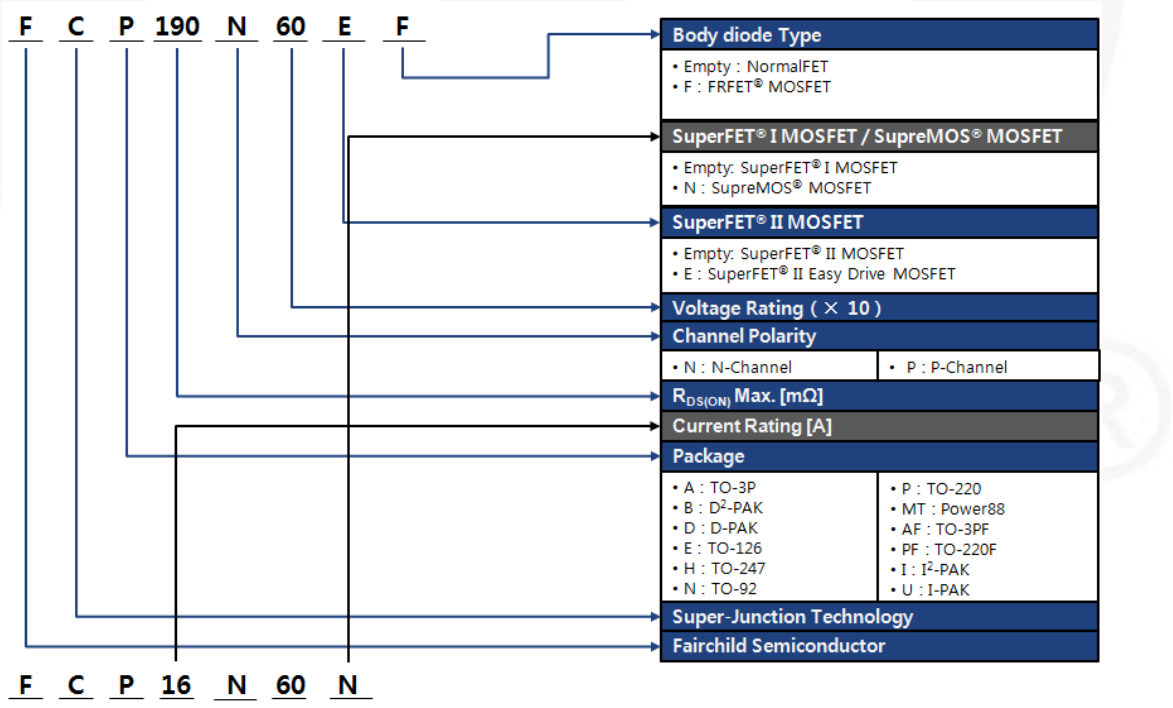
Figure 33. Good Layout Example

Table 4. 600 V SuperFET® II / SuperFET® II Easy-Drive MOSFET Product Portfolio

Technology	Part Number(1)	BV_{DSS} [V]	$R_{DS(ON).max}$ [mΩ] at V_{GS} = 10 V	$Q_{g.typ}$ [nC] at V_{GS} = 10 V	I_D [A]	Int. R_g [Ω]	Package
SuperFET® II Series	FCP190N60	600	199	57	20.2	1	TO220
	FCPF190N60	600	199	57	20.2	1	TO220F
	FCP380N60	600	380	30	10.2	1	TO220
	FCPF380N60	600	380	30	10.2	1	TO220F
	FCPF400N60	600	400	28	10	1	TO220F
	FCD600N60Z	600	600	20	7.4	2.89	DPAK
	FCP600N60Z	600	600	20	7.4	2.89	TO220
	FCPF600N60Z	600	600	20	7.4	2.89	TO220F
	FCU900N60Z	600	900	13.1	4.5	2.4	IPAK Short Lead
	FCD900N60Z	600	900	13	4.5	2.4	DPAK
SuperFET® II Easy Drive Series	FCH041N60E	600	41	285	48.7	1.2	TO247
	FCP190N60E	600	190	63	20.6	5	TO220
	FCPF190N60E	600	190	63	20.6	5	TO220F
	FCP260N60E	600	260	48	15	5.8	TO220
	FCPF260N60E	600	260	48	15	5.8	TO220F
	FCD380N60E	600	380	34	10.2	6	DPAK
	FCP380N60E	600	380	34	10.2	6	TO220
	FCPF380N60E	600	380	34	10.2	6	TO220F

Note:
1. Part suffix: E = SuperFET® II Easy Drive, Z = internal ESD diode.

Fairchild Super-Junction MOSFETs Ordering Information



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Related Datasheets

SuperFET® II and SuperFET® II Easy-Drive MOSFETs

Related Application Notes

AN-9005 – Driving and Layout Design for Fast Switching Super-Junction MOSFETs

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