Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

AN-7017

Reducing Power Losses in MOSFETs by Controlling Gate Parameters

Alan Elbanhawy, Fairchild Semiconductor

Introduction

The gate Equivalent Series Resistance (ESR) has been recognized as a factor affecting the losses in MOSFETs for a number of years. Controlling the losses is exceedingly important as devices need to produce the highest power conversion efficiency and lowest losses to operate efficiently at the target application. From an applications standpoint, an increase in losses can lead to overheating in the actual system requiring additional components such as heat sinks and fans. Additional components add to the overall cost and size of the end application. This application note explore ways to control these losses in MOSFETs.

What this application note will do:

- Provide guidance in selecting the right MOSFET for a specific application
- Optimize overall design by correct selection
- Explore the three distinct effects of gate ESR

The Effect of Rg on Switching Current Distribution

One of the first effects this application note will be explore is current distribution across the die during turn on and off. The gate ESR (Rg) together with the gate-source capacitance (Cgs) are distributed parameters across the MOSFET die.

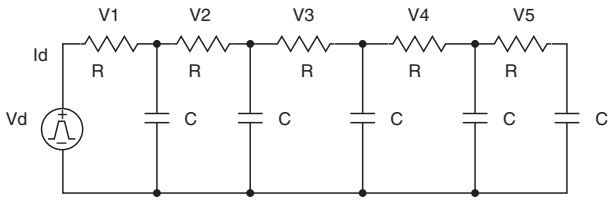

Figure 1. Simplified schematic for the solution of the current distribution

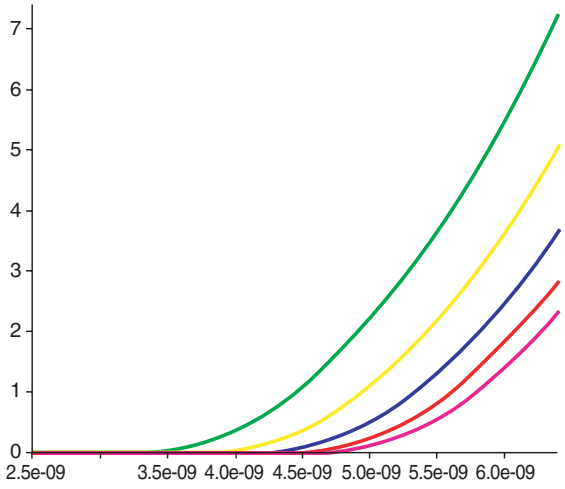

Figure 2. Current in each of the five segments

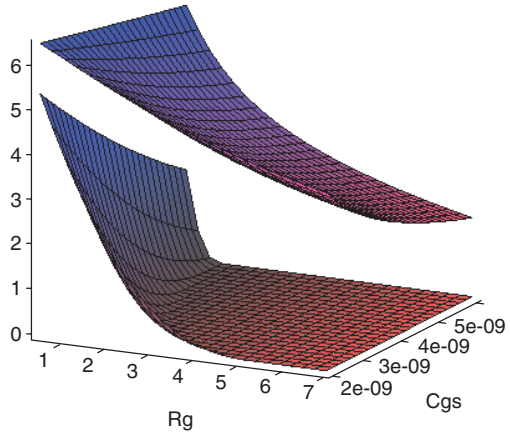

Figure 3. The first and last segment currents for different combinations of Rg and Cgs

The effect of Rg on the distribution of the switching current can be looked at in two ways:

1. Use the exact equations for a resistor-capacitor transmission line

2. Divide the die into several sections representing small enough areas on the die where all conditions are equal

The second approach is chosen since it gives a better idea of the mechanism in terms of die segments rather than the obscure distance along the die.

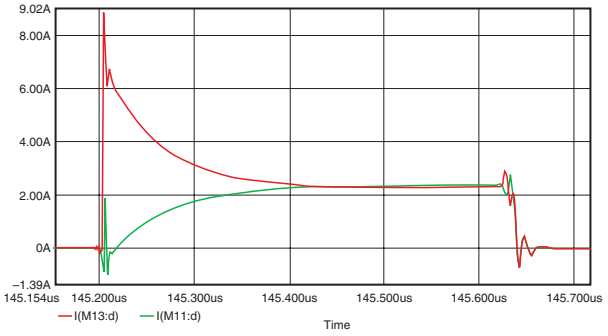

Figure 4. Switching current in the first (top, Red) and fifth (bottom green) segments

Figure 1 shows the simplified schematic used to formulate and solve the set of equations that describe the current in each segment. The equations were solved using Maple™ and the results are in Figures 2 & 3. Figure 2 depicts all the segment currents. A close examination reveals that the current is not distributed evenly among the different segments on the same die due to the propagation delay of gate drive signal along the die caused by the transmission line effects due to the distributed Rg and Cgs. This uneven distribution results in an uneven power loss at different sections of the die making the segments farthest away from the gate pad shoulder a much lower share of the switching current and switching losses as compared to the segment closest to the gate pad.

Figure 3 shows the current in the first (top curve) and the last segments as a function of both the gate ESR Rg and the gate-source capacitance Cgs midway along the switching cycle. This reveals that depending on Rg and Cgs values, the last segment starts conducting a smaller current at a much later time for moderately large values of Rg larger than 3 Ohm total in the example above but for small values of Rg say 0.5 Ohm the difference in current is much smaller and we would expect that at Rg=0 all the segment will carry identical currents. We do not recommend that MOSFETs be designed with Rg=0 since this is likely to cause a very serious ringing in the gate circuit causing much more trouble as compared to a moderate value of 0.3 – 0.7 Ohm since Rg dampens the oscillations of the gate inductance and the input capacitance of the MOSFET. With the proper layout for the gate and the gate drive circuit with minimum gate lead and PCB trace inductance we can achieve very little to no oscillations in the gate circuit as can be achieved with the BGA package from Fairchild Semiconductor.

Figure 4 depicts the circuit simulation results again showing that the first segment (red) carries most of the current during switching while the last segment (green) starts carrying current after the switching is complete.

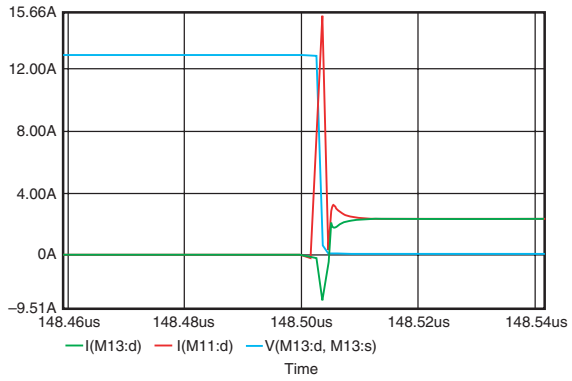

Figure 5. Drain-source voltage and first and last segment current waveform and the drain-source voltage

Figure 5 depicts the same segment currents as in Figure 4 with the drain-source voltage (blue) added to the traces. Again you can see that the switching losses mostly take place in the first segment while the last segment has a very little effect.

The Rg effect takes place only during turn on and off. During turn off, the segments that carried the largest current on turn on will turn off first while the segments that carried the smallest current will turn off last but Spice simulation results show that this effect is much less pronounced at turn off as compared to turn on. If every segment can conduct its own current without going over the maximum safe temperature of about 150°C–175°C there should be no problems but if Rg and the switching current is large enough where the losses are concentrated in a small area of the die; there exist the possibility that some segments may overheat leading to further excessive losses due to the positive temperature coefficient of the MOSFET RDS(ON) where RDS(ON) will get to be much larger which now leads to more conduction losses and hence even higher still temperature.

The gate driver source resistance does not play any part in this phenomenon since this particular effect is strictly an on die effect due to the distributed ESR and Cgs.

The effect of Rg on current rise and fall times

Let us start by examining the switching currents and voltages of the control or HS MOSFET in a synchronous buck converter. As can be observed in Figure 6, when the MOSFET is switched on at t0 the gate-source voltage rises steadily till it reaches Vgth. At this point the current will start commutating at t1 from the synchronous rectifier into the control MOSFET rising to the peak current at t2.

During the period t1–t2 the voltage across the control MOSFET will be approximately the input voltage plus one diode drop.

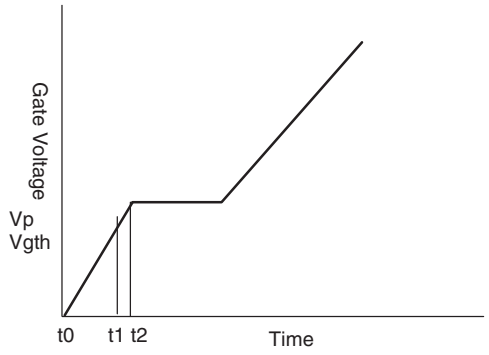

Figure 6. Gate-source voltage

The losses = $\frac{1}{2} \times Vin \times Id \times fs \times (tri + tfv)$ where,

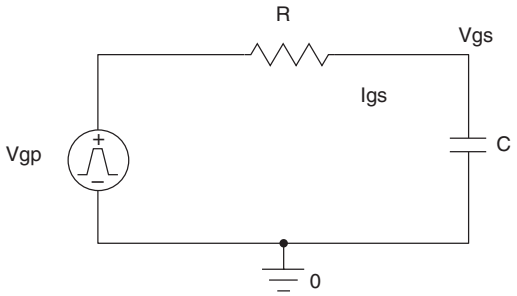

Figure 7 MOSFET input equivalent circuit with lumped Rg and Cgs

Vin is the input voltage, Id is the drain current, fs is the switching frequency and tri and tfv are the current rise time and voltage fall time. We will examine the effect of the lumped Rg on the value of tri and tfv.

The equation for a linear ramp of the gate drive voltage Vgp(t) is:

$$Vgp(t) := \frac{Vp\ t}{tr}$$

Where Vp is the peak value of the gate drive signal and t is time. The equation for the gate-source voltage, Vgs(t) node is:

$$e1 := Cgs\left(\frac{d}{dt}Vgs(t)\right) + \frac{Vgs(t) - \frac{Vp\ t}{tr}}{Rg} = 0$$

The equation for the gate drive node is:

$$e2 := Ig(t) + \frac{\frac{Vp\ t}{tr} - Vgs(t)}{Rg} = 0$$

Where Ig(t) is the current delivered by the gate driver. Using Maple™ to solve the two simultaneous differential equations we have the following solutions:

$$Vgs(t) = \frac{e^{\left(-\frac{t}{Cgs\ Rg}\right)} Vp\ Cgs\ Rg - Vp\ Cgs\ Rg + Vp\ t}{tr}$$

$$Ig(t) = \frac{e^{\left(-\frac{t}{Cgs\ Rg}\right)} Vp\ Cgs}{tr} - \frac{Vp\ Cgs}{tr}$$

Each of the two equations has different dependencies that are governed by the gate resistance with its two components of the MOSFET ESR and the gate driver source resistance as well as the gate-source capacitance Cgs and tr which is the rise time of the gate drive signal, MOSFET trance-conductance and drain current to name a few

$$Iload = (Vsegment - Vgth)^2 Gm$$

Where Iload is the load current in the segment and Vgth is the MOSFET gate threshold voltage. Substituting in the equation above and solving for the current rise time tri we get

$$tri := \left(LambertW\left(-e^{\left(-\frac{Vp\ Gm\ Cgs\ Rg + tr\ Gm\ Vgth + tr\sqrt{Gm\ Iload}}{Vp\ Gm\ Cgs\ Rg}\right)}\right)\right) Vp\ Gm\ Cgs\ Rg + tr\sqrt{Gm\ Iload}$$

$$-Gm\ LambertW\left(\left(-e^{\left(-\frac{Vp\ Cgs\ Rg + Vgth\ tr}{Vp\ Cgs\ Rg}\right)}\right) Vp\ Cgs\ Rg\right) / (Vp\ Gm)$$

Where Gm is the MOSFET transconductance while the rest of the variables are the same as above.

Figure 8 depicts the dependence of the current rise time (z axes) on Rg and Cgs. By examining Figure 8 we can observe that the current rise time is directly dependant on Rg and Cgs. One important comment here is that the tri values calculated in Figure 7 are done in an ideal package i.e., without any parasitic inductances.

By examining the tri equation it becomes very clear that the rise time is dependant on the product Rg × Cgs i.e. the smaller the product the lower the rise time and the lower the dynamic power losses.

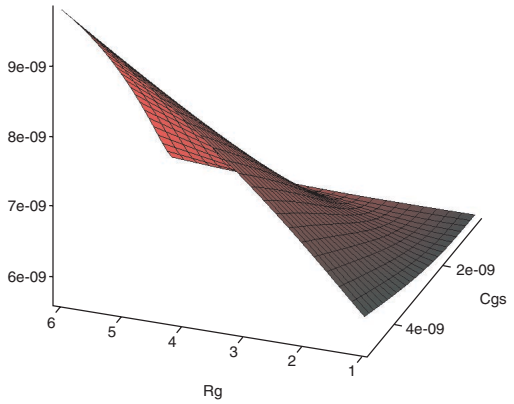

Figure 8. Effect of Rg and Cgs on Current Rise Time and a step gate drive voltage

Similar equations were derived for calculating the drain-source voltage fall time but they are too long to display here. Instead, we have Figure 9 depicts the dependency of the rise time (Z axes) on Cgd and Rg. Again you can clearly see that Rg has a direct linear influence on the drain-source voltage fall time in the range of values shown in Figure 9.

In general, the switching drain-source voltage rise and fall times are functions of MOSFET ESR Rg and gate-drain capacitance Cgd and the gate-source capacitance Cgs as well as the gate driver IC parameters of impedance and rise and fall times.

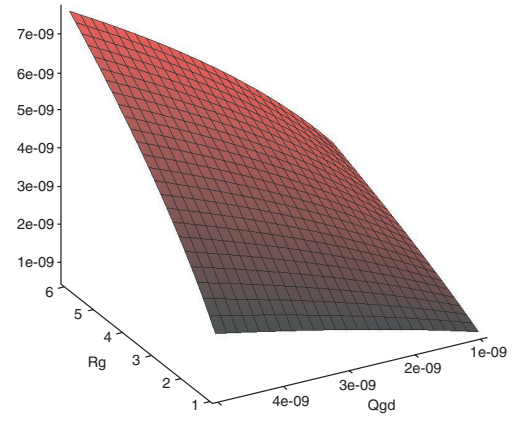

Figure 9. Effect of Rg on drain-source Voltage fall Time

1. The results of lab tests:

The practical lab results clearly show that larger ESR will result in larger current and voltage rise and fall times as can be seen in Figures 10 and 11. In this lab test we added a simple resistor between the gate driver and the gate of the MOSFET. This resistor can be considered an addition to the total gate resistance with its two parts 1- The intrinsic gate ESR resistance Rg 2- Gate driver source resistance and to these two we can add this external resistor. The results show that the addition of 4.7 Ohm will raise the current rise time from 6.56ns to 10.75ns an increase of almost 64% representing a 64% increase in the power loss during this transition.

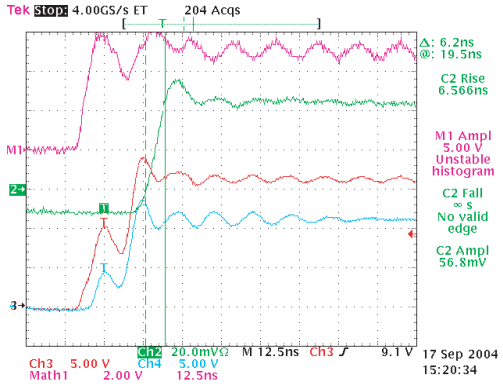

Figure 10 Rg = 0 Ohm, Current Rise time

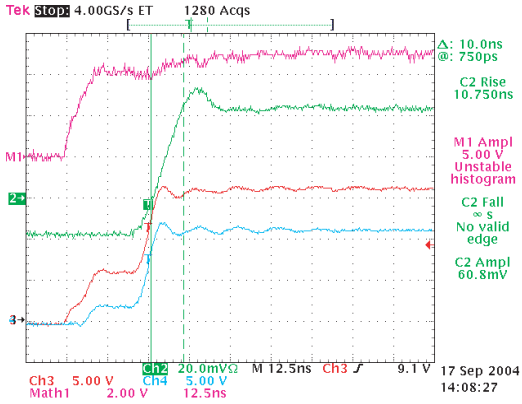

Figure 11 Rg = 4.7 Ohm, Current rise time

Conclusion

Controlling key parasitics in MOSFETs is pivotal to the power efficiency of the design and the overall performance of end applications. This application note demonstrates that both the MOSFET gate ESR and the MOSFET gate-source and gate-drain capacitances influence the switching losses and they all need to be optimized for optimal performance.

References

[1] Alan Elbanhawy, “Effect of Parasitic Inductance on switching performance” *in Proc. PCIM Europe 2003, pp.251–255*

[2] A. Elbanhawy, “Mathematical Treatment for HS MOSFET Turn-Off” *in Proc. PEDS Singapore 2003*

[3] A. Elbanhawy, “Pitfalls of MOSFET Paralleling” *in Proc. Power Electronics Technology 2003, pp. 98–106*

[4] J. Ejury, “Design Issues For DC/DC-Converters With Respect To Compact SMD MOSFET Packages” *in Proc. Power Electronics Conference USA 2004*

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative