



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

AN-7017

Reducing Power Losses in MOSFETs by Controlling Gate Parameters

Alan Elbanhawy, Fairchild Semiconductor

Introduction

The gate Equivalent Series Resistance (ESR) has been recognized as a factor affecting the losses in MOSFETs for a number of years. Controlling the losses is exceedingly important as devices need to produce the highest power conversion efficiency and lowest losses to operate efficiently at the target application. From an applications standpoint, an increase in losses can lead to overheating in the actual system requiring additional components such as heat sinks and fans. Additional components add to the overall cost and size of the end application. This application note explore ways to control these losses in MOSFETs.

What this application note will do:

- Provide guidance in selecting the right MOSFET for a specific application
- Optimize overall design by correct selection
- Explore the three distinct effects of gate ESR

The Effect of R_g on Switching Current Distribution

One of the first effects this application note will be explore is current distribution across the die during turn on and off. The gate ESR (R_g) together with the gate-source capacitance (C_{gs}) are distributed parameters across the MOSFET die.

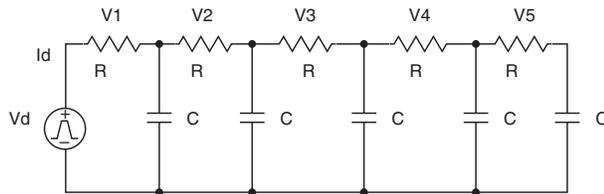


Figure 1. Simplified schematic for the solution of the current distribution

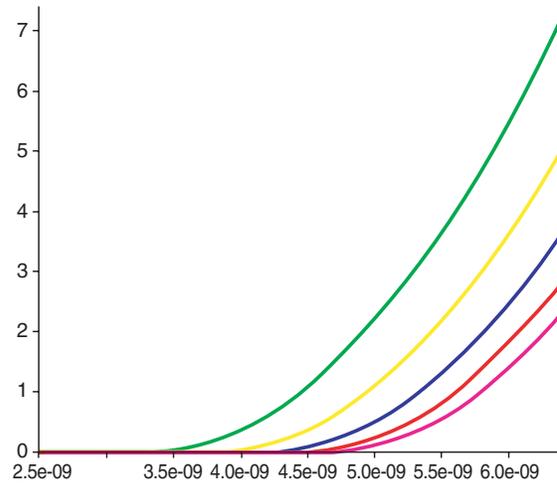


Figure 2. Current in each of the five segments

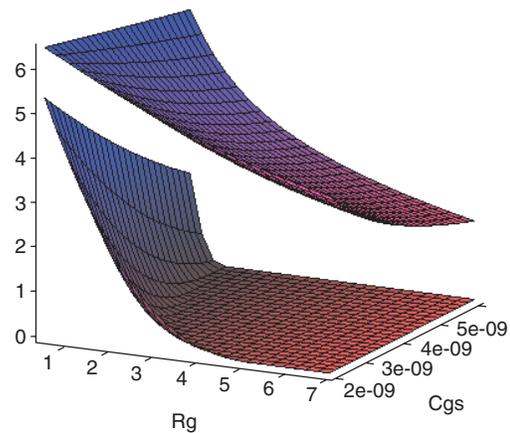


Figure 3. The first and last segment currents for different combinations of R_g and C_{gs}

The effect of R_g on the distribution of the switching current can be looked at in two ways:

1. Use the exact equations for a resistor-capacitor transmission line
2. Divide the die into several sections representing small enough areas on the die where all conditions are equal

The second approach is chosen since it gives a better idea of the mechanism in terms of die segments rather than the obscure distance along the die.

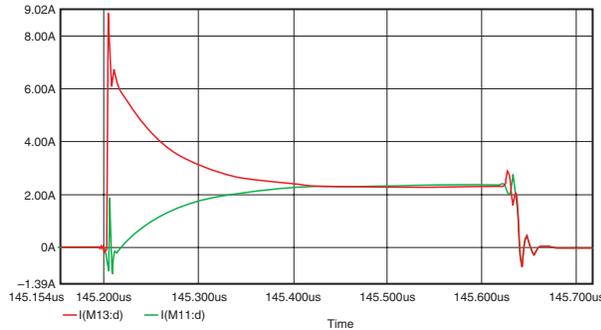


Figure 4. Switching current in the first (top, Red) and fifth (bottom green) segments

Figure 1 shows the simplified schematic used to formulate and solve the set of equations that describe the current in each segment. The equations were solved using Maple™ and the results are in Figures 2 & 3. Figure 2 depicts all the segment currents. A close examination reveals that the current is not distributed evenly among the different segments on the same die due to the propagation delay of gate drive signal along the die caused by the transmission line effects due to the distributed R_g and C_{gs} . This uneven distribution results in an uneven power loss at different sections of the die making the segments farthest away from the gate pad shoulder a much lower share of the switching current and switching losses as compared to the segment closest to the gate pad.

Figure 3 shows the current in the first (top curve) and the last segments as a function of both the gate ESR R_g and the gate-source capacitance C_{gs} midway along the switching cycle. This reveals that depending on R_g and C_{gs} values, the last segment starts conducting a smaller current at a much later time for moderately large values of R_g larger than 3 Ohm total in the example above but for small values of R_g say 0.5 Ohm the difference in current is much smaller and we would expect that at $R_g=0$ all the segment will carry identical currents. We do not recommend that MOSFETs be designed with $R_g=0$ since this is likely to cause a very serious ringing in the gate circuit causing much more trouble

as compared to a moderate value of 0.3 – 0.7 Ohm since R_g dampens the oscillations of the gate inductance and the input capacitance of the MOSFET. With the proper layout for the gate and the gate drive circuit with minimum gate lead and PCB trace inductance we can achieve very little to no oscillations in the gate circuit as can be achieved with the BGA package from Fairchild Semiconductor.

Figure 4 depicts the circuit simulation results again showing that the first segment (red) carries most of the current during switching while the last segment (green) starts carrying current after the switching is complete.

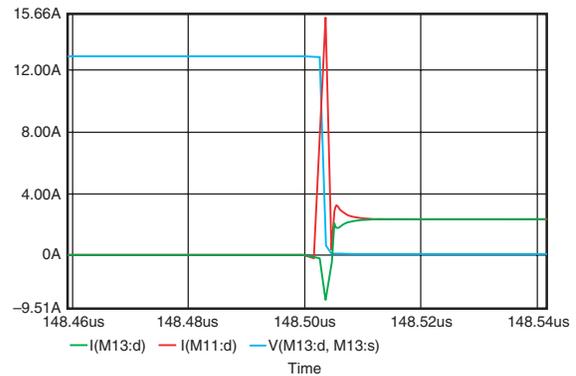


Figure 5. Drain-source voltage and first and last segment current waveform and the drain-source voltage

Figure 5 depicts the same segment currents as in Figure 4 with the drain-source voltage (blue) added to the traces. Again you can see that the switching losses mostly take place in the first segment while the last segment has a very little effect.

The R_g effect takes place only during turn on and off. During turn off, the segments that carried the largest current on turn on will turn off first while the segments that carried the smallest current will turn off last but Spice simulation results show that this effect is much less pronounced at turn off as compared to turn on. If every segment can conduct its own current without going over the maximum safe temperature of about 150°C–175°C there should be no problems but if R_g and the switching current is large enough where the losses are concentrated in a small area of the die; there exist the possibility that some segments may overheat leading to further excessive losses due to the positive temperature coefficient of the MOSFET $R_{DS(ON)}$ where $R_{DS(ON)}$ will get to be much larger which now leads to more conduction losses and hence even higher still temperature.

The gate driver source resistance does not play any part in this phenomenon since this particular effect is strictly an on die effect due to the distributed ESR and C_{gs} .

The effect of Rg on current rise and fall times

Let us start by examining the switching currents and voltages of the control or HS MOSFET in a synchronous buck converter. As can be observed in Figure 6, when the MOSFET is switched on at t0 the gate-source voltage rises steadily till it reaches Vgth. At this point the current will start commutating at t1 from the synchronous rectifier into the control MOSFET rising to the peak current at t2.

During the period t1–t2 the voltage across the control MOSFET will be approximately the input voltage plus one diode drop.

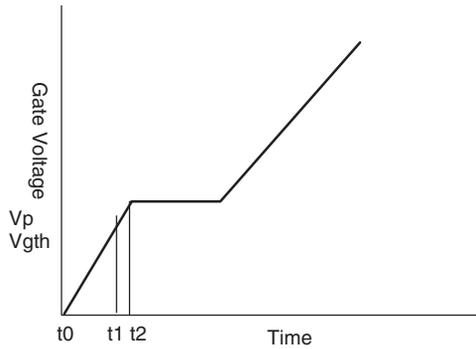


Figure 6. Gate-source voltage

The losses = $\frac{1}{2} \times V_{in} \times I_d \times f_s \times (t_{ri} + t_{fv})$ where,

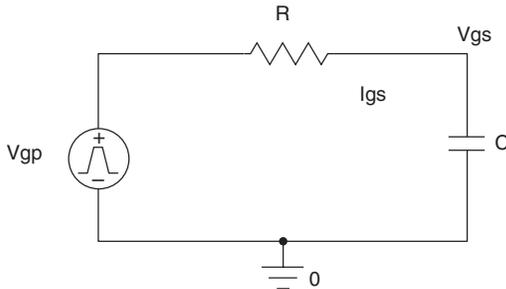


Figure 7 MOSFET input equivalent circuit with lumped Rg and Cgs

Vin is the input voltage, Id is the drain current, fs is the switching frequency and tri and tfv are the current rise time and voltage fall time. We will examine the effect of the lumped Rg on the value of tri and tfv.

The equation for a linear ramp of the gate drive voltage Vgp(t) is:

$$V_{gp}(t) := \frac{V_p t}{t_r}$$

Where Vp is the peak value of the gate drive signal and t is time. The equation for the gate-source voltage, Vgs(t) node is:

$$e1 := C_{gs} \left(\frac{d}{dt} V_{gs}(t) \right) + \frac{V_{gs}(t) - \frac{V_p t}{t_r}}{R_g} = 0$$

The equation for the gate drive node is:

$$e2 := I_g(t) + \frac{\frac{V_p t}{t_r} - V_{gs}(t)}{R_g} = 0$$

Where Ig(t) is the current delivered by the gate driver. Using Maple™ to solve the two simultaneous differential equations we have the following solutions:

$$V_{gs}(t) = \frac{e^{\left(-\frac{t}{C_{gs} R_g}\right)} V_p C_{gs} R_g - V_p C_{gs} R_g + V_p t}{t_r}$$

$$I_g(t) = \frac{e^{\left(-\frac{t}{C_{gs} R_g}\right)} V_p C_{gs} - V_p C_{gs}}{t_r}$$

Each of the two equations has different dependencies that are governed by the gate resistance with its two components of the MOSFET ESR and the gate driver source resistance as well as the gate-source capacitance Cgs and tr which is the rise time of the gate drive signal, MOSFET transconductance and drain current to name a few

$$I_{load} = (V_{segment} - V_{gth})^2 G_m$$

Where Iload is the load current in the segment and Vgth is the MOSFET gate threshold voltage. Substituting in the equation above and solving for the current rise time tri we get

$$t_{ri} := \left(\text{LambertW} \left(-e^{\left(-\frac{V_p G_m C_{gs} R_g + t_r G_m V_{gth} + t_r \sqrt{G_m I_{load}}}{V_p G_m C_{gs} R_g} \right)} \right) \right) \left(V_p G_m C_{gs} R_g + t_r \sqrt{G_m I_{load}} \right) - G_m \text{LambertW} \left(\left(-e^{\left(-\frac{V_p C_{gs} R_g + V_{gth} t_r}{V_p C_{gs} R_g} \right)} \right) V_p C_{gs} R_g \right) / (V_p G_m)$$

Where Gm is the MOSFET transconductance while the rest of the variables are the same as above.

Figure 8 depicts the dependence of the current rise time (z axes) on Rg and Cgs. By examining Figure 8 we can observe that the current rise time is directly dependant on Rg and Cgs. One important comment here is that the tri values calculated in Figure 7 are done in an ideal package i.e., without any parasitic inductances.

By examining the tri equation it becomes very clear that the rise time is dependant on the product $R_g \times C_{gs}$ i.e. the smaller the product the lower the rise time and the lower the dynamic power losses.

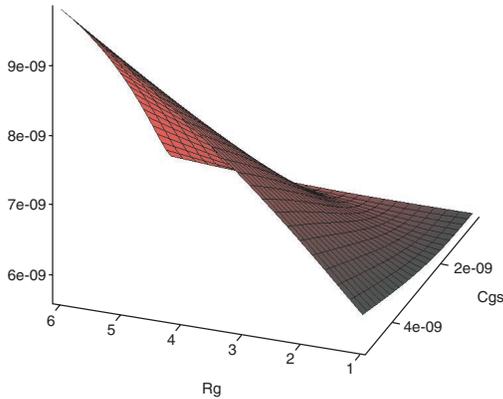


Figure 8. Effect of Rg and Cgs on Current Rise Time and a step gate drive voltage

Similar equations were derived for calculating the drain-source voltage fall time but they are too long to display here. Instead, we have Figure 9 depicts the dependency of the rise time (Z axes) on Cgd and Rg. Again you can clearly see that Rg has a direct linear influence on the drain-source voltage fall time in the range of values shown in Figure 9.

In general, the switching drain-source voltage rise and fall times are functions of MOSFET ESR Rg and gate-drain capacitance Cgd and the gate-source capacitance Cgs as well as the gate driver IC parameters of impedance and rise and fall times.

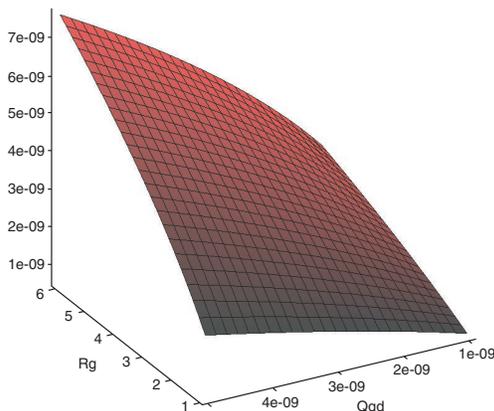


Figure 9. Effect of Rg on drain-source Voltage fall Time

1. The results of lab tests:

The practical lab results clearly show that larger ESR will result in larger current and voltage rise and fall times as can be seen in Figures 10 and 11. In this lab test we added a simple resistor between the gate driver and the gate of the MOSFET. This resistor can be considered an addition to the total gate resistance with its two parts 1- The intrinsic gate ESR resistance Rg 2- Gate driver source resistance and to these two we can add this external resistor. The results show that the addition of 4.7 Ohm will raise the current rise time from 6.56ns to 10.75ns an increase of almost 64% representing a 64% increase in the power loss during this transition.

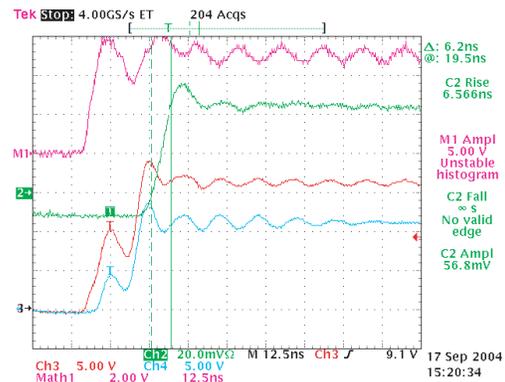


Figure 10 Rg = 0 Ohm, Current Rise time

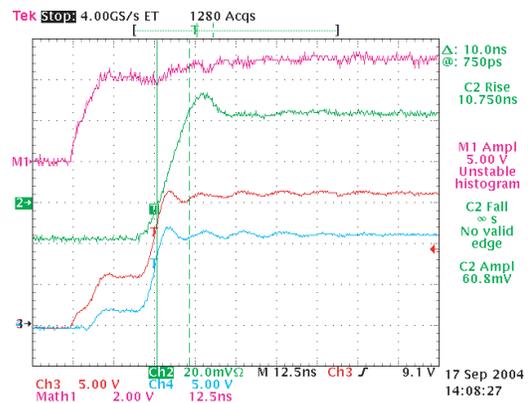


Figure 11 Rg = 4.7 Ohm, Current rise time

Conclusion

Controlling key parasitics in MOSFETs is pivotal to the power efficiency of the design and the overall performance of end applications. This application note demonstrates that both the MOSFET gate ESR and the MOSFET gate-source and gate-drain capacitances influence the switching losses and they all need to be optimized for optimal performance.

References

- [1] Alan Elbanhawy, "Effect of Parasitic Inductance on switching performance" in *Proc. PCIM Europe 2003*, pp.251–255
- [2] A. Elbanhawy, "Mathematical Treatment for HS MOSFET Turn-Off" in *Proc. PEDS Singapore 2003*
- [3] A. Elbanhawy, "Pitfalls of MOSFET Paralleling" in *Proc. Power Electronics Technology 2003*, pp. 98–106
- [4] J. Ejury, "Design Issues For DC/DC-Converters With Respect To Compact SMD MOSFET Packages" in *Proc. Power Electronics Conference USA 2004*

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative