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Improved IGBTs with Fast Switching Speed And High-Current Capability

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Abstract

Conventional vertical power MOSFETs are limited at high voltages (>500V) by the appreciable resistance of their epitaxial drain region. In a new MOS-gate controlled device called an IGBT, this limitation is overcome by modulating the conductivity of the resistive drain region, thereby reducing the on-resistance of the device by a factor of at least 10. However, the device previously described is slow in turnoff, having a fall time in the range 8 to 40μs. The purpose of our present work has been to reduce the fall time significantly and to increase the latching current level of the IGBTs, while retaining its desirable features. By modification of the epitaxial structure and addition of recombination centers, we have achieved fall times as low as 0.1μs and latching currents as high as 50A, while retaining on-resistance values <0.2Ω for a 0.09cm^2 chip area. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping. For a series of IGBTs (with forward-blocking voltage capabilities of 400-600V), the fall time can be reduced by more than one order of magnitude with a penalty of less than a 20 % increase in on-resistance.

Introduction

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. This limitation has been effectively overcome by the development of a new MOS power device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate. We have called this device a COMFET-an acronym for **CO**nductivity **M**odulated **F**ield **E**ffect **T**ransistor;[4] the device has also been called an IGBT or **I**nsulated **G**ate **B**ipolar **T**ransistor.

The devices, as originally described, had most of the advantages of conventional power MOSFETs; in addition, they exhibited more than an order-of-magnitude reduction in high current on-resistance values, permitting improved utilization of silicon chip area. However, they also had two disadvantages:

When a IGBT is turned off, the injected minority carriers that remain in the epitaxial drain region decay by recombination with majority carriers at a rate determined by the minority-carrier lifetime, τ_F. Large values of τ resulted in anode-current fall time, t_F, in the range 8-40ms. [4,5]

The maximum operating current is limited by latchup of the parasitic thyristor that is inherent in the device structure. Typical latching current levels of I_L, ≤ 10A were observed in 0.09cm^2 area devices when the gate voltage was turned off rapidly (<1ms); for slower gate voltage turnoff (~10ms), I_L values as high as ~30A were observed.

The purpose of the present work has been to reduce t_F and to increase I_L while retaining the desirable features of the device. By modifying the epitaxial structure and adding recombination centers to the epitaxial drain region, we have achieved t_F values as low as 100ns and I_L values as high as 50A with rapid gate voltage turnoff.

Modified Structure

A schematic diagram of the original IGBT structure[4] is shown in Figure 1(a), and the equivalent circuit is shown in Figure 1(b); they are similar to those of an MOS-gated thyristor except for the presence of the shunting resistance Rs in each unit cell. The fabrication is like that of a standard n-channel power MOSFET, except that the n-epitaxial layer is grown on a p+ substrate instead of an n+ substrate. The heavily doped p+ region in the center of each unit cell, combined with the aluminum contact shorting the n+ and p+ regions, provides the shunting resistance RS. This has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit so that αnpn + αpnp <1, thereby preventing latching over a large operating range of anode voltage V_A and anode current i_A. However, for sufficiently large i_A, emitter injection in the n-p-n transistor will increase, accompanied by an increase in αnpn. When αnpn + αpnp increases to 1, the four-layer device will latch; the level of i_A at which this occurs is the latching current level, I_L. Thus, it can be seen that a structure modification that lowers αpnp will allow a greater range of i_A (and αnpn) without latching; that is, a reduction in αpnp corresponds to an increase in I_L.

The modified structure shown in Figure 1(C) differs from that in Figure 1(A) by the addition of a thin (~10mm) layer of n+ silicon in the epitaxial structure between the n- region and the p+ substrate. This n+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in I_L by a factor of 2 to 3. In addition, there is also a reduction in t_F.

These results are illustrated in Figure 2, in which t_F, is plotted versus i_A for each device structure. It should be noted that IGBTs with the modified structure can block high voltage only in the forward voltage direction since the emitter junction (p+ - n+) of the p-n-p transistor breaks down at a low level when the polarity of the applied voltage is reversed.

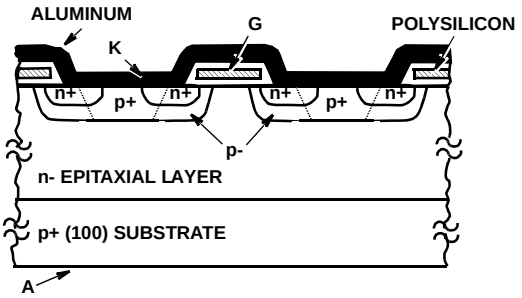


FIGURE 1A. SCHEMATIC DIAGRAM OF ORIGINAL IGBTs STRUCTURE

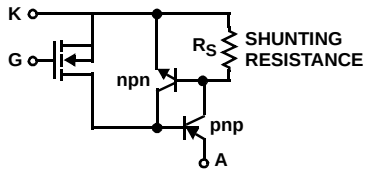


FIGURE 1B. EQUIVALENT CIRCUIT

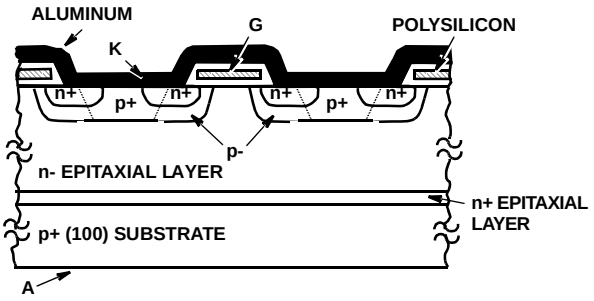


FIGURE 1C. SCHEMATIC DIAGRAM OF MODIFIED STRUCTURE

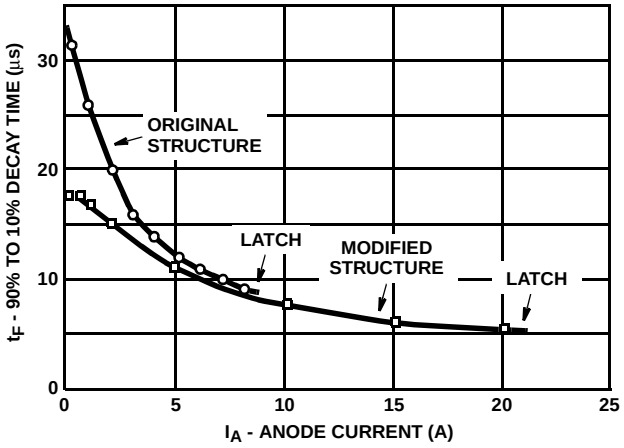


FIGURE 2. ANODE-CURRENT FALL TIME t_F VERSES ANODE CURRENT FOR ORIGINAL STRUCTURE AND MODIFIED STRUCTURE

Addition Of Recombination Centers

We have used a variety of techniques to add recombination centers to IGBTs; these include high energy electron, gamma ray, and fast neutron irradiation, as well as heavy metal doping. The irradiations were carried out after completion of all of the high-temperature processing steps, but in each case an additional heat treatment was necessary to stabilize the devices by annealing out gate oxide charge, as well as those radiation induced defects in the s ilicon (recombination centers) that would otherwise anneal out slowly at the device operating temperature.[7] Typical values of t_F of the order of 1µs or less were achievable using any of the techniques.

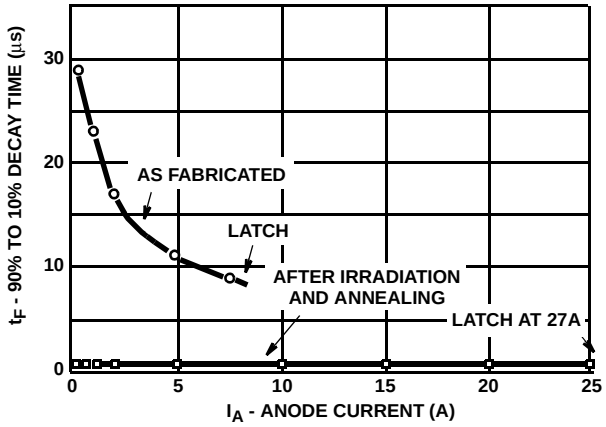
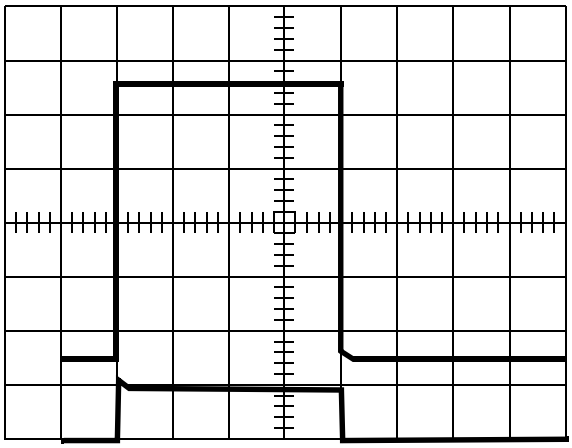
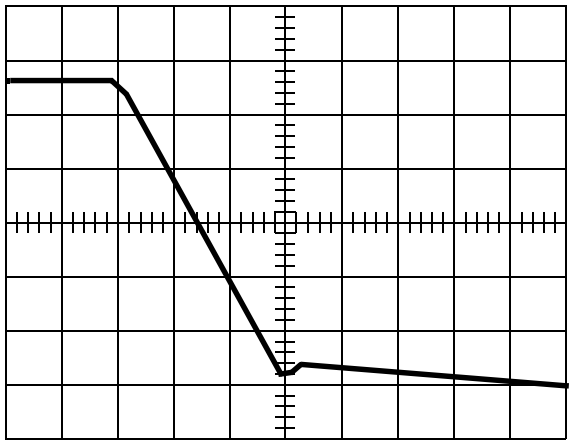


FIGURE 3. ANODE-CURRENT FALL TIME t_F VERSUS ANODE CURRENT FOR AN AS-FABRICATED DEVICE AND AFTER 14MeV NEUTRON IRRADIATION (10^{13}n/cm^2) FOLLOWED BY ANNEALING AT +300^{o}C.

An example of the variation of tF , with iA (1) as fabricated and (2) after irradiation with 14MeV neutrons and annealing is shown in Figure 3. Here, the neutron fluence was ~10^{13}n/cm^2; this was followed by annealing at +300^{o}C. Note that t_F, has not only been drastically reduced, but is virtually constant at ~0.6µs; i.e., almost independent of i_A.



TOP: ANODE CURRENT, 5A/DIV
BOTTOM: GATE VOLTAGE, 20V/DIV
5μs/DIV



ANODE CURRENT ON
EXPANDED TIME SCALE
5A/DIV
100ns/DIV
t_{FALL} ~ 160ns

FIGURE 4. IGBTs ANODE CURRENT AND GATE VOLTAGE WAVEFORMS

It is possible to lower t_F, still further by appropriate irradiation and annealing or by heavy metal doping procedures, although this is not necessarily desirable for reasons that are discussed below. The smallest values of t_F, that we have obtained for fully stabilized IGBTs is in the range 100ns to 200ns. This is illustrated in Figure 4.

The reduction in minority carrier lifetime that allows faster switching also carries with it a penalty higher forward voltage drop when the device is turned on; i.e., higher on-resistance. Since, in the forward conduction of an IGBT, current and voltage are not linearly related, it is necessary to specify a current level at which to compare on-resistance values of different devices. In Figure 5 we plot the on-resistance (at i_A = 20A) of a series of devices with 0.09cm^2 chip area against their t_F, values after irradiation and annealing. All t_F, values shown were obtained at i_A = 5A; for the devices with short switching times, t_F, is virtually independent of i_A. Clearly, there is a trade-off involved, and the optimum choice of a value for t_F, and the corresponding on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100ns), the on-resistance value of 0.2Ω is approximately an order-of-magnitude less than that of comparably sized n-channel MOSFETs.

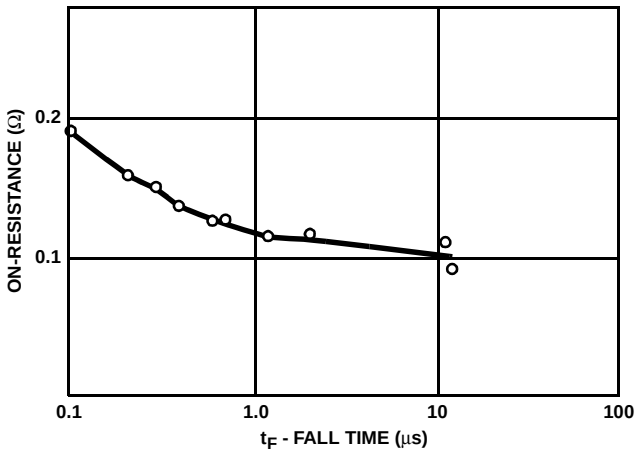


FIGURE 5. ON-RESISTANCE vs. ANODE-CURRENT FALL TIME t_F FOR A SERIES OF IGBTs AFTER VARIOUS IRRADIATION AND ANNEALING TREATMENTS

Temperature Dependence of T_F, and I_L

All of the device performance data presented thus far have been measured at room temperature. However, power devices are often operated at elevated temperatures, and it is important to determine how their performance varies with temperature. In Figure 6 the variation of t_F and I_L for a device that has been irradiated and annealed is plotted versus temperature in the range +25°C to +150°C. This behavior is typical of all of the devices we have tested; i.e., t_F increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval +25 °C to +150°C.

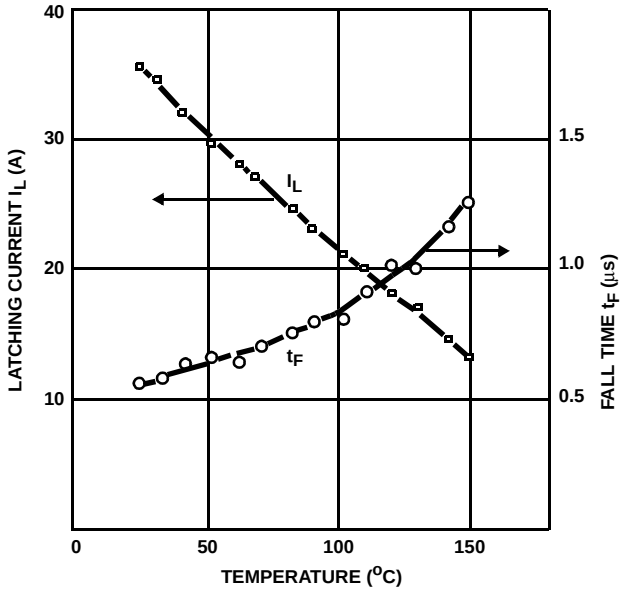


FIGURE 6. VARIATION OF ANODE-CURRENT FALL TIME t_F AND LATCHING CURRENT I_L WITH TEMPERATURE

Summary

By modification of the epitaxial structure of the IGBT and the addition of recombination centers, we have achieved anode-current fall times as low as 100ns in IGBTs with latching currents as high as 50A for a 0.09cm^2 chip area. We have described the trade-off between on-resistance and anode-current fall time that may be obtained, and have demonstrated the variation of anode-current fall time and latching current with operating temperature.

Acknowledgment

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