# Design Considerations for Asymmetric Half-Bridge Converters

Hangseok Choi

**Abstract** — Among various kinds of soft-switching converters, asymmetric PWM half-bridge converters have drawn attention due to their simplicity, inherent zero voltage switching (ZVS) capability, and fixed-frequency operation. This paper presents an analysis and reviews practical design considerations for an asymmetric half-bridge converter. It includes designing the transformer and selecting components. A step-by-step design procedure with a design example will help engineers design an asymmetric half-bridge converter.

## I. INTRODUCTION

The effort to obtain ever-increasing power density of switched-mode power supplies has been limited by the size of passive components. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters; however, switching losses have hindered high-frequency operation. To reduce switching losses and allow high-frequency operation, resonant switching and soft-switching techniques have been developed [1-5].

The resonant switching method processes power in a sinusoidal manner by utilizing the resonance during the entire switching period. Generally, the output voltage is regulated by variable frequency control and the current or voltage waveform in the resonant network has a sinusoidal shape.

Meanwhile, soft-switching techniques utilize the resonance operation only during the switching transition to soften the switching characteristics of the devices. When the switching transition is over, the converter reverts to Pulse-Width-Modulation (PWM) mode. Since resonant operation only occurs during the switching transition, the parameters of resonant components are not as critical as in a resonant converter. Moreover, the switching frequency is fixed and easily synchronized to the other power stages to minimize EMI.

Among various kinds of soft-switching converters, the asymmetric PWM half-bridge converter has drawn attention due to its simplicity and inherent zero voltage switching (ZVS) capability. Figure 1 and 2 show the basic circuit and typical operation waveforms of the asymmetric PWM half-bridge converter. This converter has several advantages over other soft-switching topologies: low MOSFET voltage and current stress, small output capacitor and inductor, minimum component count, and simple control.

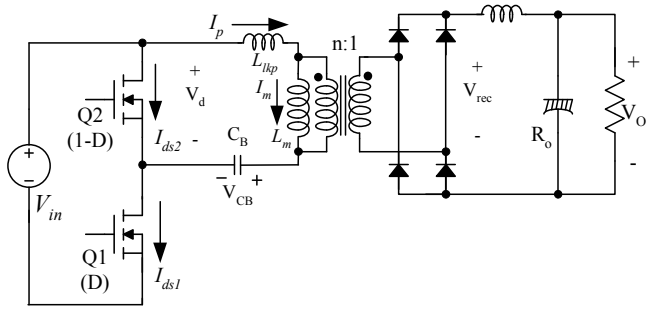



**Fig.1. Asymmetric PWM half-bridge converter.**

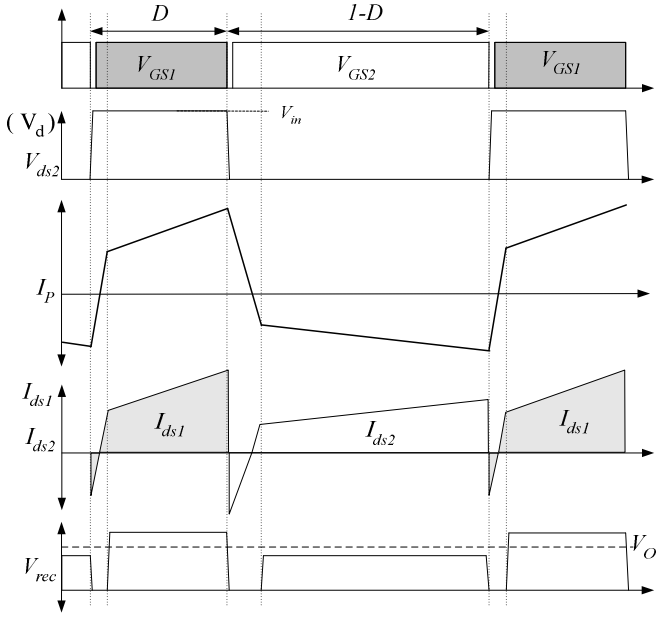



**Fig.2. Typical waveforms of an asymmetric PWM half-bridge converter.**

This paper presents design considerations of an asymmetric PWM half-bridge converter. It includes designing the transformer and selecting the components. The step-by-step design procedure explained with a design example will help engineers design an asymmetric PWM half-bridge converter.

## II. IDEALIZED OPERATION PRINCIPLE OF ASYMMETRIC PWM HALF-BRIDGE CONVERTER

Figure 3 illustrates the simplified circuit diagram of an asymmetric PWM half-bridge converter and its ideal waveforms, where the leakage inductance of the transformer is ignored. The DC blocking capacitor ($C_B$) acts not only as an energy source feeding the load while the upper switch ($Q_2$) is conducting, but also as a blocking capacitor to prevent transformer saturation.

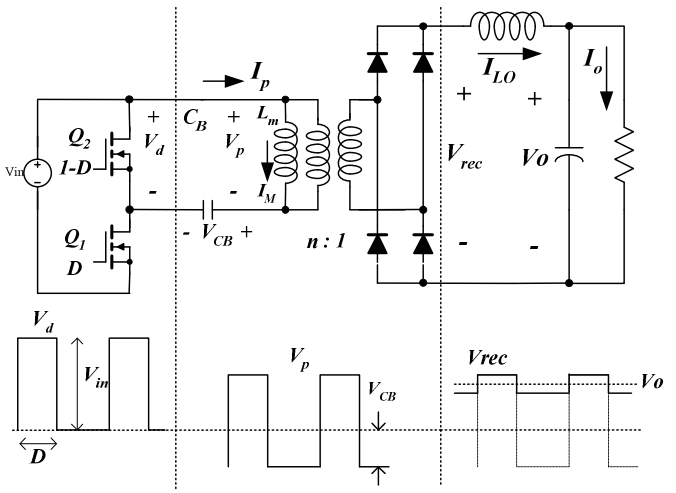



**Fig. 3. Simplified circuit diagram of an asymmetric PWM half-bridge converter and its waveforms.**

Applying a voltage-second balance equation across the transformer primary side as:

$$(V_{in} - V_{CB}) \cdot D = V_{CB} \cdot (1 - D) \tag{1}$$

The voltage across $C_B$ is obtained by:

$$V_{CB} = V_{in} \cdot D \tag{2}$$

where $D$ is the duty cycle ratio of low-side MOSFET ($Q_1$).

Idealized output voltage is obtained by averaging the secondary-side rectifier voltage ($V_{rec}$) as:

$$V_o = \frac{(V_{in} - V_{CB})}{n} \cdot D + \frac{V_{CB}}{n} \cdot (1 - D) \tag{3}$$

where $n$ is the transformer turns ratio ($N_p/N_s$).

Substituting Equations 2 into 3, the idealized output voltage in Equation 3 is simplified as:

$$V_o = \frac{V_{in} \cdot 2(1 - D) \cdot D}{n} \tag{4}$$

Figure 4 shows the normalized gain using Equation 4. The operation shows symmetry for the two operation ranges of D from 0% to 50% and from 50% to 100%. Since the slope of the gain curve is reversed at 50% duty cycle, duty cycle should be either below or above 50% for output voltage regulation. In general, operation range from 0% to 50% is preferred since the conventional PWM controller can be used as it is. Meanwhile, operation range above a 50% duty cycle requires additional circuitry to a conventional PWM controller due to the reversed control polarity.

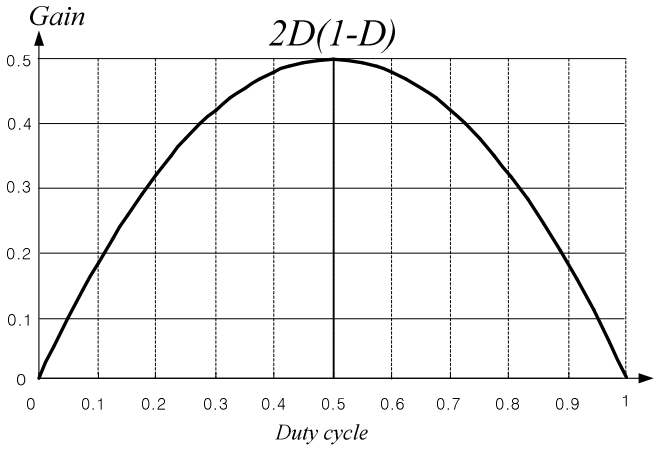



**Fig. 4. Normalized voltage gain when ignoring the duty cycle losses caused by leakage inductance.**

Figure 5 shows simplified primary-side current waveforms. The transformer primary-side current ($I_p$) is the sum of the output inductor current referred to as the primary side ($I_{LO}/n$) and the magnetizing current ($I_M$).

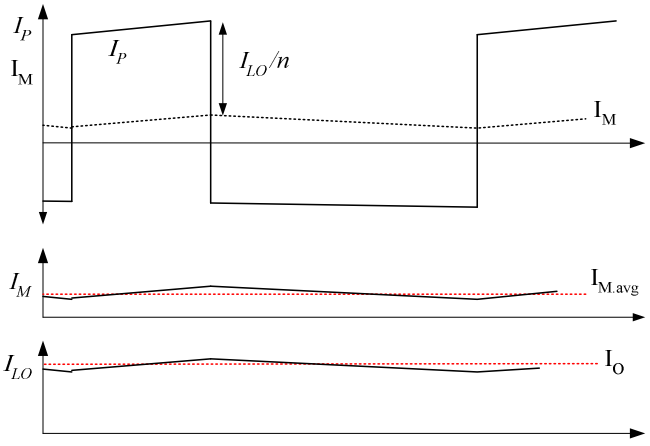



**Fig. 5. Primary-side current waveforms.**

In steady-state operation, the magnetizing current is automatically adjusted so that the average charging current of $C_B$ over one cycle is zero. The mean value of the transformer magnetizing current, $I_{M.avg}$, is obtained from the condition for zero net current through the DC blocking capacitor ($C_B$):

$$(I_{M.avg}+\frac{I_O}{n})D=(-I_{M.avg}+\frac{I_O}{n})(1-D) \quad (5)$$

$$I_{M.avg}=(1-2D)\cdot\frac{I_O}{n} \quad (6)$$

where $I_o$ is the output load current.

As observed, the mean value of the transformer magnetizing current is zero when duty cycles for the MOSFETs are even (50% and 50%). Meanwhile, the mean value of the magnetizing current increases as the duty cycle moves away from 50%, which should be the worst case for transformer design. In other words, minimum and maximum duty cycles are the worst cases for operation range below 50% duty cycle and above 50% duty cycle, respectively.

## III. Steady-State Analysis of Actual Asymmetric PWM Half-Bridge Converter

Figure 6 shows the schematic of an asymmetric PWM half-bridge converter and Figure 7 shows its typical waveforms. In Figure 6, $L_m$ and $L_{lk}$ are the magnetizing inductance and effective leakage inductance in the transformer primary side, respectively, and $C_B$ is the DC blocking capacitor whose voltage is almost constant during one switching cycle.

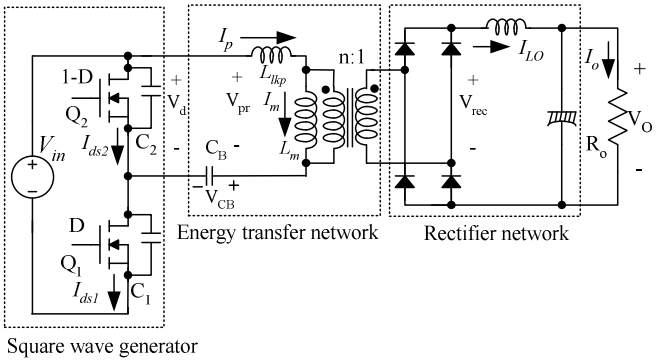



**Fig. 6. Schematic of an asymmetric PWM half-bridge converter.**

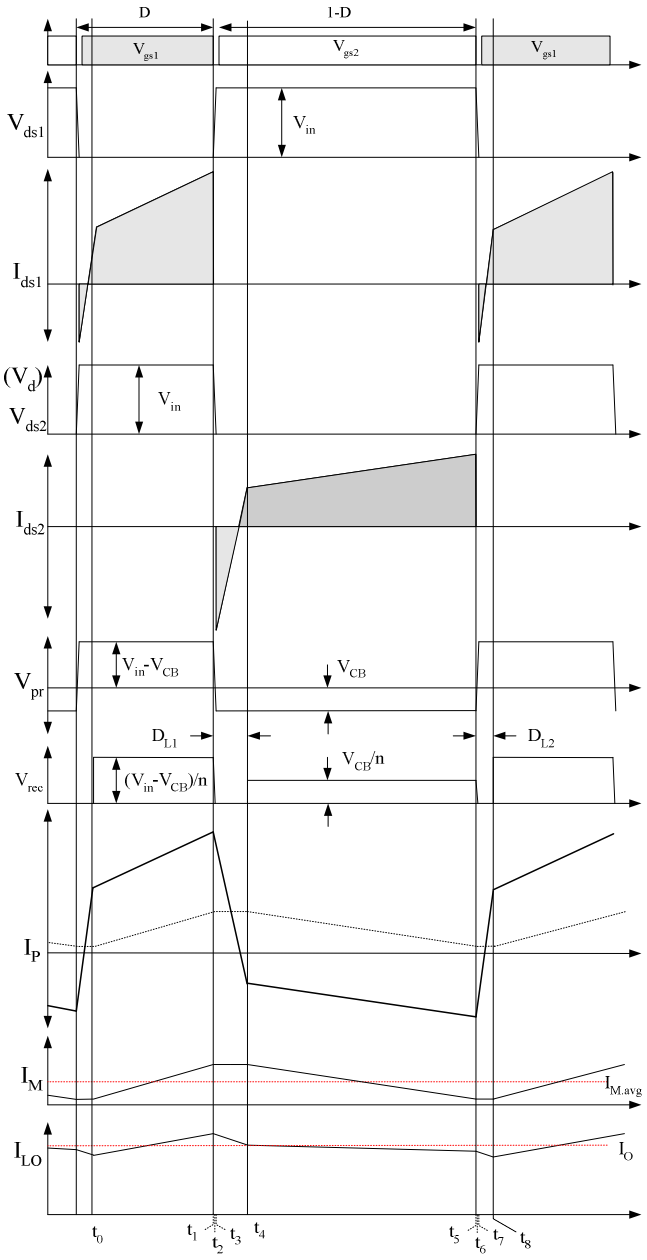



**Fig. 7. Typical waveforms of an asymmetric PWM half-bridge converter.**

In general, the asymmetric PWM half-bridge converter consists of three stages, as shown in Figure 6: a square wave generator, energy transfer network, and rectifier network.

- The square wave generator produces a square wave voltage ($V_d$) by driving switches Q1 and Q2 complementarily. In order words, the lower and upper MOSFETs duty cycles should be D and 1-D, respectively. A small dead time is usually introduced between the consecutive transitions.
- The energy transfer network consists of a DC blocking capacitor and transformer. The energy transfer network removes the DC offset of the

square wave voltage ($V_d$) using the DC blocking capacitor ($C_B$), then transfers the pure AC square wave voltage to the secondary side through the transformer. The transformer primary-side current, $I_p$, lags the voltage applied to the transformer primary side due to the leakage inductance, which allows the MOSFETs to be turned on with zero voltage. As seen in Figure 7, after one of the switches has been turned off, $I_p$ charges (or discharges) the MOSFET output capacitances and eventually swings the switch voltages from one input rail to the other (from $V_{in}$ to ground or from ground to $V_{in}$). Then, $I_p$ continues to flow through the anti-parallel body diode. As long as the body diode conducts, the corresponding MOSFET can be turned on with zero voltage.

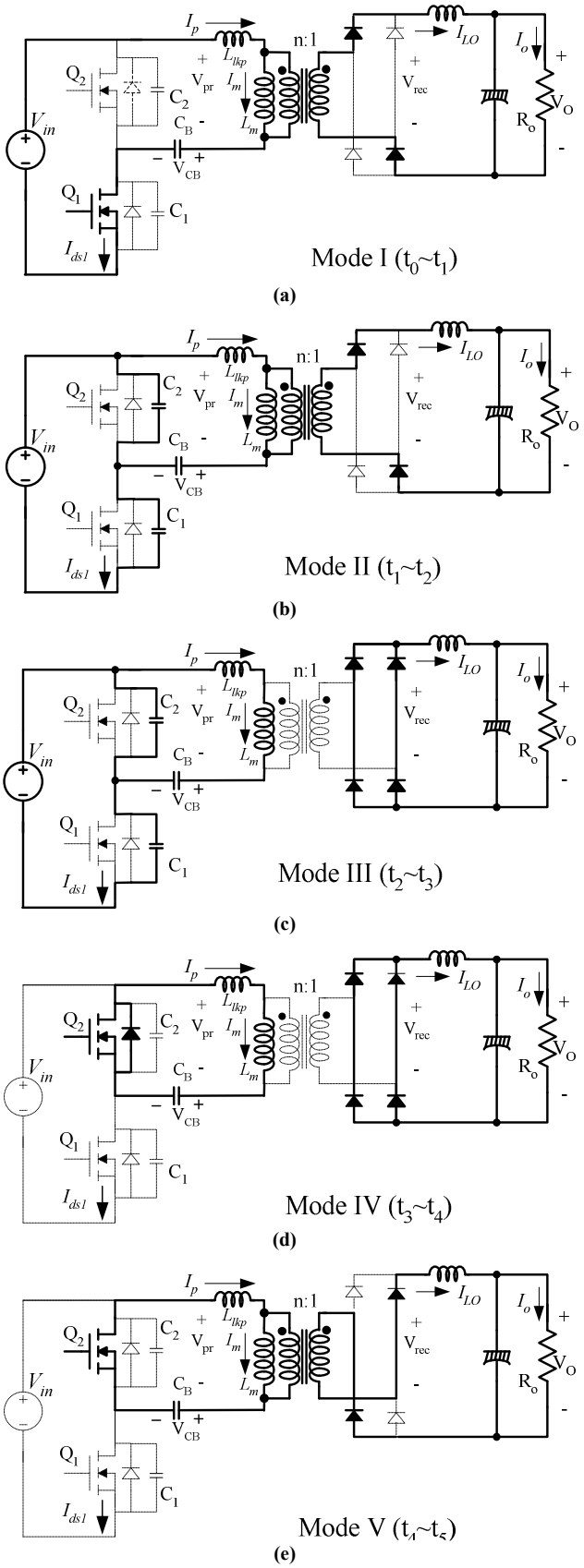
- The rectifier network produces a DC voltage by rectifying the AC voltage with rectifier diodes and a low-pass LC filter. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration.

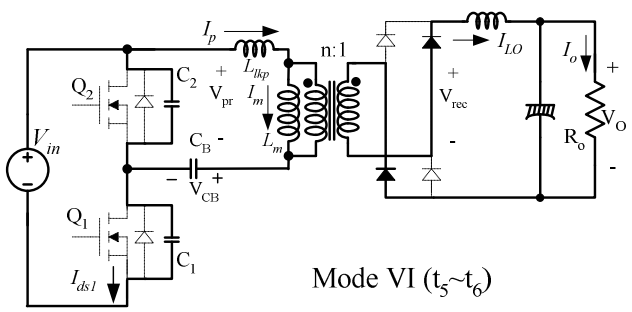
In steady-state analysis, the following assumptions are made:

- The dead time is negligible since it is very small compared to the switching cycle.
- The leakage inductance is much smaller than the magnetizing inductance.
- The DC blocking capacitor, $C_B$, is large enough to neglect the voltage ripple across $C_B$.
- The output filter inductor operates in continuous conduction mode.
- All circuit elements are ideal and lossless.
- The duty cycle for lower MOSFET, D, is limited below 50%.
- The capacitors $C_1$ and $C_2$ include not only the internal output capacitance of MOSFETs, but also the external parasitic capacitances.

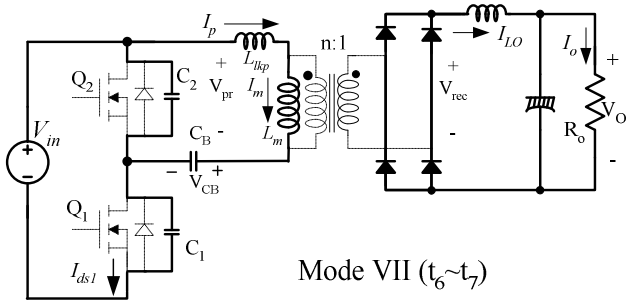
### *A. Operation Mode Analysis*

The asymmetric half-bridge converter has eight operation modes during one switching cycle. The equivalent circuit of each mode is illustrated in Figure 8.






(f)

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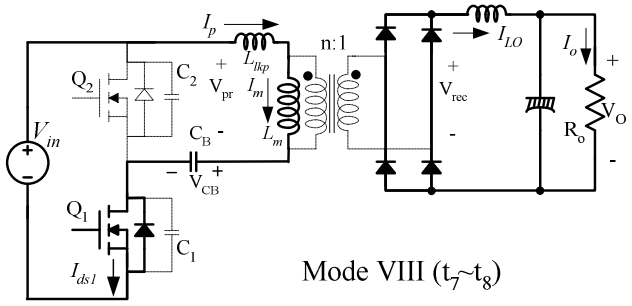


(h)

**Fig. 8. Operation modes of an asymmetric PWM half-bridge converter.**

**Mode I ($t_0$~$t_1$)**: The lower switch ($Q_1$) is conducting and a voltage of ($V_{in}$-$V_{CB}$) is applied to the transformer primary side ($V_{pr}$). The transformer primary-side current ($I_p$) is the sum of the output inductor current referred to as the primary side ($I_{LO}$/n) and the magnetizing current ($I_M$). This mode is similar to the power transferring mode of a conventional half-bridge converter.

**Mode II ($t_1$~$t_2$):** The lower switch ($Q_1$) is turned off at $t_1$ and the primary side current, $I_p$, charges $C_1$ and discharges $C_2$. This mode continues until the primary-side voltage drops to zero (until $C_2$ is discharged to $V_{CB}$) at $t_2$. Since the secondary side is connected to the primary side, $C_2$ is discharged using the energy stored in the leakage inductance and output inductor.

**Mode III ($t_2$~$t_3$):** At $t_2$, the transformer primary-side and secondary-side voltages become zero and the secondary side is decoupled from the primary side. Then, the output inductor current, $I_{LO}$, begins to freewheel in the secondary side through the rectifiers while $C_2$ continues to be discharged. Since the secondary-side inductor ($L_o$) is disconnected from the primary side, $C_2$ is discharged using the energy stored in the leakage inductance only. After $C_2$ is fully discharged, the body diode of $Q_2$ begins conducting before $t_3$.

**Mode IV ($t_3$~$t_4$):** The body diode of $Q_2$ is conducting and the voltage across the switch $Q_2$ is clamped at zero. By turning on $Q_2$ while the body diode is conducting, zero voltage switching (ZVS) is achieved. During this mode, a voltage of $-V_{CB}$ is applied across the leakage inductance and the primary-side current ($I_p$) decreases. This mode continues until $I_p$, plus the magnetizing current ($I_M$), becomes $-I_{LO}/n$. During this mode, the transformer secondary-side voltage remains zero, which causes duty cycle losses of as much as:

$$D_{L1} = \frac{t_4 - t_3}{T_s} = \frac{2I_o L_{lk}}{T_S \cdot n \cdot V_{in} \cdot D} \tag{7}$$

where $T_s$ is the switching period.

**Mode V ($t_4$~$t_5$):** The upper switch ($Q_2$) is conducting and $-V_{CB}$ is applied to the transformer primary side ($V_{pr}$). The transformer primary-side current ($I_p$) is the sum of the output inductor current referred to as the primary side ($-I_{LO}/n$) and the magnetizing current ($I_M$). This mode is similar to the power transferring mode of a conventional half-bridge converter.

**Mode VI ($t_5$~$t_6$):** The upper switch ($Q_2$) is turned off at $t_5$ and the primary-side current $I_p$ charges $C_2$ and discharges $C_1$. This mode continues until the primary-side voltage becomes zero (until $C_1$ is discharged to $V_{in}$-$V_{CB}$) at $t_6$. Since the secondary-side inductor ($L_o$) is connected to the primary side, $C_1$ is discharged using the energy stored in the leakage inductance and output inductor.

**Mode VII ($t_6$~$t_7$):** At $t_6$, the transformer primary-side and secondary-side voltages become zero and the secondary side is decoupled from the primary side. Then, the output inductor current, $I_{LO}$, begins to freewheel in the secondary side and $C_1$ continues to be discharged. Since the secondary side is disconnected from the primary side, $C_1$ is discharged using the energy stored in the leakage

inductance only. After $C_1$ is fully discharged, the body diode of $Q_1$ begins conducting before $t_7$.

**Mode VIII ($t_7$~$t_8$):** The body diode of $Q_1$ is conducting and the voltage across the switch $Q_1$ is clamped at zero voltage. By turning on $Q_1$ while the body diode is conducting, zero voltage switching (ZVS) is achieved. During this mode, a voltage of ($V_{in}$-$V_{CB}$) is applied across the leakage inductance and the primary side current ($I_p$) increases. This mode continues until $I_p$ minus the magnetizing current becomes $I_{LO}$ /n. During this mode, the transformer secondary side voltage remains zero, which causes duty cycle losses of as much as

$$D_{L2} = \frac{t_8 - t_7}{T_s} = \frac{2I_o L_{lk}}{T_S \cdot n \cdot V_{in} \cdot (1-D)} \tag{8}$$

### *B. Zero-Voltage Switching Condition*

As discussed in the explanation of operation mode, after $Q_1$ is turned off at $t_1$, $C_2$ is discharged from $V_{in}$ to $V_{CB}$ by the energy stored in the leakage inductance and output inductor. Then $C_2$ is fully discharged by the energy stored in the leakage inductance only. Therefore, the ZVS condition for switch $Q_2$ is given as:

$$L_{lk}[I_p(t_2)]^2 > (C_1 + C_2)[DV_{in}]^2 \tag{9}$$

where $L_{lk}$ is the effective leakage inductance in the transformer primary side and $I_p(t_2)$ is the primary side current at $t_2$, given as:

$$I_p(t_2) = \frac{I_o}{n} + I_{M.avg} + \frac{V_{in}(1-D)DT_S}{2L_m} \tag{10}$$

After $Q_2$ is turned off at $t_5$, $C_1$ is discharged from $V_{IN}$ to $V_{IN}$-$V_{CB}$ by the energy stored in the leakage inductance and output inductor. Then $C_1$ is fully discharged by the energy stored in the leakage inductance only. Therefore, the ZVS condition for switch $Q_1$ is given as:

$$L_{lk}[I_p(t_6)]^2 > (C_1 + C_2)[(1-D)V_{in}]^2 \tag{11}$$

where $I_p(t_6)$ is the primary-side current at $t_6$, given as:

$$I_p(t_6) = -\frac{I_o}{n} + I_{M.avg} - \frac{V_{in}(1-D)DT_S}{2L_m} \tag{12}$$

Since $I_p(t_2)$ is always larger than $|I_p(t_6)|$ and $DV_{in}$ is always smaller than $(1\text{-}D)V_{in}$ for duty cycles smaller than 50%, the ZVS condition of Equation 9 is satisfied more easily than that of Equation 11. Thus, the condition given by Equation 11 should be satisfied to achieve ZVS for both MOSFETs. It is required to increase the leakage inductance ($L_{lk}$) or increase the value of $|I_p(t_6)|$ to guarantee ZVS for both switches over wide load range. Too large a leakage inductance increases the voltage overshoot and ringing in the rectifier diodes, which results in using higher voltage rated rectifiers and power dissipation in the snubber circuit to clamp the voltage overshoot. Another way to guarantee ZVS over a wide load range is to increase the value of $|I_p(t_6)|$ by reducing the magnetizing inductance. Even though this method increases conduction losses on the primary side, it is more effective than increasing the leakage inductance for high input voltage applications where the conduction losses in the primary side are negligible.

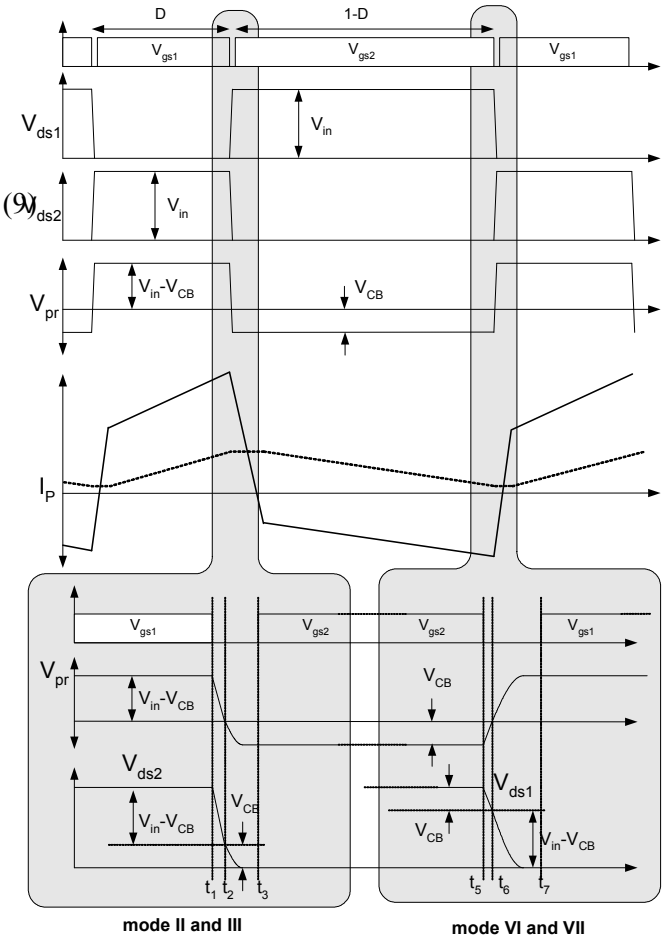


**Fig. 9. Detailed waveforms during the switching transient.**

### *C. DC Characteristics Considering Duty Cycle Losses*

In the input to output voltage relationship of Equation 4, the duty cycle losses caused by leakage inductance is ignored. In practical design, however, duty cycle losses take a considerable amount of the switching cycle and should be considered to obtain the correct output voltage equation. As observed in Figure 7, duty cycle losses take place not only during the $Q_1$ conduction period ($D_{L1}$), but also during the $Q_2$ conduction period ($D_{L2}$). Considering the duty cycle losses from Equations 7 and 8, the output voltage of Equation 4 is modified as:

$$V_o = \frac{(V_{in} - V_{CB})}{n} \cdot (D - D_{L2}) + \frac{V_{CB}}{n} \cdot (1 - D - D_{L1}) \quad (13)$$

Substituting Equations 2, 7, and 8 into 13, the output voltage in Equation 13 is simplified as:

$$V_o = \frac{2V_{in}}{n} \cdot D(1-D) - (\frac{2}{n})^2 \frac{I_o L_{lk}}{T_S} \quad (14)$$

As observed in Equation 14, duty cycle losses increase as the leakage inductance increases. Even though large leakage inductance increases ZVS load range and alleviates the reverse-recovery problem by reducing di/dt, it results in reduced transformer turns ratio, which causes more voltage stress on the rectifier diodes and increased conduction losses due to duty cycle losses. Considering the overall efficiency, leakage inductance resulting in 5~10% duty cycle losses ($D_{L1}$+$D_{L2}$) is proper.

## IV. DESIGN PROCEDURE

In this section, a design procedure is presented using the schematic of Figure 10 as a reference. A center tapped transformer is used in the rectifier stage and the input voltage is assumed to be supplied from power factor correction (PFC) pre-regulator. A DC-DC converter with a 192W/24V output has been selected as a design example. As a major device, FSFA-series Fairchild Power Switch (FPS$^{TM}$) is employed, which is an integrated Pulse Width Modulation (PWM) controller and MOSFETs specifically designed for Zero Voltage Switching (ZVS) half-bridge converters with minimal external components. Compared with a discrete MOSFET and PWM controller solution, the FSFA-series can reduce total cost, component count, size, and weight, while simultaneously increasing efficiency, productivity, and system reliability.

The design specifications are as follows:

- Nominal Input Voltage: 400$V_{DC}$ (output of PFC stage)
- Output: 24V/8A (192W)
- Hold-up Time Requirement: 20ms (50Hz Line Frequency)
- DC Link Capacitor of PFC Output: 330μF
- Switching Frequency: 100kHz
- Maximum Duty Cycle of PWM Controller: 50%

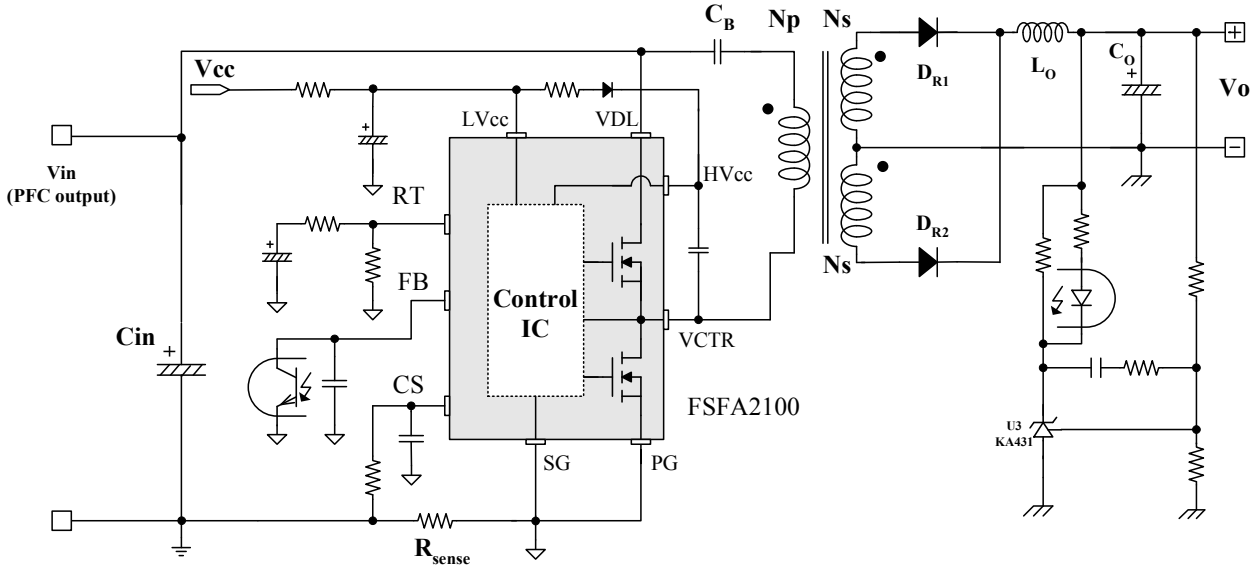


**Fig. 10. Reference circuit of an asymmetric PWM half-bridge converter for the design example.**

## [STEP-1] Define the System Specifications

The following specification should be defined.

**Estimated Efficiency ($E_{ff}$)**: The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. If no reference data is available, use $E_{ff}$ = 0.88~0.92 for low-voltage output applications and $E_{ff}$ = 0.92~0.96 for high-voltage output applications. With the estimated efficiency, the maximum input power is:

$$P_{in} = \frac{P_o}{E_{ff}} \tag{15}$$

**Input Voltage Range ($V_{in}^{min}$ and $V_{in}^{max}$)**: The maximum input voltage would be the nominal PFC output voltage:

$$V_{in}^{max} = V_{O.PFC} \tag{16}$$

Though the input voltage is regulated as a constant by the PFC pre-regulator, it drops during the hold-up time. The minimum input voltage, considering the hold-up time requirement, is given as:

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{in}}} \tag{17}$$

where $V_{O.PFC}$ is the nominal PFC output voltage, $T_{HU}$ is the hold-up time, and $C_{in}$ is the DC link bulk capacitor on the input side.

(Design Example) Assuming the efficiency is 92%,

$$P_{in} = \frac{P_o}{E_{ff}} = \frac{192}{0.92} = 209W$$

$$V_{in}^{max} = V_{O.PFC} = 400V$$

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{in}}} = \sqrt{400^2 - \frac{2 \cdot 209 \cdot 20 \times 10^{-3}}{330 \times 10^{-6}}} = 367V$$

## [STEP-2] Determine the Transformer Turns Ratio ($n=N_p/N_s$)

As observed in Equation 14, leakage inductance of the transformer results in duty cycle losses and affects the input to output voltage ratio. Considering the forward voltage drop in the rectifier diode, Equation 14 is modified as:

$$V_o + V_F = V_{in} D(1-D)\frac{2}{n} - (\frac{2}{n})^2 \frac{I_o L_{LK}}{T_S} \tag{18}$$

where $V_F$ is the secondary-side rectifier diode voltage drop.

There are three design parameters in Equation 18: duty cycle (D), transformer turns ratio (n), and leakage inductance. It is necessary to determine the leakage inductance prior to the transformer turns ratio and duty cycle. Rather than choosing the leakage inductance arbitrarily, it is reasonable to determine the leakage inductance by considering the duty cycle losses. The duty cycle losses are approximately:

$$D_{Loss} = D_{L1} + D_{L2} \cong \frac{16 \cdot P_{in} \cdot L_{lk}}{(V_{in}^{max})^2 \cdot T_S} \tag{19}$$

It is typical to set the duty cycle losses as 5~10% of the switching cycle. Once the leakage inductance is determined, the transformer turns ratio is calculated by solving Equation 18 for *n* with a given *D* as:

$$n = \frac{V_{in} D(1-D) + \sqrt{(V_{in} \cdot D \cdot (1-D))^2 - 4(V_o + V_F) I_o L_{lk} f_s}}{(V_o + V_F)} \tag{20}$$

When calculating the transformer turns ratio with minimum input voltage and maximum duty cycle condition, there should be some margin on the maximum duty cycle of the PWM controller to guarantee output voltage regulation.

(Design Example) By choosing duty cycle losses as 9% of the switching cycle, the leakage inductance is obtained as:

$$L_{lk} = \frac{D_{Loss} \cdot (V_{in}^{max})^2 \cdot T_S}{16 \cdot P_{in}}$$

$$= \frac{0.09 \cdot 400^2 \cdot 10 \times 10^{-6}}{16 \cdot 209} = 43\mu H$$

Considering 5% margin on the maximum duty cycle of the PWM controller (50±3%), the worst-case maximum duty cycle to calculate the transformer turns ratio is chosen as 42%. Assuming the forward voltage drop of the rectifier is 1.2V, the turns ratio is given as:

(Design Example — Continued)

$$n = \frac{V_{in}^{\min} D_{\max} \cdot (1 - D_{\max})}{(V_o + V_F)} + \frac{\sqrt{(V_{in}^{\min} \cdot D_{\max} \cdot (1 - D_{\max}))^2 - 4(V_o + V_F) I_o L_{lk} f_s}}{(V_o + V_F)}$$

$$= \frac{367 \cdot 0.42 \cdot (1 - 0.42)}{(24 + 1.2)} + \frac{\sqrt{(367 \cdot 0.42 \cdot (1 - 0.42))^2 - 4(24 + 1.2) \cdot 8 \cdot 43 \times 10^{-6} \cdot 100 \times 10^3}}{(V_o + V_F)}$$

$$= 6.2$$

## [STEP-3] Calculate the Nominal Duty Cycle for Maximum Input Voltage and Full-Load Condition

Since the turns ratio is determined in STEP-2, the nominal duty cycle for maximum input voltage and full load condition is obtained by solving:

$$V_o + V_F = V_{in}^{\max} \cdot D_{nom}(1 - D_{nom})(\frac{2}{n}) - (\frac{2}{n})^2 \frac{I_o L_{lk}}{T_S} \quad (21)$$

The nominal duty cycle is given as:

$$D_{nom} = \frac{1 - \sqrt{1 - 4[\frac{n(V_o + V_F)}{2V_{in}^{\max}} + \frac{2I_o L_{lk}}{nV_{in}^{\max} T_S}]}}{2} \quad (22)$$

(Design Example)

$$D_{nom} = \frac{1 - \sqrt{1 - 4[\frac{n(V_o + V_F)}{2V_{in}^{\max}} + \frac{2I_o L_{lk}}{nV_{in}^{\max} T_S}]}}{2} = \frac{1 - \sqrt{1 - 4[\frac{6.2 \cdot 25.2}{2 \cdot 400} + \frac{2 \cdot 8 \cdot 43 \times 10^{-6}}{6.2 \cdot 400 \cdot 10 \times 10^{-6}}]}}{2} = 0.34$$

## [STEP-4] Output Inductor Design

The current ripple of the output filter inductor is given as:

$$\Delta I_L = \frac{(\frac{V_{in}(1-D)}{n} - V_o - V_F)}{L_o} \times [DT_S - \frac{2I_O L_{lk}}{n \cdot V_{in}(1-D)}] \quad (23)$$

where $L_o$ is the output inductor.

It is typical to set the ripple as 10~20% of the rated output current.

(Design Example) By choosing the current ripple of the output inductor as 20% of the rated output current, the output inductance is given from Equation 23 as:

$$L_o = \frac{(\frac{V_{in}(1-D)}{n} - V_o - V_F)}{\Delta I_L} \times [DT_S - \frac{2I_O L_{lk}}{n \cdot V_{in}(1-D)}]$$

$$= \frac{(\frac{400 \cdot (1 - 0.34)}{6.2} - 25.2)}{8 \times 0.2} \times [0.34 \cdot 10 \times 10^{-6} - \frac{2 \cdot 8 \cdot 43 \times 10^{-6}}{6.2 \cdot 400 \cdot (1 - 0.34)}]$$

$$= 32.3 \mu H$$

The output inductor is smaller than the forward converter with the same current ripple and output power.

## [STEP-5] Determine the Magnetizing Inductance

As observed in Equations 10 and 12, the magnetizing inductance value is closely related to the ZVS condition, since it determines the peak current level during the switching transition. Of the two ZVS conditions in Equations 9 and 11, Equations 11 is the worst case for operation with a duty cycle below 50%. Thus, The ZVS condition for both MOSFETs is given as:

$$L_{lk}[\frac{I_o}{n} - I_{M.avg} + \frac{V_{in}(1-D)DT_S}{2L_m}]^2 > (C_1 + C_2) \cdot [(1-D)V_{in}]^2 \quad (24)$$

where $C_1$ and $C_2$ are the effective output capacitances (parasitic and external capacitance) for $Q_1$ and $Q_2$, respectively.

(Design Example)
Here, it is designed to guarantee ZVS from full load to 20% load. First, the duty cycle for 20% load condition is obtained as:

$$D_{@20\%} = \frac{1 - \sqrt{1 - 4[\frac{n(V_o + V_F)}{2V_{in}^{\max}} + \frac{2I_o L_{lk}}{nV_{in}^{\max} T_S}]}}{2} = \frac{1 - \sqrt{1 - 4[\frac{6.2 \cdot 25.2}{2 \cdot 400} + \frac{2 \cdot (8 \times 0.2) \cdot 43 \times 10^{-6}}{6.2 \cdot 400 \cdot 10 \times 10^{-6}}]}}{2} = 0.28$$

With the duty cycle at 20% load condition, the maximum magnetizing inductance value to guarantee ZVS is obtained by solving (24) for $L_m$ as:

$$L_m < \frac{V_{in}^{\max}(1-D)DT_S}{2[\sqrt{\frac{2C_{oss}}{L_{lk}}}(1-D)V_{in} - \frac{I_o}{n}2D]}$$

$$= \frac{400\cdot(1-0.28)\cdot 0.28\cdot 10\times 10^{-6}}{2[\sqrt{\frac{2\cdot 150\times 10^{-12}}{43\times 10^{-6}}}(1-0.28)\cdot 400 - \frac{8\times 0.2}{6.2}\cdot 2\cdot 0.28]}$$

$$= 654\mu H$$

The magnetizing inductance is determined as 630μH.

## [STEP-6] Design the Transformer

The peak magnetizing current is given as:

$$I_{M.pk} = \frac{V_{in}^{\max}D(1-D)T_S}{2L_m} + \frac{I_o}{n}(1-2D) \quad (25)$$

During transient or startup, the duty cycle can be almost zero. Thus, the magnetizing current should be calculated for the worst case of zero duty cycle. The minimum turns for the transformer primary side is given as:

$$N_p^{\min} = \frac{L_m I_{M.pk}}{A_e B_{\max}} \quad (26)$$

where $A_e$ is the core cross-sectional area in $mm^2$ and $B_{max}$ is the maximum flux density in Tesla.

Then, choose the proper number of turns for the secondary side that results in primary side turns larger than $N_p^{min}$ as:

$$N_p = n\cdot N_s > N_p^{\min} \quad (27)$$

The wire diameter should be chosen based on the current density. The current density is typically $5A/mm^2$ when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 6-10 $A/mm^2$ is also acceptable. Avoid using wire with a diameter larger than 0.4 mm to avoid skin-effect losses as well as to make winding easier. For a high-current output, it is better to use parallel windings with multiple strands of thinner wire to minimize the skin effect.

Figure 11 shows the primary-side current waveforms. The rms value of the primary side current is approximately given as:

$$I_p^{rms} = \sqrt{\frac{(I_{P0}^2 + I_{P0}I_{P3} + I_{P3}^2)}{3}D + \frac{(I_{P4}^2 + I_{P4}I_{P7} + I_{P7}^2)}{3}(1-D)} \quad (28)$$

$$I_{P0} = \frac{I_o}{n} + I_{M.avg} - \frac{V_{in}(1-D)DT_S}{2L_m} \quad (29)$$

$$I_{P3} = \frac{I_o}{n} + I_{M.avg} + \frac{V_{in}(1-D)DT_S}{2L_m} \quad (30)$$

$$I_{P4} = -\frac{I_o}{n} + I_{M.avg} + \frac{V_{in}(1-D)DT_S}{2L_m} \quad (31)$$

$$I_{P7} = -\frac{I_o}{n} + I_{M.avg} - \frac{V_{in}(1-D)DT_S}{2L_m} \quad (32)$$

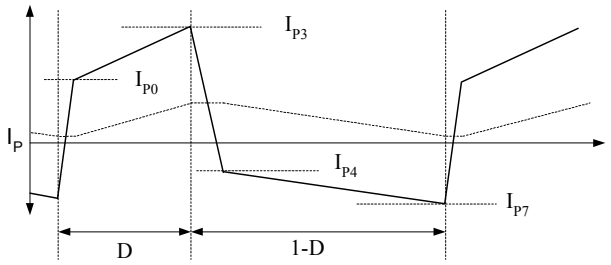


**Fig. 11. Primary-side current waveforms.**

The rms current for secondary windings are uneven for duty cycles smaller than 50%. The current in the winding for diode $D_{F1}$ in normal operation is:

$$I_{DF1}^{rms} \cong I_o\sqrt{D} \quad (33)$$

Meanwhile, the current in winding for $D_{F2}$ diode in normal operation is:

$$I_{DF2}^{rms} \cong I_o\sqrt{(1-D)} \quad (34)$$

(Design Example) For worst case zero duty cycle (D=0), the maximum magnetizing current is:

$$I_{M.pk} = \frac{V_{in}^{\max}D(1-D)T_S}{2L_m} + \frac{I_o}{n}(1-2D)$$

$$= \frac{8}{6.2}(1-2\cdot 0) = 1.29A$$

Since the primary-side current equals the magnetizing current plus the output current referred to the primary, magnetizing current can reach the pulse-by-pulse current limit level given by PWM controller during transient. There should be enough margin in transformer design, however, $B_{max}$=0.15T is used to guarantee non-saturation of the transformer during transient (EER3542, $A_e$=109$mm^2$). The maximum flux density in the worst case scenario will be checked in STEP-8 after current limit level is determined. The minimum number of turns for the primary winding is given as:

$$N_p^{\min} = \frac{L_m I_{M.pk}}{A_e B_{\max}} = \frac{630\times 10^{-6}\cdot 1.29}{109\times 10^{-6}\cdot 0.15} = 49.7turns$$

The primary and secondary-side turns are determined as 50 turns and 8 turns, respectively.

The rms value of the primary-side current is given by:

$$I_{P0} = \frac{8}{6.2} + 0.41 - \frac{400 \cdot (1-0.34) \cdot 0.34 \cdot 10 \times 10^{-6}}{2 \cdot 630 \times 10^{-6}} = 0.99A$$

$$I_{P3} = \frac{8}{6.2} + 0.41 + \frac{400 \cdot (1-0.34) \cdot 0.34 \cdot 10 \times 10^{-6}}{2 \cdot 630 \times 10^{-6}} = 2.42A$$

$$I_{P4} = -\frac{8}{6.2} + 0.41 + \frac{400 \cdot (1-0.34) \cdot 0.34 \cdot 10 \times 10^{-6}}{2 \cdot 630 \times 10^{-6}} = -0.17A$$

$$I_{P7} = -\frac{8}{6.2} + 0.41 - \frac{400 \cdot (1-0.34) \cdot 0.34 \cdot 10 \times 10^{-6}}{2 \cdot 630 \times 10^{-6}} = -1.59A$$

$$I_p^{rms} = 1.29A$$

The current in the winding for $D_{F1}$ diode in normal operation is

$$I_{DF1}^{rms} \cong I_o \sqrt{D} = 8 \cdot \sqrt{0.34} = 4.7A$$

Meanwhile, the current in the winding for $D_{F2}$ diode in normal operation is:

$$I_{DF2}^{rms} \cong I_o \sqrt{(1-D)} = 8 \cdot \sqrt{(1-0.34)} = 6.5A$$

For the primary winding, 0.12φ×30 (Litz wire) is selected and the current density is 3.8A/mm$^2$. In the case of the secondary winding, 0.1φ×100 (Litz wire) is selected and the current densities are 5.9A/mm$^2$ and 8.2A/mm2 for $D_{F1}$ and $D_{F2}$, respectively.

## [STEP-7] DC Blocking Capacitor Selection

Even though it has been assumed that the DC blocking capacitor CB is large enough to neglect the voltage ripple across CB, too large a capacitor results in slow dynamic response. Thus, it is typical to select the capacitor so that the ripple is 5~10% of the input voltage. The voltage ripple of DC blocking capacitor is given as:

$$\Delta V_{CB} \cong \frac{1}{C_B} \int_0^{DT_S} i_p dt = \frac{1}{C_B} [\frac{I_o}{n} + \frac{I_o}{n}(1-2D)] \quad (35)$$

(Design Example)

To set the voltage ripple below 30V, the minimum DC blocking capacitor value is obtained from

$$\frac{1}{C_B} \int_0^{DT_S} i_p dt = \frac{1}{C_B} [\frac{I_o}{n} + \frac{I_o}{n}(1-2D_{nom})] < 30V$$

$$C_B > \frac{1}{30V} [\frac{I_o}{n} + \frac{I_o}{n}(1-2D_{nom})] D_{nom} T_S$$

$$C_B > \frac{1}{30V} [\frac{8}{6.2} + \frac{8}{6.2}(1-2 \cdot 0.34)] \cdot 0.34 \cdot 10 \times 10^{-6} = 193nF$$

The voltage of $C_B$ is given as $V_{IN} \times D$ by (2) and the maximum capacitor voltage is theoretically half of the input voltage. However, it can reach the input voltage while the converter is not operating if the leakage currents of the MOSFETs are unbalanced. Thus, voltage rating should be higher than maximum input voltage (400V).

Another important factor to consider when selecting the capacitor is the current rating. Since the primary-side current of 1.27A calculated in STEP-6 flows through the capacitor, a low-ESR capacitor should be chosen. Thus, a 220nF/275$V_{AC}$ film capacitor is selected.

## [STEP-8] Current Sensing

To determine the pulse-by-pulse current limit level, the peak current in the primary side should be obtained first as:

$$I_p^{pk} = \frac{I_o}{n}(2-2D_{nom}) + \frac{V_{in} D_{nom} (1-D_{nom}) T_S}{2L_m} \quad (36)$$

(Design Example)

The peak current is obtained as:

$$I_p^{pk} = \frac{I_o}{n}(2-2D_{nom}) + \frac{V_{in} D_{nom} (1-D_{nom}) T_S}{2L_m}$$

$$= \frac{8}{6.2}(2-2 \cdot 0.34) + \frac{400 \cdot 0.34 \cdot (1-0.34) \cdot 10 \times 10^{-6}}{2 \cdot 630 \times 10^{-6}}$$

$$= 2.41A$$

Current limit level is determined as 3A, using 0.2Ω resistor since the current limit threshold voltage is 0.6V.

As mentioned in STEP-6, the transformer magnetizing current can reach the pulse-by-pulse current limit level given by the PWM controller during transient. Therefore, the maximum flux density of transformer should be checked as.

$$B_{\max}^{worst} = \frac{L_m I_{LIM}}{A_e N_p^{\min}} = \frac{630 \times 10^{-6} \cdot 3}{109 \times 10^{-6} \cdot 50} = 0.35T$$

## [STEP-9] Diode Selection

The voltage stress for each rectifier diode ($D_{F1}$ and $D_{F2}$) is given as:

$$V_{DF1} = V_{in} \cdot D \cdot \frac{2}{n} \quad (37)$$

$$V_{DF2} = V_{in} \cdot (1-D) \cdot \frac{2}{n} \quad (38)$$

(Design Example)
Considering a worst case of D=50% for $D_{F1}$:

$$V_{DF1} = 400 \cdot 0.5 \cdot \frac{2}{6.2} = 64V$$

Considering a worst case of D=0% for $D_{F2}$:

$$V_{DF2} = 400 \cdot 1 \cdot \frac{2}{6.2} = 128V$$

Considering voltage overshoot and ringing, 100V and 200V diodes are selected for $D_{F1}$ and $D_{F2}$, respectively. The current for each diode obtained in STEP-6 is:

$$I_{DF1}^{rms} \cong I_o\sqrt{D} = 8 \cdot \sqrt{0.34} = 4.7A$$

$$I_{DF2}^{rms} \cong I_o\sqrt{(1-D)} = 8 \cdot \sqrt{(1-0.34)} = 6.5A$$

## V. DESIGN TIPS

### *A. Unbalanced Secondary Turns Transformer*

When a center-tapped winding is used in the transformer secondary winding, unbalanced turns can be used to optimize the transformer design, as shown in Figure 12. The magnetizing current of the transformer is shifted, as shown in Figure 13, by using a transformer with unbalanced secondary turns. The average value of the magnetizing current, or the DC offset of the magnetizing current, is given as:

$$I_{M.avg} = I_o \frac{N_{S2}}{N_p}(1-D) - I_o \frac{N_{S1}}{N_p} D \tag{39}$$

This becomes zero especially when:

$$D = \frac{N_{S2}}{N_{S1} + N_{S2}} \tag{40}$$

Thus, the magnetizing current DC offset for some operating point can be made virtually zero using unbalanced turns. However, this increases current ripple in the output inductor, which results in a larger inductor on the secondary side. The unbalanced transformer should be designed using trade-offs between the transformer size and the inductor size. Notice that the diode voltage stress remains unchanged, even when unbalanced turns are used.

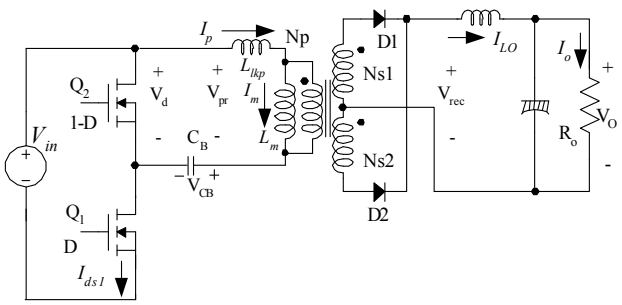


**Fig. 12. Transformer with unbalanced secondary turns.**

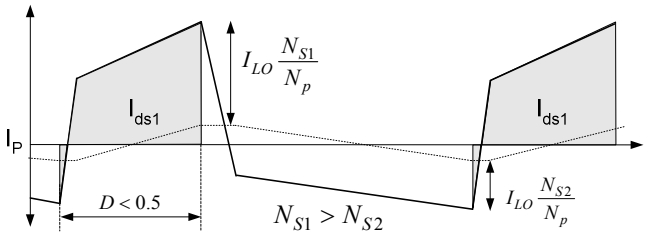


**Fig. 13. Shift of magnetizing current by a transformer with unbalanced secondary turns.**

### *B. External Soft-Start*

Even though the FSFA-series has internal soft-start, current overshoot can occur during startup when the leakage inductance is very small, as depicted in Figure 14.

When Q1 is first turned on, the primary-side voltage is only imposed on the leakage inductance until the secondary-side rectifier diode is turned on. This induces high di/dt current in the primary side and the current can exceed the pulse-by-pulse current limit level during the leading-edge blanking (LEB) time and turn-off delay time. To reduce the current overshoot, PFM (pulse-frequency-modulation) soft-start can be added to the internal PWM soft-start using an external capacitor and resistor on the RT pin, as shown in Figure 14.

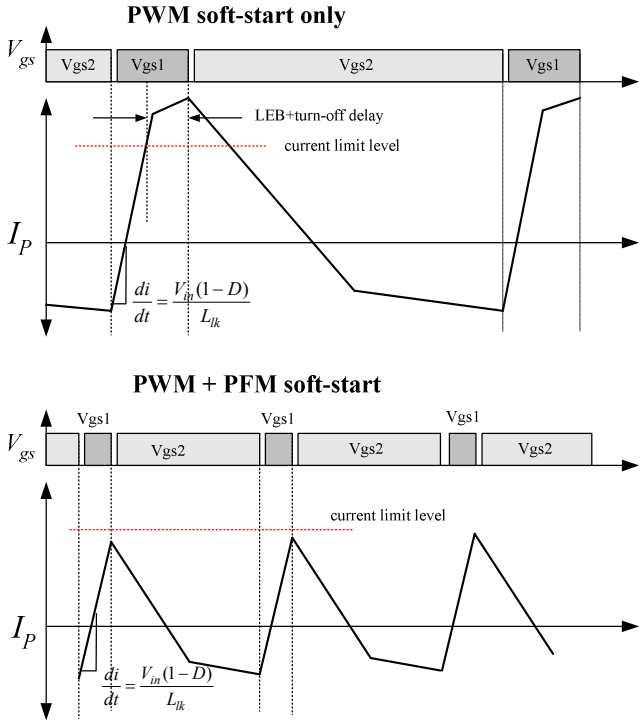


**Fig. 14. Soft-start waveforms comparison.**

## VI. EXPERIMENTAL VERIFICATION

To show the validity of the design procedure presented in this paper, the converter of the design example was built and tested. All circuit components are used as designed. Figure 15 shows the final schematic of the asymmetric PWM half-bridge converter design example. Since the leakage inductance is relatively small, frequency modulated soft-start is incorporated with the original PWM soft-start to reduce the current overshoot. Figure 16 shows the transformer structure. To obtain the design leakage inductance value, edge winding rather than center winding is used for the secondary-side turns.

Figure 17 shows the drain-to-source voltage of $Q_1$ and the transformer primary-side current ($I_p$) waveforms at full load condition. From the drain-to-source voltage of $Q_1$, the duty cycle for $Q_1$ is about 34% as designed in STEP-3. Figure 18 shows the drain-to-source voltage of $Q_1$ and transformer primary-side current ($I_p$) waveforms at no-load condition. As observed, the converter operates in burst mode due to the built-in burst mode operation of the FSFA2100. The power consumption at no load is 0.3W, including the power consumption of the controller. Figure 19 shows the drain-to-source voltage and current waveforms of $Q_1$ at full-load condition. The drain voltage drops to zero and the body diode conducts before the switch is turned on. The peak value of the drain current is about 2.4A, as designed. Figure 20 shows the drain-to-source voltage of $Q_1$ and voltage and current of the rectifier diode D211. As observed, the conduction duration of the diode D211 is less than half of the switching cycle. Figure 21 shows the drain-to-source voltage of $Q_1$ and voltage and current of rectifier diode D212. As observed, the conduction duration of the diode D212 is more than half of the switching cycle. As observed from Figure 20 and 21, the voltage stresses of these diodes are uneven. Thus, a 200V rated diode is required for D212 to handle the voltage overshoot while a 100V rated diode is used for D211. Thanks to the reduced di/dt by the leakage inductance, there is almost no reverse recovery, even though the 200V ultra-fast diode is used. Figure 22 shows the soft-start waveforms. Since the leakage inductance is relatively small, frequency modulated soft-start is incorporated with the original PWM soft-start to reduce the current overshoot. Figure 23 shows the measured efficiency for different load conditions. The efficiency at full-load condition is about 93%.

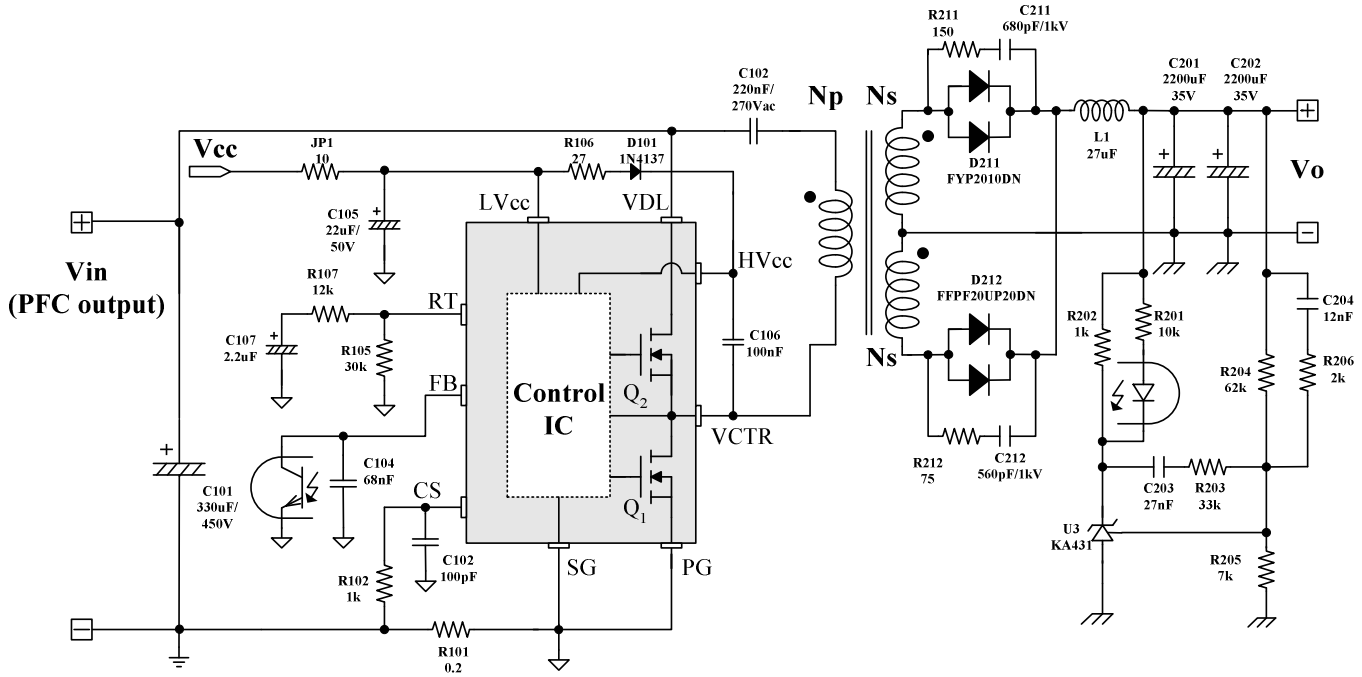


**Fig. 15. Schematic of an asymmetric PWM half-bridge converter.**

- Core: EER3542 (Ae=109 $mm^2$)
- Bobbin: EER3542 (Horizontal)

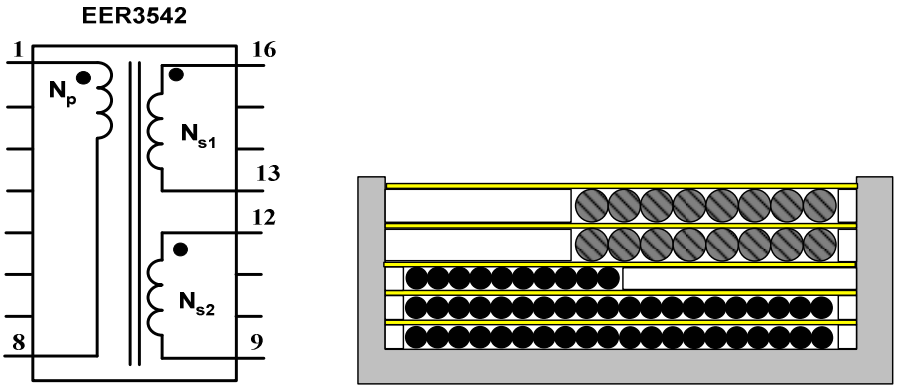


**Fig. 16. Transformer structure.**

| | Pin(S → F) | Wire | Turns | Winding Method |
|---|---|---|---|---|
| $N_p$ | 1 → 8 | 0.12φ×30 (Litz wire) | 50 | Solenoid Winding |
| $N_{s1}$ | 16 → 13 | 0.1φ×100 (Litz wire) | 8 | Solenoid Winding |
| $N_{s2}$ | 12 → 9 | 0.1φ×100 (Litz wire) | 8 | Solenoid Winding |

| | Pin | Spec. | Remark |
|---|---|---|---|
| Inductance | 1 – 8 | 630μH ± 5% | 100kHz, 1V |
| Leakage | 1 – 8 | 45μH ± 10% | Short one of the secondary windings. |

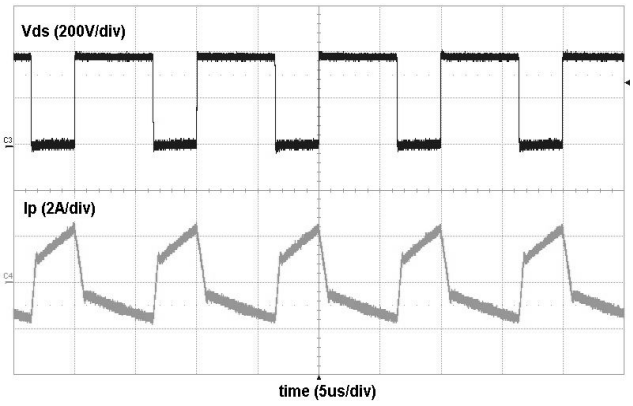


**Fig. 17. Operation waveforms at full load condition.**

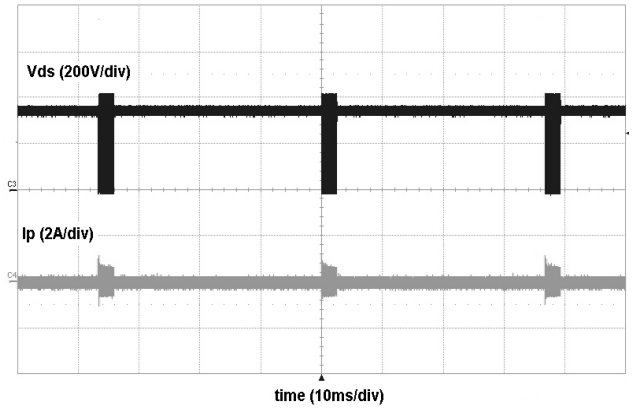


**Fig. 18. Operation waveforms at no load condition.**

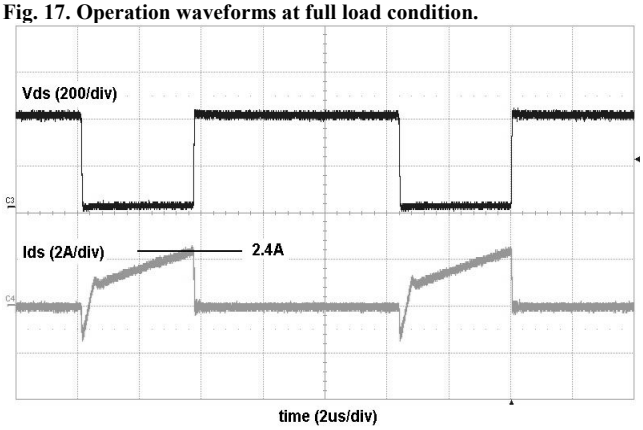


**Fig. 19. Zero voltage switching waveforms at full load condition.**

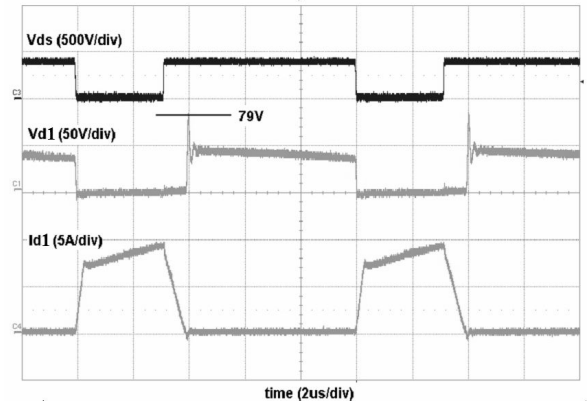


**Fig. 20. Rectifier diode (D211) waveforms at full load.**

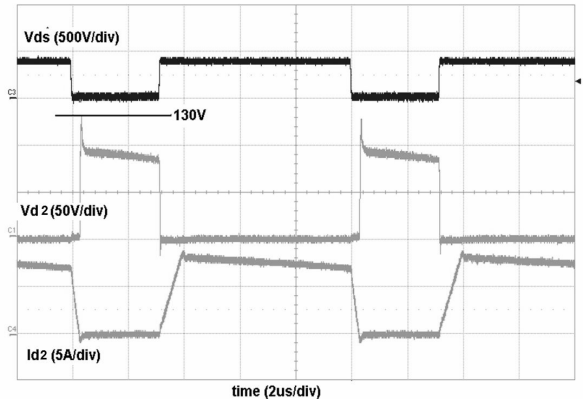


**Fig. 21. Rectifier diode (D212) waveforms at full load.**

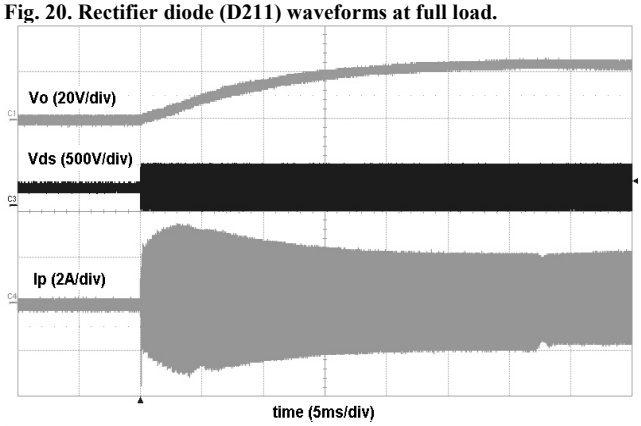


**Fig. 22. Soft-start waveforms at full load.**

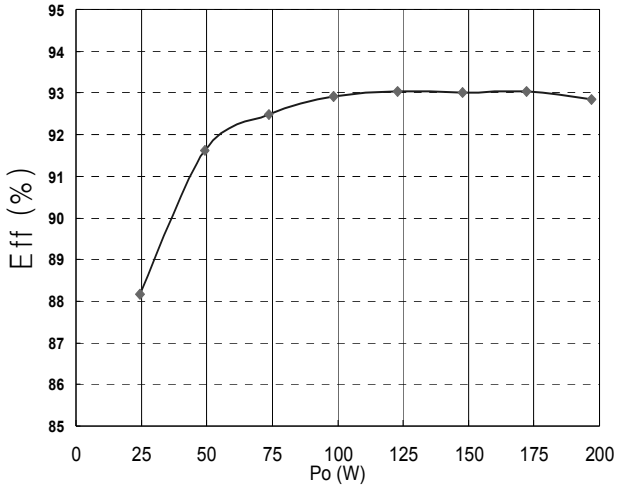


**Fig. 23. Measured efficiency.**

## VII. CONCLUSION

This paper presents design considerations of an asymmetric PWM half-bridge converter. The practical design procedure ends with a design example of a 24V/8A (192W) asymmetric half-bridge converter, which validates the discussion.

## VIII. REFERENCES


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**Hangseok Choi** received B.S., M.S., and Ph.D degrees in electrical engineering from Seoul National University, in 1996, 1999, and 2002, respectively. From 2002 to 2007, he worked for Fairchild Semiconductor in Korea as a system and application engineer. He is currently working for Fairchild Semiconductor in Bedford, NH, USA, as a principal system and application engineer. His research interests include soft-switching techniques, modeling, and control of converters. He has published 15 papers in IEEE conferences and transactions and 12 application notes for Fairchild Semiconductor.