User Guide for

FEBFAN6604MR_CH11U65A

Evaluation Board

Fairchild Computing Notebook Adapter

Featured Fairchild Product:

FAN6604MR

Direct questions or comments about this evaluation board to: "Worldwide Direct Support"

Fairchild Semiconductor.com

Table of Contents

This user guide supports the evaluation kit for the FAN6604MR. It should be used in conjunction with the FAN6604MR datasheets as well as Fairchild's application notes and technical support team. Please visit Fairchild's website at https://www.fairchildsemi.com/

1. Introduction

This document is an engineering report describing a 65 W power supply using FAN6604MR PWM controller. This power supply is targeted towards power adapters and open-frame for consumer products.

With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, FAN6604MR is manufactured by using the BiCMOS process. This allows an operating current of 1.7 mA and low startup current of 30 μA. Built-in synchronized slope compensation ensures the stability of Peak Current Mode control.

2. Evaluation Board Specifications

The data for Table 1 was measured with 90 V_{AC}~264 V_{AC} line input at an ambient temperature of 25°C.

Table 1. Summary of Features and Performance

Specification	Min.	Max.	Unit
Input Voltage	90	264	V_{AC}
Input Frequency	47	63	Hz

Description	Design Spec.	Test Results	Comments
Output Voltage	18.05 ~ 19.95 V	±0.08%	CV<± 5% Regulation CC<±5% Regulation
Output Current Protection	4.1 ~ 5.1 A	4.635 ~ 4.783 A	
Input Power	< 100 mW	90 mW	264 V_{AC}
Ripple	< 250 mVp-p	101 mVp-p (Max.)	Measured at PCB End
Startup Time	< 3 S	2.3 S	Full Load
Dynamic	> 18.5 V	18.83 V	Measure at PCB End
Voltage Stress	600 V	584 V	264 V_{AC}
	150 V	124 V	
Efficiency	Avg. > 87%	87.9 % at 115 V_{AC} 88.5 % at 230 V_{AC}	Meets Energy Star v2.0
Conducted EMI	Under 6 dB	3 dB Margin	Meets CISPER22B/EN55022B/IEC950/UL1950 Class II

3. Photographs

Figure 1. Photograph (W x L: 40 x 103 mm2) Top View

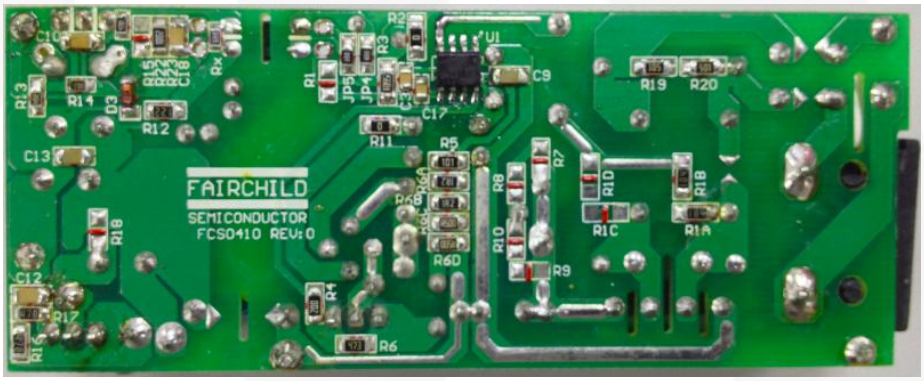


Figure 2. Photograph (W x L: 40 x 103 mm2) Bottom View

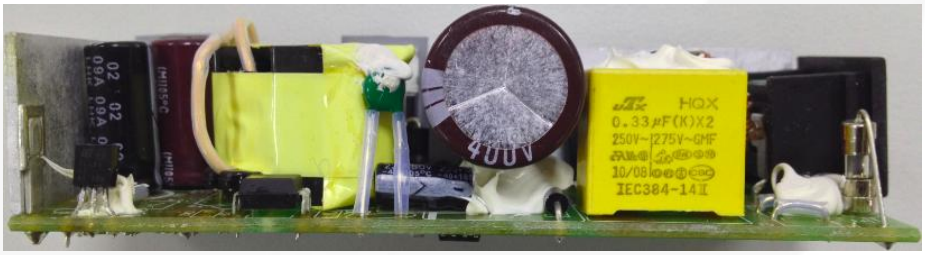


Figure 3. Photograph (H:27 mm) Side View

4. Printed Circuit Board

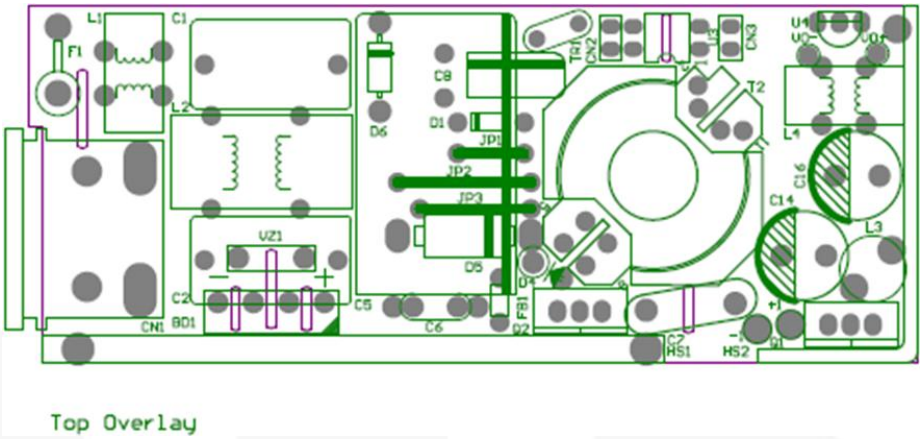


Figure 4. Top View

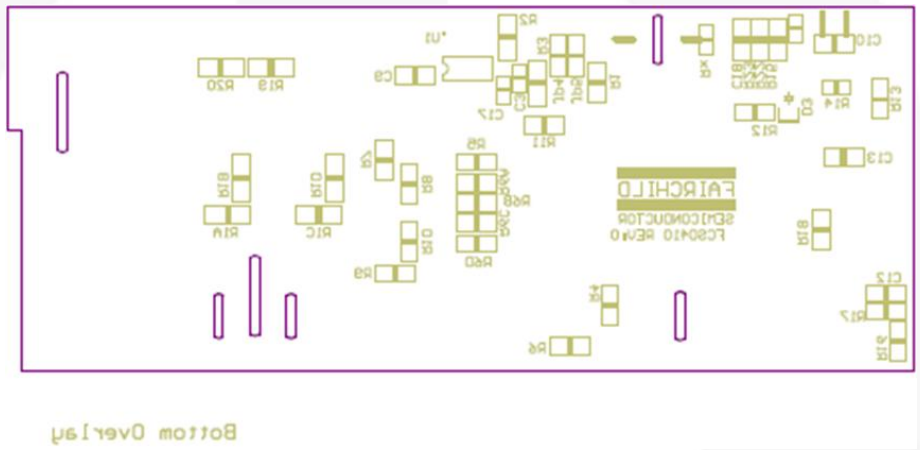


Figure 5. Bottom View

5. Schematic

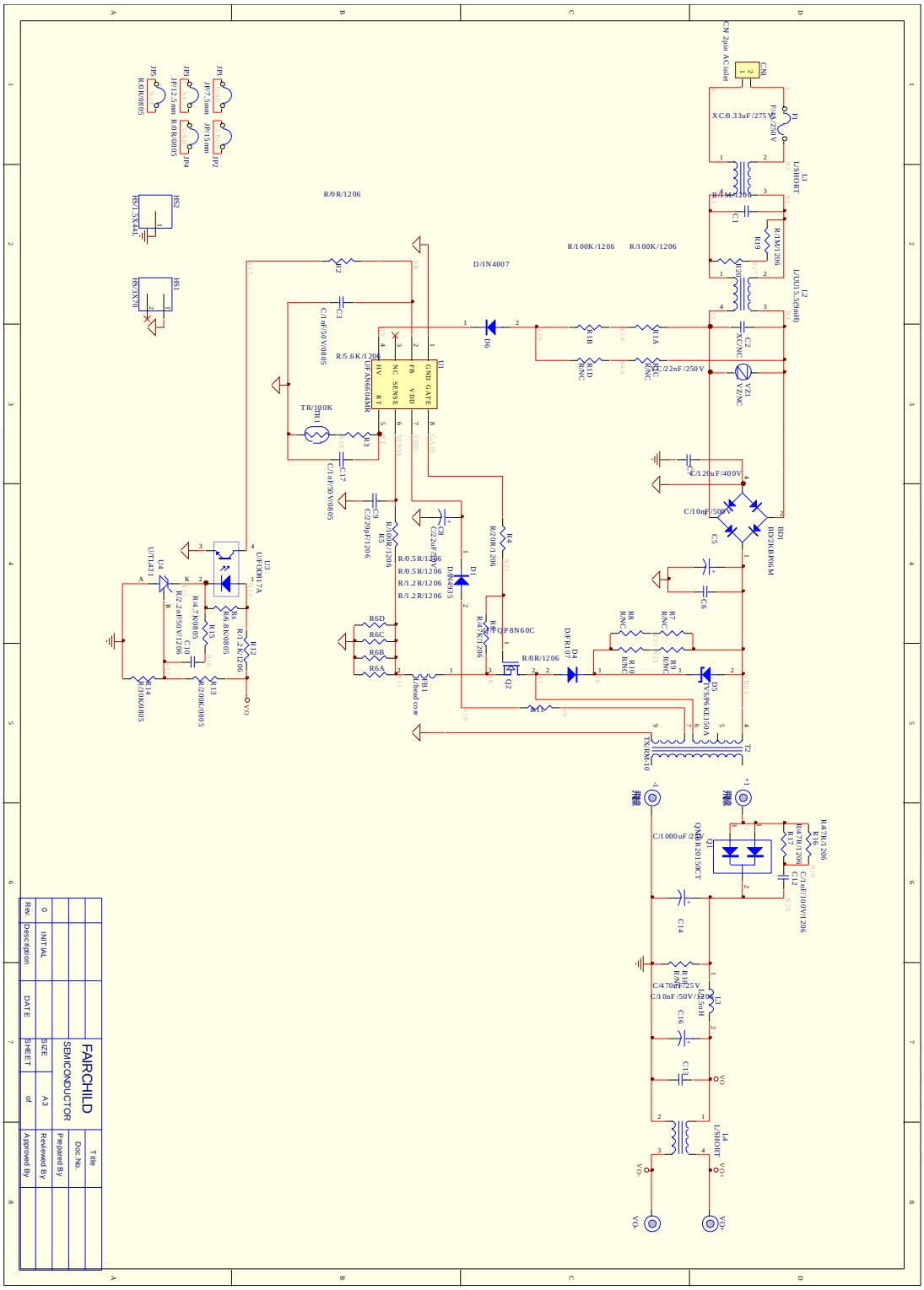


Figure 6. Evaluation Board Schematic

6. Bill of Materials

Part Specification	Package	Qty.	No.
JUMPER WIRE 0.8ψ(mm)	REEL	7	L1, L4, JP1, JP2, JP3
Chip Resistor 0805 0 Ω ±5%	REEL	1	JP4
Chip Resistor 0805 4K7 Ω ±1%	REEL	1	R15
Chip Resistor 0805 6K8 Ω ±5%	REEL	1	Rx
Chip Resistor 0805 30 KΩ ±5%	REEL	1	R14
Chip Resistor 0805 200 KΩ ±5%	REEL	1	R13
Chip Resistor 1206 0 Ω ±5%	REEL	2	R2, R11
Chip Resistor 1206 0 Ω 5 ±5%	REEL	2	R6C, R6D
Chip Resistor 1206 1 Ω 2 ±5%	REEL	2	R6A, R6B
Chip Resistor 1206 20 Ω ±5%	REEL	1	R4
Chip Resistor 1206 47 Ω ±5%	REEL	2	R16, R17
Chip Resistor 1206 100 Ω ±5%	REEL	1	R5
Chip Resistor 1206 1K2 Ω ±5%	REEL	1	R12
Chip Resistor 1206 5K6 Ω ±1%	REEL	1	R3
Chip Resistor 1206 47 KΩ ±5%	REEL	1	R6
Chip Resistor 1206 100 KΩ ±5%	REEL	2	R1A, R1B
Chip Resistor 1206 1 MΩ ±5%	REEL	2	R19, R20
NTC 5ψ 100000 Ω	REEL	1	TR1
Ceramic Capacitor 103P 500 V +80/-20%	REEL	1	C6
0805 MLCC X7R ±10% 102P 50 V	REEL	2	C3, C17
1206 MLCC X7R ±10% 102P 100 V	REEL	1	C12
1206 MLCC X7R ±10% 103P 50 V	REEL	1	C13
1206 MLCC X7R ±10% 221P 50 V	REEL	1	C9
1206 MLCC X7R ±10% 222P 50 V	REEL	1	C10
Electrolytic Capacitor 22 µ 50 V 105°C	JACKCON	1	C8
Electrolytic Capacitor 120 µ 400 V 105°C	NCC	1	C5
Electrolytic Capacitor 470 µ 25 V 105°C	NCC	1	C16
Electrolytic Capacitor 1000 µ 25 V 105°C	NCC	1	C14
X2 Capacitor 0.33 µ 275 V ±20%	REEL	1	C1
Y2 Capacitor 222P 250 V ±20%	REEL	1	C7
Inductor 1.7 µH	SUMIDA (74M-431)	1	L3
Common Choke 9 mH	SUMIDA (04291-T144)	1	L2
Bead Core C8B 3.5*3.2*1.0+T	MCH0041 (REEL)	1	FB1
Bead Core C8B 3.5*3.2*1.0	MCH0040	2	D4, C7

Continued on the following page…

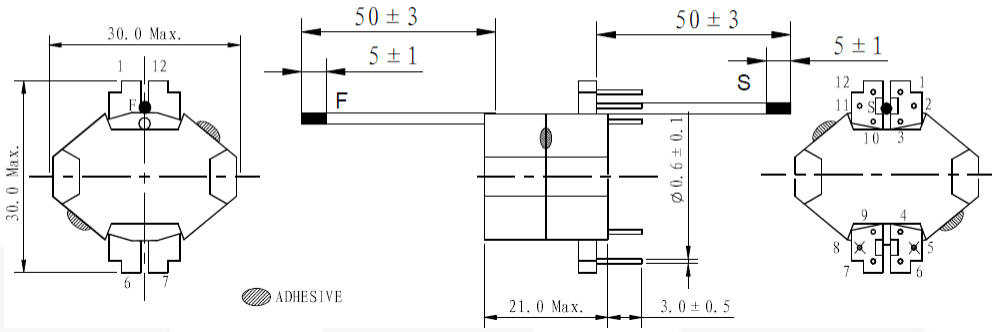
Part Specification	Package	Qty.	No.
Transformer RM-10 510 µH	SUMIDA (PS15-020)	1	T2
Diode 1 A/20 V	1N4935 (DO-41)	1	D1
Fast Diode 1 A/1000 V	FR107	1	D4
Diode 1 A/1000 V	1N4007	1	D6
Bridge 2 A/600 V	2KBP06M (Fairchild)	1	BD1
Schottky Diode 20 A/150 V	MBR20150CT (TO-220)	1	Q1
REGULATOR TL431ACZ-AP ±1%	TO-92	1	U4
MOSFET 8 A/600 V	FQP8N60C (TO-220)	1	Q2
IC FOD817A	DIP	2	U2, U3
FUSE GLASS 250V4A QUICK	REEL	1	F1
TVS P6KE150A	REEL	1	D5
INLET 2P 90°		1	CN1
PWM Controller IC SOIC	FAN6604MR 8-pin SOP	1	U1
Heat Sink 70 x 20 x 3.0 mm	MCH0534	1	HS1
Heat Sink 20 x 40 x 18 x 1.5 mm	MCH0555	1	HS2
CANADA Silicone ES2482W 333 ml		0	CN2, CN3, CN2A, CN3A
PCB FCS0410 REV 0		1	

7. Transformer and Winding Specifications

- Core: RM-10
- Bobbin: RM-10

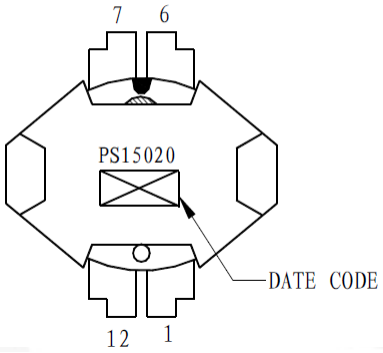
1.Appearance

1-1.Dimension(mm)

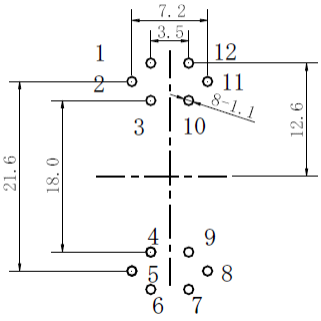


* Terminals should be measured excluding the length of the soldered point.
* Dimensions non-toleranced are just for reference.
* "×" indicates no terminal.

1-2.Stamp

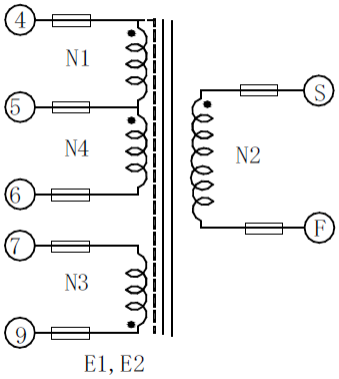


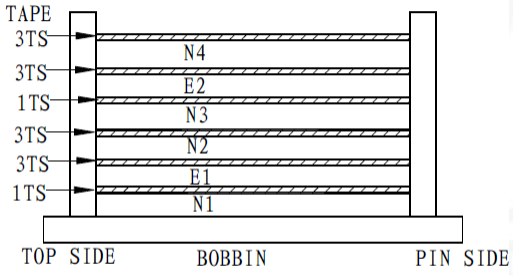
1-3 Recommended land patterns dimension



2.Coil specification

2-1.Electric schematic





" S "indicates winding polarity.

Figure 7. Transformer Specifications & Construction

Table 2. Winding Specifications

Winding	Terminal		Winding	Turns	Isolation Layer
	Start Pin	End Pin			Turns
N4	5	6	0.5 mm*1	19	3
Copper Shielding (E2)	Open	4	Copper Foil 0.025 mm	1.2	3
N3	9	7	0.4 mm*1	7	1
N2	S	F	0.9 mm*1	8	3
Copper Shielding (E1)	Open	4	Copper Foil 0.025 mm	1.2	3
N1	4	5	0.5 mm*1	19	1

Table 3. Electrical Characteristics

	Pin	Specification	Remark
Inductance	4 - 6	510 µH ±10%	1 kHz, 1 V
Effective Leakage	4 - 6	20 µH Max.	Short Other Pin

8. Test Conditions & Test Equipment

Table 4. Test Conditions & Test Equipment

Evaluation Board #	FEBFAN6604MR_CH11U65A
Test Date	2014-10-28
Test Temperature	25℃
Test Equipments	AC Power Source: 6800 AC POWER SOURCE Electronic Load: Chroma 63030 and 63102 Power Meter : WT210 Oscilloscope : LeCory 24Xs-A

9. Performance of Evaluation Board

9.1. Input Power at No Load Condition

Test Condition:

Measure the input power at three output voltage level at no load condition.

Table 5. Test Results

Input Voltage	Input Wattage	Output Voltage
90 V_{AC} / 60 Hz	44 mW	19.2 V
115 V_{AC} / 60 Hz	47 mW	19.2 V
230 V_{AC} / 50 Hz	79 mW	19.2 V
264 V_{AC} / 50 Hz	90 mW	19.2 V

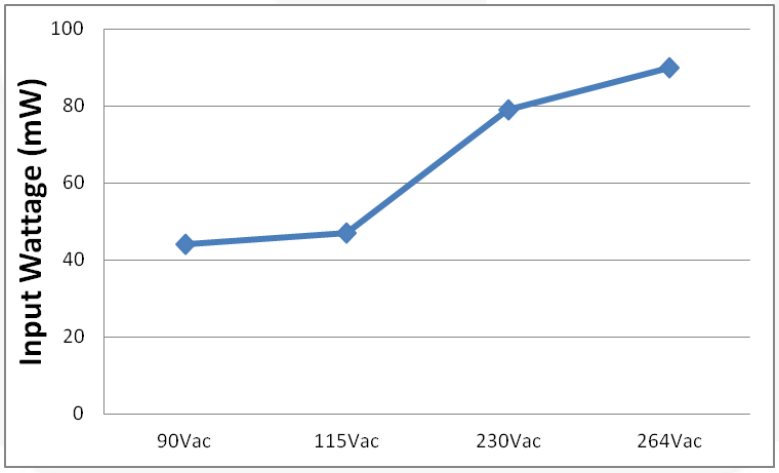


Figure 8. Input Wattage Curve

9.2. Startup Time

Test Condition:

Measure the time from AC plug-in to nominal output voltage build-up at full load condition.

Table 6. Test Results

Input Voltage	Startup Time	Specification
90 V_{AC} / 60 Hz	2.300 s	<3 sec
264 V_{AC} / 50 Hz	0.758 s	

Waveform:

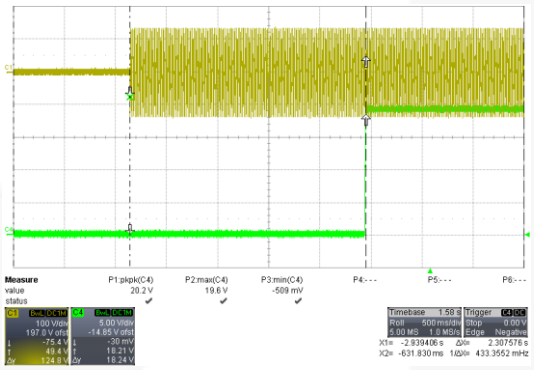


Figure 9. C1[V_{IN}], C4[Vo], 90 V_{AC} / 60 Hz

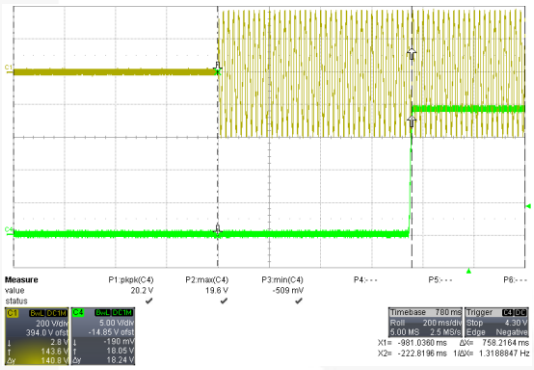


Figure 10. C1[V_{IN}], C4[Vo]. 264 V_{AC} / 50 Hz

9.3. Hold-up Time

Test Condition:

Set output at maximum load. Measure the time interval between AC off and output voltage falling to lower limit of rated value. The AC waveform should be off at zero degree.

Table 7. Test Results

Input Voltage	Hold-up Time	Specification
90 V_{AC} / 60 Hz	8.5 ms	
264 V_{AC} / 50 Hz	119.0 ms	

Waveforms:

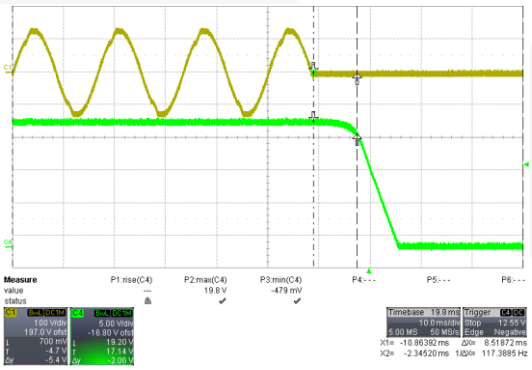


Figure 11. C1[V_{IN}], C4[V_O], 90 V_{AC} / 60 Hz

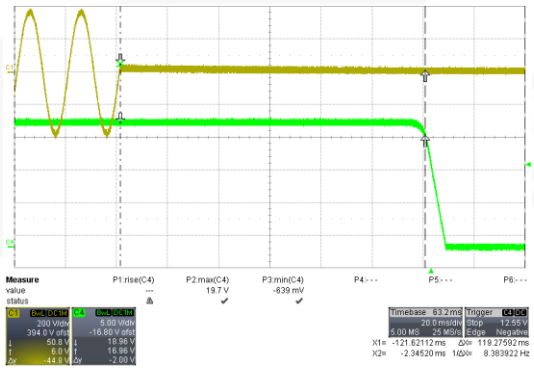


Figure 12. C1[V_{IN}], C4[V_O], 264 V_{AC} / 50 Hz

9.4. Input Current

Test Condition:

Measure the AC input current at maximum output loading, where the maximum input power occurs.

Table 8. Test Results

Input Voltage	Input Current	Specification
90 V_{AC} / 60 Hz	1.681 A	< 2 A
264 V_{AC} / 50 Hz	0.680 A	

9.5. DC Output Rising Time

Test Condition:

Measure the time interval between 10% to 90% of output voltage during startup.

Table 9. Test Results

Input Voltage	Minimum Load	Full Load	Specification
90 V_{AC}/60 Hz	5.38 ms	9.40 ms	<20 ms
264 V_{AC}/50 Hz	5.21 ms	8.86 ms	

Waveforms:

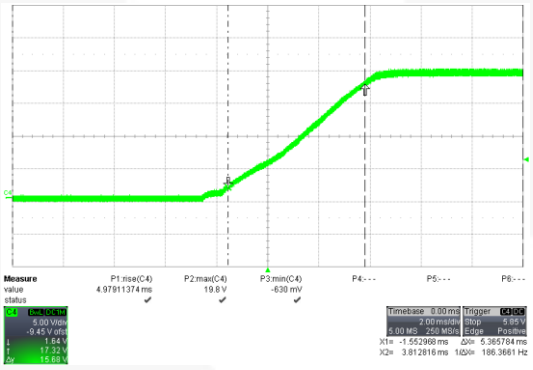


Figure 13. C4[V_O], 90 V_{AC}/60 Hz, Minimum Load

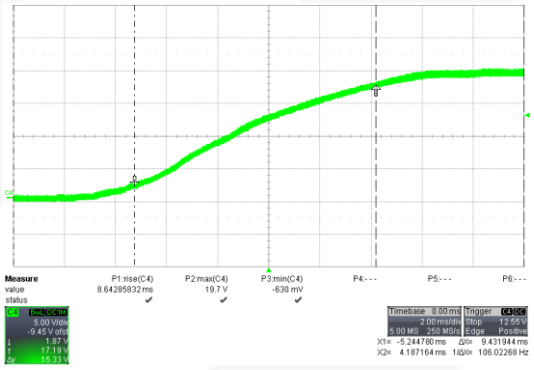


Figure 14. C4[V_O], 90 V_{AC}/60 Hz, Full Load

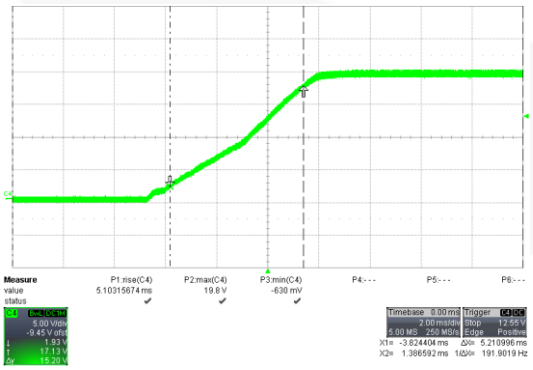


Figure 15. C4[V_O], 264 V_{AC}/50 Hz, Minimum Load

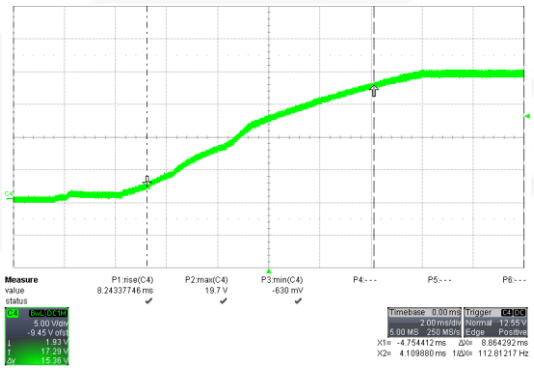


Figure 16. C4[V_O] 264 V_{AC}/50 Hz, Full Load

9.6. Dynamic Response

Test Condition

Dynamic loading (0%~100%), 50% duty cycle (5 ms), 2.5 A/µsec rise/fall time. Measured at PCB end.

Table 10. Test Results

Input Voltage	Overshoot	Undershoot	Specification
115 V_{AC}/60 Hz	157 mV	163 mV	> V
230 V_{AC}/50 Hz	141 mV	144 mV	

Waveforms:

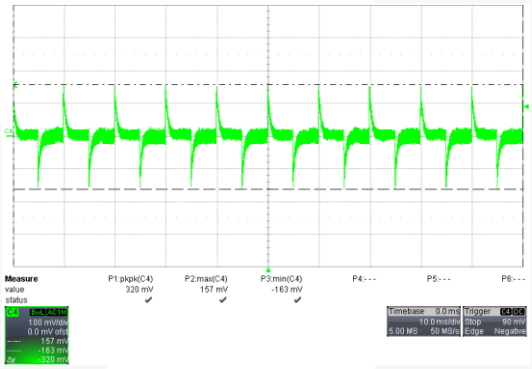


Figure 17. C4[V_O], 115 V_{AC} / 60 Hz

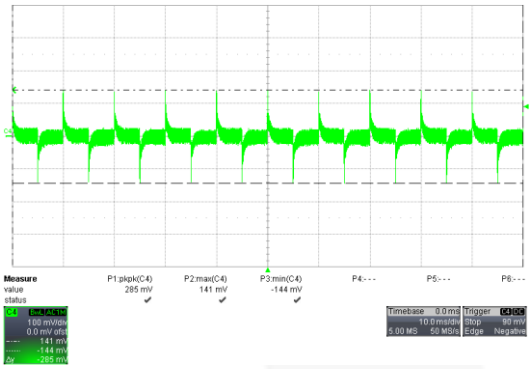


Figure 18. C4[V_O], 230 V_{AC} / 50 Hz

9.7. Output Ripple & Noise

Test Condition

Measure the output voltage ripple at full load condition at EVB end with 10 µF electrolytic capacitor in parallel with 0.1 µF MLCC.

Table 11. Test Results

Input Voltage	Full Load	Specification
90 V_{AC} / 60 Hz	101 mV_{P-P}	<150 mV_{P-P}
115 V_{AC} / 60 Hz	72 mV_{P-P}	
230 V_{AC} / 50 Hz	56 mV_{P-P}	
264 V_{AC} / 50 Hz	48 mV_{P-P}	

Waveforms:

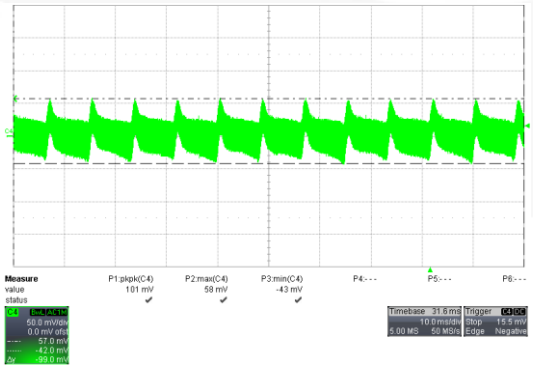


Figure 19. C4[V_O], 90 V_{AC} / 60 Hz

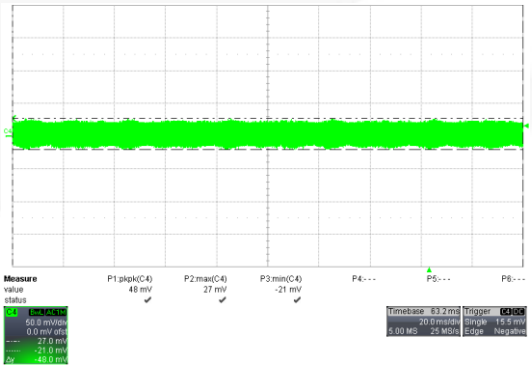


Figure 20. C4[V_O], 264 V_{AC} / 50 Hz

9.8. VDD Voltage Level

Test Condition

Measure VDD voltage at minimum, maximum loading and close over-current protection point.

Table 12. Test Results with Input Power

Input Voltage	Minimum Load	Maximum Load	Near OCP	Specification
90 V_{AC} / 60 Hz	14.71 V	19.37 V	20.82 V	< 1 W
264 V_{AC} / 50 Hz	14.40 V	18.53 V	19.63 V	

9.9. Overload Protection (OLP)

Test Condition:

Increase output loading gradually to trigger OLP and measure the debounce time.

Table 13. Test Results

Input Voltage	Minimum Load	Maximum Load	Specification
90 V_{AC} / 60 Hz	54.8 ms	54.8 ms	
264 V_{AC} / 50 Hz	53 ms	55.1 ms	

Waveforms:

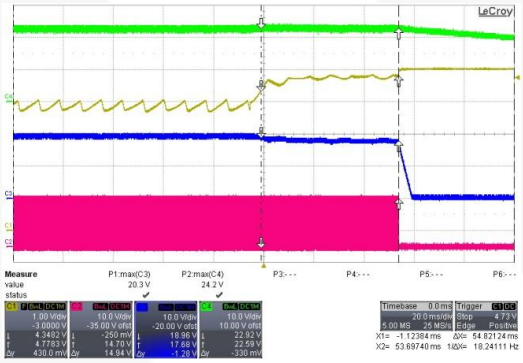


Figure 21. C1[FB], C2[GATE], C3[Vo], C4[V_{DD}], 90 V_{AC}/60 Hz

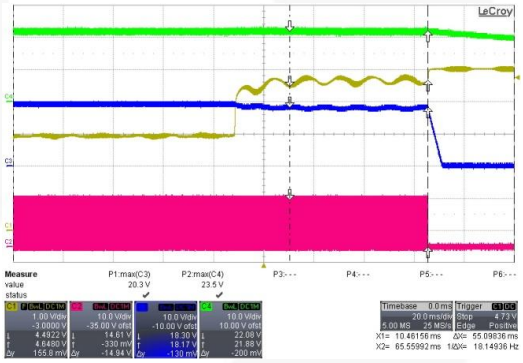


Figure 22. C1[FB], C2[GATE], C3[Vo], C4[V_{DD}], 264 V_{AC}/50 Hz

9.10. Voltage Stress on MOSFET & Rectifiers

Test Condition

Measure the voltage and current stress on MOSFET and secondary rectifier under below the conditions where the maximum voltage stress occurs.

Table 14. Test Results

		90 V_{AC}/ 60 Hz	264 V_{AC}/ 50 Hz	Specification
		Full Load	Full Load	
Normal	MOSFET	326 V	584 V	V_{DS}<650 V V_D<150 V
	Rectifier	66.4 V	117 V	
Short Circuit	MOSFET	326 V	584 V	
	Rectifier	64.9 V	124 V	

Waveforms:

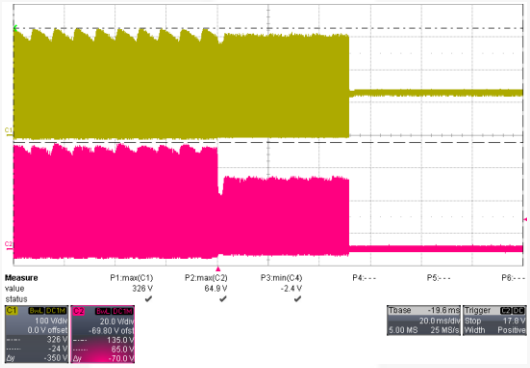


Figure 23. C1[V_{DS}], C2[V_{AK}], 90 V_{AC}/60 Hz, Full Load Output Short

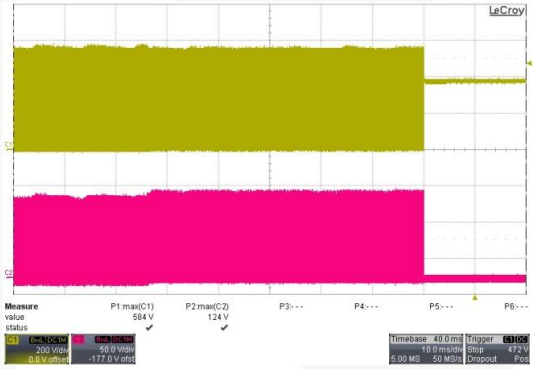


Figure 24. C1[V_{DS}], C2[V_{AK}], 264 V_{AC}/50 Hz, Full Load Output Short

9.11. Line & Load Regulation

Test Condition

Measure the line and load regulation according universal input and minimum to maximum loading.

Table 15. Test Results with CC

Input Voltage	Output Voltage at Maximum Loading	Output Voltage at Minimum Loading	Load Regulation	Specification
90 V_{AC} / 60 Hz	19.144 V	19.16 V	0.08%	< ±5%
115 V_{AC} / 60 Hz	19.146 V	19.16 V	0.07%	
132 V_{AC} / 60 Hz	19.146 V	19.16 V	0.07%	
180 V_{AC} / 50 Hz	19.146 V	19.16 V	0.07%	
230 V_{AC} / 50 Hz	19.148 V	19.162 V	0.07%	
264 V_{AC} / 50 Hz	19.148 V	19.162 V	0.07%	
Line Regulation	0.02%	0.01%		

9.12. Efficiency

Test Condition

Measure the efficiency at universal input voltage and maximum loading.

Table 16. Test Results

Input Voltage	Output Voltage	Output Current	Input Wattage	Efficiency	Average Efficiency
90 V_{AC} / 60 Hz	19.184 V	0.85 A	18.68 W	87.29%	86.55%
	19.176 V	1.69 A	37.07 W	87.42%	
	19.172 V	2.546 A	56.44 W	86.48%	
	19.162 V	3.416 A	77.02 W	84.99%	
115 V_{AC} / 60 Hz	19.172 V	0.849 A	18.425 W	88.34%	87.90%
	19.170 V	1.704 A	37.04 W	88.19%	
	19.160 V	2.545 A	55.55 W	87.78%	
	19.156 V	3.416 A	74.96 W	87.30%	
230 V_{AC} / 50 Hz	19.150 V	0.849 A	18.44 W	88.17%	88.51%
	19.156 V	1.704 A	36.90 W	88.46%	
	19.150 V	2.544 A	55.01 W	88.56%	
	19.140 V	3.414 A	73.54 W	88.85%	
264 V_{AC} / 50 Hz	19.150 V	0.849 A	18.53 W	87.74%	88.22%
	19.150 V	1.702 A	36.94 W	88.23%	
	19.148 V	2.544 A	55.03 W	88.52%	
	19.144 V	3.414 A	73.95 W	88.38%	

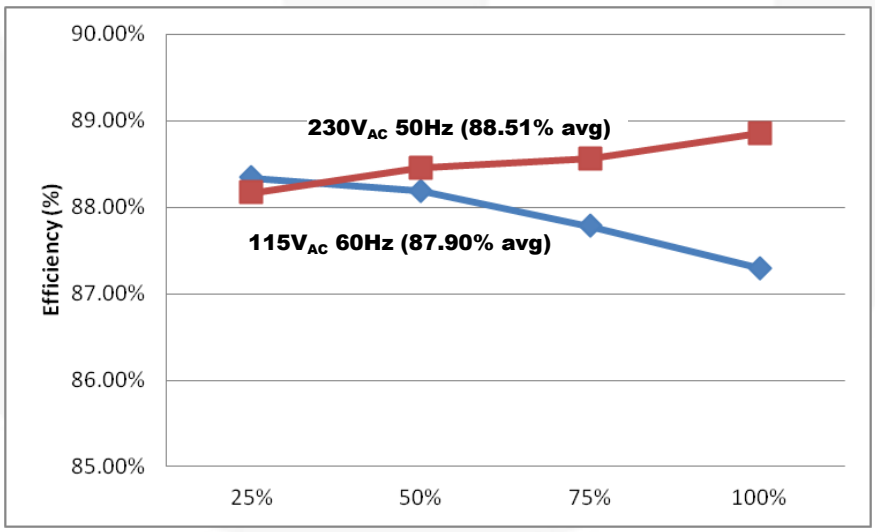


Figure 25. 4 Points Efficiency Curve

9.13. Over-Current Protection (OCP)

Test Condition

Increase output loading current gradually; and measure the output maximum current.

Table 17. Test Results

Input Voltage	Over-Current Protection	Specification
90 V_{AC} / 60 Hz	4.635 A	
115 V_{AC} / 60 Hz	4.783 A	
230 V_{AC} / 50 Hz	4.725 A	
264 V_{AC} / 50 Hz	4.657 A	

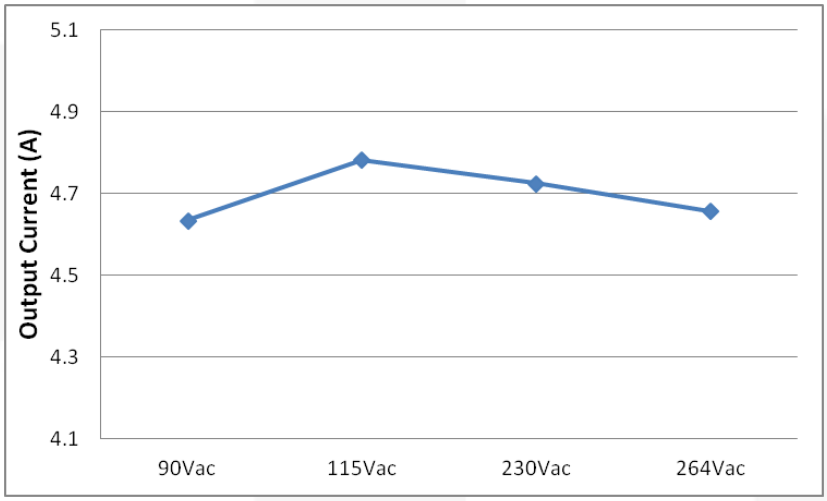


Figure 26. Output Current Protection Curve

9.14. Conducted Electromagnetic Interference (EMI)

Test Condition

- Frequency Range: 150 kHz – 30 MHz, Probe: 2-Line-LISN ENV216
- Signal Path: Receiver-2-Line-LISN ENV216, Detectors: Average
- Output Load: 5.55 Ω

Test Results:

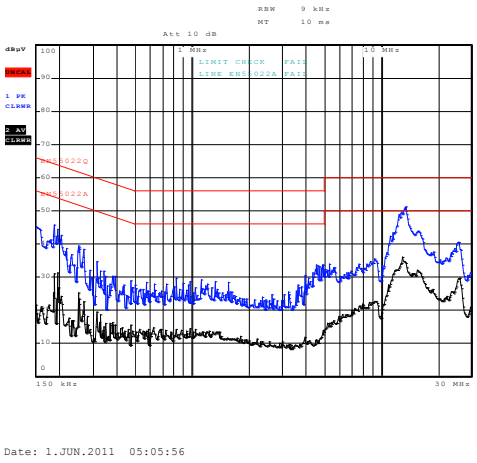


Figure 27. Line: 115 V_{AC} / 60 Hz

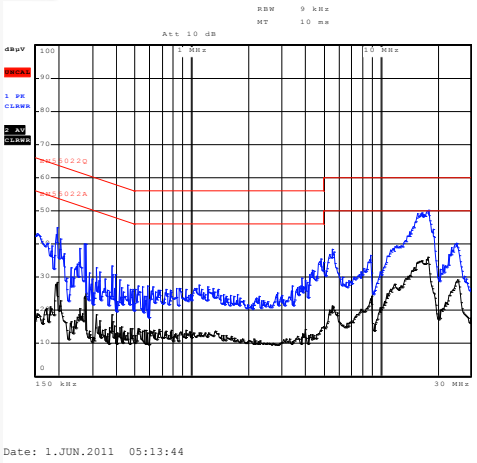


Figure 28. Neutral: 115 V_{AC} / 60 Hz

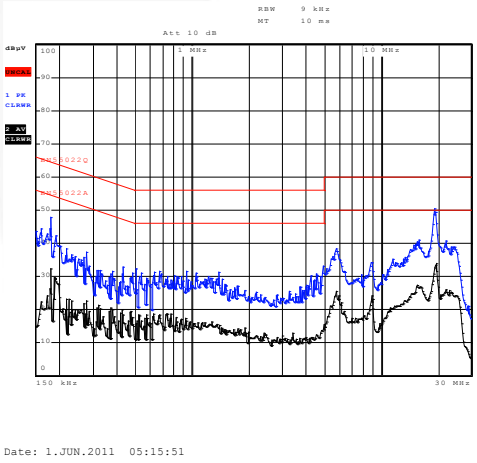


Figure 29. Line: 230 V_{AC} / 50 Hz

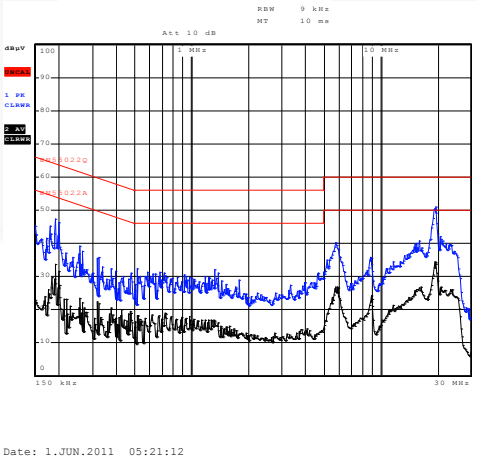


Figure 30. Neutral: 230 V_{AC} / 50 Hz

9.15. Surge Test

Test Condition

- 230 V_{AC} / 50 Hz, maximum load.
- N-PE / L-PE: (Positive & Negative) 1 kV ~ 4 kV, Phase 0°, 90°, 180°, 270°.
- L-N: (Positive & Negative) 500 V ~ 1 kV, Phase 0°, 90°, 180°, 270°.

Table 18. QC2.0 DP/DN Section Table

	L-PE	N-PE	L-N
Result	±4.4 kV	±4.4 kV	±1 kV

9.16. ESD Test

Test Condition:

- 230 V_{AC} / 50 Hz, maximum load.
- Air discharge: (Positive & Negative) 8 kV ~ 16 kV, 20 times per level.
- Contact discharge: (Positive & Negative) 4 kV ~ 8 kV, 20 times per level.

Table 19. Test Results

	Air Discharge	Contact Discharge
Result	±16.5 kV	±8.8 kV

10. Revision History

Rev.	Date	Description
1.0	January 2015	Initial Release
1.1	June 2015	Table 1, 2, and 3 updated, BOM updated, Figure 7 replaced.