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Segmented Voltage Regulator Modules (VRM) as a Solution for CPU Core Voltage

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Abstract

The PC industry continues to move closer to the goal of having DC/DC converters that deliver up to 150–200 Amp at 0.95V in the near future. This goal may be an achievable one if engineers carefully consider all of the loss mechanisms, especially loss mechanisms are that most pronounced at high currents such as 30A to 40A per phase. As a step in moving closer to this goal, we have developed a segmented VRM in the form of several modules with each one being capable of delivering up to 40 Amps per phase at efficiency over 80%. With a five phase design, DC/DC converters could deliver 200 Amps. This approach divides a multi-phase DC-DC converter into the following sections:

1. PWM controller and its associated components.
2. Power MOSFETs, MOSFET driver, Output inductor and associated components.
3. Input and output capacitors bank comprising ceramic and electrolytic type.

This application note will address only point (2) above i.e., the power train. The selection of the controller and the output and input capacitors is fairly standard and may be found in the technical publications. For each phase, the components on point (2) above which constitute all the power components are placed on a small plug-in board of 1.15" x 0.85" that delivers 40 Amps and receives the PWM TTL signal from the controller. This module has a footprint of about 0.85" x 0.25" of the motherboard space and may be placed anywhere on the board as close as possible to the CPU reducing the transmission impedance and losses and giving the Motherboard designer the flexibility to optimize the power and PCB space utilization. Each modular board may be fitted individually with its own heat sink.

Design Approach

By examining the loss mechanisms in a synchronous buck converter the individual impact on the module efficiency can be assessed and will allow us to address different choices to be made in component selection and PCB layout techniques. Loss mechanisms may be grouped as follows:

- Conduction losses = Iload^2*RDS(on)*Duty Cycle. Since both the maximum current, Iload is determined by the application and the Duty Cycle is determined by the input and output voltages specs, we only have RDS(on) to minimize for the lowest possible losses. In a synchronous buck converter operating from 12-volt input and generating an output voltage of 1 Volt, the duty cycle for the synchronous rectifier is about 91.7% this leads us to select the MOSFET with the lowest available RDS(on). By reviewing available MOSFETs datasheets, it is clear that one device will not have a low enough RDS(on) to achieve acceptable losses and hence we have to select two to do the job. The conduction losses for the high side MOSFET is much lower with a duty cycle of 8.3%, which means that we can tolerate a higher RDS(on). But as we will see in the next point a balance must be struck between the on-resistance, RDS(on) and the miller charge, Qgd and the post gate threshold gate-source charge, Qgsp to minimize the total losses. This is addressed in the next point.
- Dynamic losses = 0.5*(Rise Time + Fall Time)* Input Voltage*Iload*Switching Frequency. This form of losses is predominant in the high side MOSFET. By closely examining the above equation we can partition the individual parameters influence as follows:
- The rise and fall times are dominated by the MOSFET Qgd and Qgsp. The high side MOSFET must have the lowest possible Qgd and Qgsp with an acceptable on-resistance RDS(on) to satisfy the previous point. At 40 Amps output current the conduction losses still dominate dictating the choice of the most suitable device to have as low as possible RDS(on) even at the expense of higher dynamic losses to achieve the optimum combined dynamic and conduction losses. This very fact, lead us to select a MOSFET typically used for the synchronous rectifier application for the high side device to minimize the total losses.
- The rise and fall times are also dependant on the gate driver source resistance, rise and fall time of the drive waveforms and maximum source and sink currents. Pspice testing done in preparation for this work shows clearly that we ideally need a driver that is capable of delivering 4–5 Amps and a drive signal of about 3–5ns rise and fall times. Unfortunately such drivers are not available in the market right now instead, we selected a driver capable of delivering 2 amps at rise and fall times of slightly over 5 ns.
- The switching frequency is sometimes determined based on the control loop bandwidth requirements, maximum

ripple voltage and current, PCB real estate and maximum losses allowed. Determination of the switching frequency for this application is probably the single most important decision to make and has to be made after careful considerations. The switching frequency was selected to be 200KHz for the following reasons:

a. Since the dynamic losses are directly proportional to the switching frequency, a lower frequency of 200KHz is a good compromise.

b. The losses due to the source inductance effects (see reference [1], [2] and [3]) will also be minimized since it too is dependant on the switching frequency.

c. At this high power level, the heat generated by the DC-DC converter has to be removed from the VRM and ultimately from the computer case by the cooling system. In my opinion, this is a new fact of life that thermal design engineers have to deal with very seriously when dealing with this new generation of Core supplies. This fact translates into two definite requirements the first, air flow of about 400 FPM must be provided for the VRM board and the second is a suitable heatsink must be used on the VRM.

d. At 200KHz switching frequency, the inductor size is still small and does not need any more PCB real estate compared to say 300KHz.

e. The reduction in the control loop bandwidth is minimum. As a rule of thumb, the bandwidth is between 1/4 to 1/10 the switching frequency. For a BW = 1/6 the BW for 200KHz = 200/6 = 33.3KHz while at 300KHz the BW = 300/6 = 50KHz a difference of 16.3KHz. This is unlikely to cause any load transient problems and is quite unlikely to require any more output filter capacitors either.

- Printed circuit and power connector Ohmic losses. Using multiplayer PCB with 2Oz copper or more for as many layers as possible may control these losses. Clearly it costs more to have more layers with heavier copper but remember that with 40 amps per inch^2, this is the only way to go or we will have significant amount of copper losses. My choice was to go for 8 layers of 2OZ copper. This will allow us to allocate adequate number of layers with low enough parasitic resistance to carry the heavy currents in different circuit nodes while reducing the parasitic inductance in all the critical nodes like the drain of the HS MOSFET, the switching node and the source of the synchronous rectifier allowing fast switching while significantly limiting the ringing everywhere on the board. Figure 6a depicts the switching node waveform where the ringing is reduced to a very small value at 40 amps compared to Figure 6b of a typical layout at a current of 15 amps only. This significant improvement has been achieved by the choice of the BGA package and the layout technique that we will discuss later on in this paper.

Table 1

Package	Parasitic Resistance	Lss	Ldd	Lgg
SO8	2290μΩ	690pH	318pH	1800pH
BGA, 5x5.5	58μΩ	6pH	30pH	40pH
BGA, 2x2.5	209μΩ	10.5pH	54pH	32pH

- Losses due to MOSFET source inductance (see reference [1], [2] and [3]) as follows.
- In a synchronous buck converter, tests and simulation show that during the turn off of the high side MOSFET the source inductance will develop a negative voltage across it due to $\text{ParasiticInductance} \times \frac{\partial \text{Idrain}}{\partial t}$ forcing the MOSFET to continue to conduct even after the Gate has been fully switched off. This has the effect of increasing the dynamic losses due to the slower fall time of the drain current brought on by the total source inductance. This effect will cause slower drain current fall time for higher current i.e. higher current per phase will result in disproportionate increase in the dynamic losses. The best way to minimize this effect is to choose a package that has very low source inductance and practice good high frequency PCB layout techniques. Table 1 shows a comparison between several packages. Notice that the BGA package has a negligible source inductance compared to say SO8, which in fact is several orders of magnitude larger than that of the 5x5.5 mm BGA package. In summary the source inductance effect is governed by the following factors:
- The total effective source inductance. This includes both the package source inductance and PCB source trace inductance. Both must be minimized for acceptable switching losses
- MOSFET gate threshold voltage and forward Trans-conductance, gm and Load current
- Capacitive losses, C*V^2*f where there is very little that can be done to reduce these losses other than selecting a MOSFET with lower inter-electrode capacitance and reduce the switching frequency. In general this type of losses is less than 1–3% of the total losses in the circuit and may be considered a secondary effect.

Component Selection

The topology used in this application is the synchronous buck converter which offers the best combination of simplicity and high efficiency combined with a low total cost compared to any other topology. Figure 1b depicts a synchronous buck converter with parasitic inductances in the gate and source of the MOSFETs. Figure 1a depicts the efficiency as a function of the HS MOSFET RDS(on) and load current based on an extended mathematical model. It can be seen that the optimum RDS(on) for the HS MOSFET

is around 7 mΩ. The MOSFETs chosen were one FDZ7064S for the high side and two FDZ5047N for the synchronous rectifier. Table 1 is a brief summary of the specifications.

MOSFET	RDS(on) @ 10V Typ.	RDS(on) @ 4.5V Typ.	Gate Charge Typ.	Gate Thresh-old Typ.
FDZ7064S	5.0 mΩ	7.0 mΩ	6.0nC	1.4 V
FDZ5047N	2.3 mΩ	3.2 mΩ	Qg = 52nC	1.3 V

The inductor was selected to be 1µH. This will allow us to limit the current ripple to a manageable level.

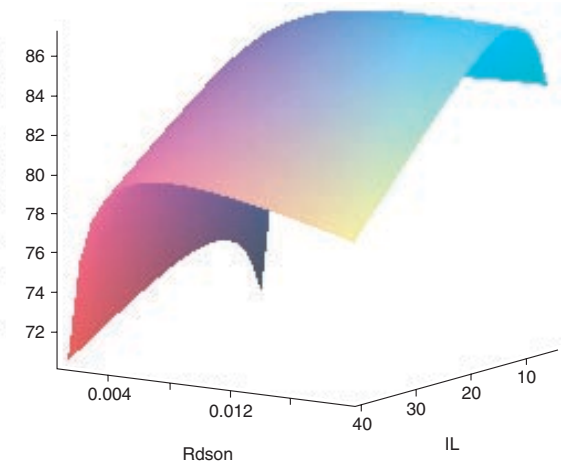

Figure 1a. Efficiency as a function of the HS MOSFET

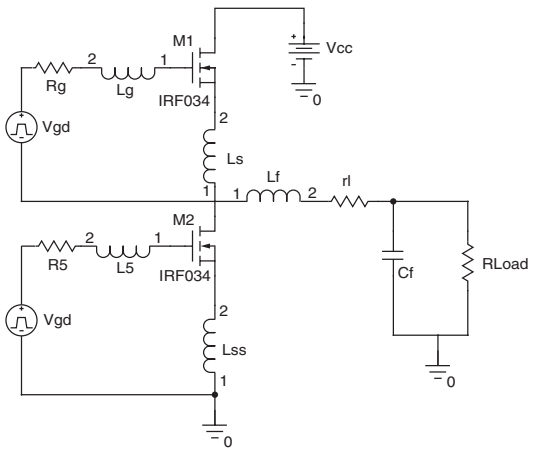

Figure 1b. Synchronous Buck converter showing parasitic inductances

Layout Approach

The pivoting principle around which the layout approach revolves is to minimize all parasitics to the greatest extent possible. This applies to the following:

- The PCB parasitic resistance, which is dealt with by having 8 layers of 2OZ copper. The use of vias right under the BGA package allows the switching current to be carried by several layers right from the beginning significantly reducing the effective trace resistance. See Figure 3 for details.
- The MOSFET package parasitic inductance. The choice here was clearly to go with the BGA package which is several orders of magnitude better than packages like SO8 and DPAK.
- The PCB parasitic inductance. Again the use of vias right under the BGA package allows the switching current to be carried by several layers right from the beginning significantly reducing the effective trace inductance. See Figure 3 for details. This can clearly be seen in Figure 6 when comparing the switching waveform of the module (a) with another PCB using DPAK on a four-layer board (b).

Figure 2 depicts the connection of the MOSFETs. Notice the source connection for minimum source inductance while the gate trace is kept at a minimum. Figure 3 shows in detail the usage of tinted vias that help distribute the current to several layers right at the device source. As mentioned above, this helps to drastically reduce both the parasitic resistance and inductance.

Thermal Management

The output power for each module = 40 Amps x 1.5V = 60 Watt. For a total power efficiency of 88.5%, the power dissipation in each module = (60 / .885) – 60 = 7.79 Watt dissipated in one inch^2. A heatsink with airflow of 400 FPM is needed to remove this heat from the board and maintain a board temperature of less than 105°C.

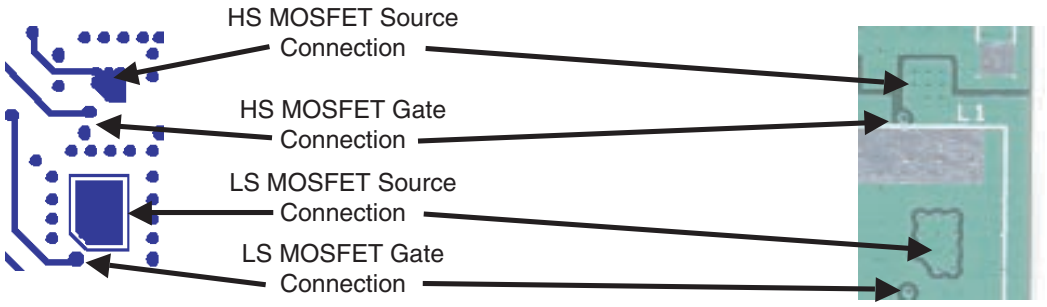

Figure 2. Gate and Switching node connection

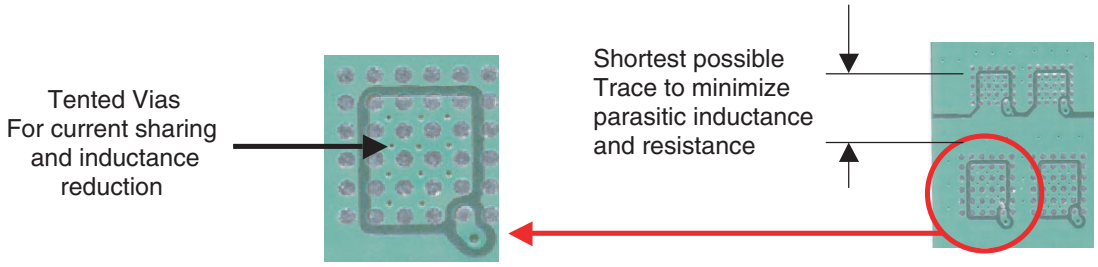

Figure 3. Use vias to accomplish low parasitic resistance and inductance

Efficiency

Figure 4 depicts the measured overall power efficiency for a two-phase 80 Amps implementation. Each module was fitted with a heatsink and placed in 400 FPM airflow. The efficiency at 40 Amps per phase or a total of 80 Amps was measured to be 88.5%. This efficiency value measured at 40 Amps per phase and achieved with only three BGA MOSFETs per phase rivals those of 20 Amps per phase solutions that use a much larger number of MOSFETs in traditional packages to achieve the same results.

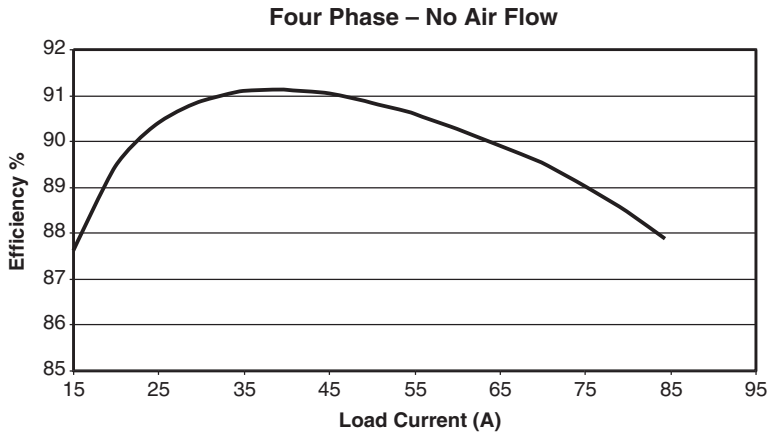

Figure 4. Efficiency Curve for two phase application

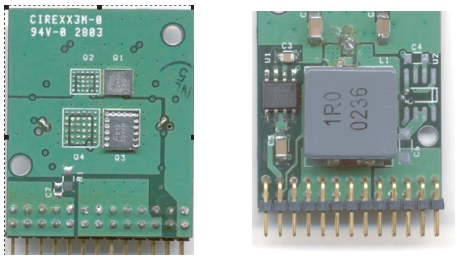

Figure 5. Final module with components mounted on both sides

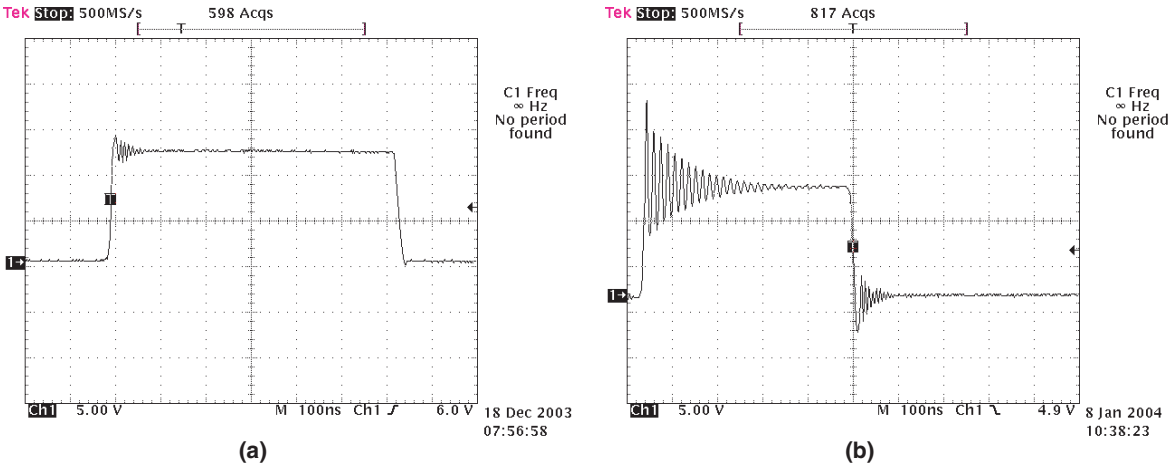

Figure 6. Switching node waveform for the module (a) and a typical layout (b)

Conclusion

With the industry' current per phase hovering between 25–30 Amps, the VRM solution proposed in this application note offers an innovative alternative. Not only does it operate at 40 Amp per phase, it offers a flexible and small module that gives designers the flexibility of placing the module in the best position to minimize power losses and maximize transient response and load line. Furthermore, this VRM solution presents an excellent choice for the PC market as it has the largest power density per phase while maintaining a safe PCM temperature.

References

[1] Alan Elbanhawy, "Effect of Parasitic Inductance on switching performance" *in Proc. PCIM Europe 2003, pp.251–255*

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[4] Alan Elbanhawy, "A quantum Leap in Semiconductor packaging" in Proc. *PCIM China, pp. 60–64*

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